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Isolated Single-stage Power Electronic Building Blocks Using Medium Voltage Series-stacked Wide-bandgap Switches

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ISOLATED SINGLE-STAGE POWER ELECTRONIC BUILDING BLOCKS USING MEDIUM VOLTAGE SERIES-STACKED WIDE-BANDGAP SWITCHES

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by

Noureldeen Mohamed Anwar Elsayad

2019

To: Dean John Volakis
College of Engineering and Computing

This dissertation, written by Noureldeen Mohamed Anwar Elsayad, and entitled Isolated Single-Stage Power Electronic Building Blocks using Medium Voltage Series-Stacked Wide-Bandgap Switches, having been approved in respect to style and intellectual contents, is referred to you for judgment.

We have read this dissertation and recommend that it be approved.

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Date of Defense: November 13, 2019

The dissertation of Noureldeen Mohamed Anwar Elsayad is approved.

Dean John Volakis
College of Engineering and Computing

Andrés G. Gil
Vice President for Research and Economic Development
and Dean of the University Graduate School

Florida International University, 2019

DEDICATION

For their endless support, love, and sacrifice, I dedicate this work.

To my Beloved Parents and my Sister

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I would like to thank my supervisor, Professor Osama Mohammed, for supervising me in this work, and for providing me with endless research ideas and technical support. He also provided me with financial support through a research assistantship in his research group working on his research projects and for some semesters as a teaching assistant at the Electrical and Computer Engineering Department at FIU. I would also like to thank Professor Mohammed for making me a part of the Energy System Research Laboratory and for the excellent facilities made available for this project. I have gained a lot of skills and experience at ESRL with its first-class equipment needed to build and experimentally verify the results. This helped me complete my doctoral studies and enabled scholarly production resulting from this project. Also, as my doctoral research started to gain traction, Professor Mohammed provided me opportunities to grow within my professional career inside and outside the university and helped me build my own name in this field.

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ABSTRACT OF THE DISSERTATION

ISOLATED SINGLE-STAGE POWER ELECTRONIC BUILDING BLOCKS USING MEDIUM VOLTAGE SERIES-STACKED WIDE-BANDGAP SWITCHES

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Professor Osama A. Mohammed, Major Professor

The demand for efficient power conversion systems that can process the energy at high power and voltage levels is increasing every day. These systems are to be used in microgrid applications. Wide-bandgap semiconductor devices (i.e. Silicon Carbide (SiC) and Gallium Nitride (GaN) devices) are very promising candidates due to their lower conduction and switching losses compared to the state-of-the-art Silicon (Si) devices. The main challenge for these devices is that their breakdown voltages are relatively lower compared to their Si counterpart. In addition, the high frequency operation of the wide-bandgap devices are impeded in many cases by the magnetic core losses of the magnetic coupling components (i.e. coupled inductors and/or high frequency transformers) utilized in the power converter circuit.

Six new dc-dc converter topologies are propose. The converters have reduced voltage stresses on the switches. Three of them are unidirectional step-up converters with universal input voltage which make them excellent candidates for photovoltaic and fuel cell applications. The other three converters are bidirectional dc-dc converters with wide voltage conversion ratios. These converters are very good candidates for the applications

that require bidirectional power flow capability. In addition, the wide voltage conversion ratios of these converters can be utilized for applications such as energy storage systems with wide voltage swings.

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PV	Photovoltaic
EV	Electric Vehicle
MV	Medium Voltage
LV	Low Voltage
PCC	Point of Common Coupling
LVRT	Low Voltage Ride-Through
HCC	Hysteresis Current Controller
MF	Medium Frequency
HF	High Frequency
CHF	Cascaded High Frequency
ESS	Energy Storage System
MPPT	Maximum Power Point Tracker
RMS	Root Mean Square
n	Number of cells per phase
m	Transformer turns ratio between the primary and one of the secondary windings
C_{dc}	Capacitor connected to the LV dc bus of the station
V_{DC}	Voltage of the LV dc bus of the station
V_{PCC}	RMS Voltage at the *PCC*
P_{PCC}	Active power flowing through the *PCC*.
Q_{PCC}	Reactive power flowing through the *PCC*.

i_d^*, i_q^*	Reference d-q components of the 3-phase grid currents flowing through the *PCC* under normal operation
i_d , i_q	d-q components of the 3-phase grid currents flowing through the *PCC*
i_{dlv}^*, i_{qlv}^*	Reference d-q components of the 3-phase grid currents flowing through the *PCC* for LVRT operation
$cell_{ij}$	Cell number *j* in phase *i*
K_{ij}	Switching state of $cell_{ij}$
H_{ij}	Desired output state of $cell_{ij}$
r_i	Polarity signal of phase *i* current
Q	Switching state of the single phase inverter connected to the transformer primary winding
e(k)	Current error signal at instant *k*
e(k-1)	*Delayed current error signal* at instant *k-1*
i_a, i_b, i_c	3-phase currents flowing through the *PCC*
I_{rated}	Rated current of the CHF ac-link system
P_{EV}	EV chargers power demand.
P_{PV}	Generated PV power
K_{P1}	Proportional coefficient of PI controller 1
K_{I1}	Integral coefficient of PI controller 1
K_{P2}	Proportional coefficient of PI controller 2
K_{I2}	Integral coefficient of PI controller 2

GaN	Gallium Nitride
SiC	Silicon Carbide
Si	Silicon
PEBB	Power Electronic Building Block
SC	Switched-Capacitor
SL	Switched-Inductor

Chapter 1 Introduction to Power Electronic Building Blocks

1.1 Introduction

There is a growing global interest in adopting renewable energy sources at large-scale to decrease the reliance on fossil fuels and reduce the CO_2 emissions [1]-[14]. In addition, the recent developments in energy storage systems made the electrification of transportation more economically feasible [15]-[30].

Power electronic converters play a critical role in interfacing the different power sources and the loads, where they can provide the following functions:

1) Solving the voltage mismatch between the power source bus and the load bus.
2) Extract the maximum power from a power source (e.g. photovoltaic systems, wind energy turbines, fuel cells, etc.).
3) May provide galvanic isolation between the power sources and the load.
4) Control the speed and torque of electric motors.
5) In case of grid-connected power electronic systems, they can support the voltage during voltage sags and support the nominal grid frequency during contingencies, by adequately controlling the injected active and reactive power to the grid [31]-[45].

The concept of the Power Electronic Building Blocks (PEBBs) is based on synthesizing all the important power electronic systems from few generic power electronic structures, which are referred to as PEBBs. This approach can result in the following outcomes:

1) Reduction of the number of the spare parts of the power electronic systems onboard a ship or an aircraft.

2) The mass production of few generic structures can dramatically reduce the total cost of the power electronic systems.
3) Reduction of the complexity of the maintenance of the power electronic systems.

The two-level synchronous buck structure (push-pull configuration) is the basic building block of all the conventional power electronic systems (i.e. buck dc-dc converter, boost dc-dc converter, buck-boost dc-dc converter, single-phase dc-ac inverter, three-phase dc-ac inverter, single-phase ac-dc active rectifier, and three-phase ac-dc active rectifier), due to its simple circuit structure, low number of active and passive components, simple controller structure, and simple gate driver circuits. In addition, it has a common ground between its input and output ports which reduces the electromagnetic interference (EMI) noise and require less periodic maintenance. Nevertheless, the voltage-conversion-ratios of this converter are low, hence, to achieve a high voltage conversion ratio, the converter needs to operate at an extreme duty cycle value where its efficiency deteriorates significantly [46].

Designing high-order power electronic converters with wide-voltage-conversion-ratios as PEBBs can be a step forward towards more efficient and compact power electronic systems. The different categories of the PEBBs and their different configurations will be briefly presented. Then, the utilization of high-voltage series-stacked wide-bandgap (WBG) devices will be discussed.

1.2 Overview of the Power Electronic Building Blocks

The Power Electronic Building Block (PEBB) is a generic power electronic converter circuit that can be configured in different ways to synthesize popular power electronic architectures (DC-DC, DC-AC, AC-DC, and AC-AC converters). This can reduce the number of spare parts needed onboard a ship, plane, … etc., also the PEBB can reduce the

manufacturing cost of the power electronic systems since the mass production of one generic power electronic architecture is more economical than producing application-specific power electronic architectures.

Many literature have discussed different possible architectures for the PEBB, however, all of them are either implemented using Silicon (Si), or Silicon Carbide (SiC) Metal Oxide Field Effect Transistors (MOSFETs) or Insulated Gate Bipolar Junction Transistors (IGBTs) [47]-[49], which suffer from high conduction and switching losses. In [50], a PEBB is built with Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) to reduce the conduction and switching losses of the transistors, since the GaN HEMTs have lower on resistance (Ron) and less device total charge. The major problem with GaN HEMTs is that their break down voltage is relatively lower compared to Si and SiC MOSFETs or IGBTs, which limits the utilization of GaN HEMTs to the low voltage applications. Multilevel half-bridge configurations can enable the utilization of GaN HEMTs in high voltage applications.

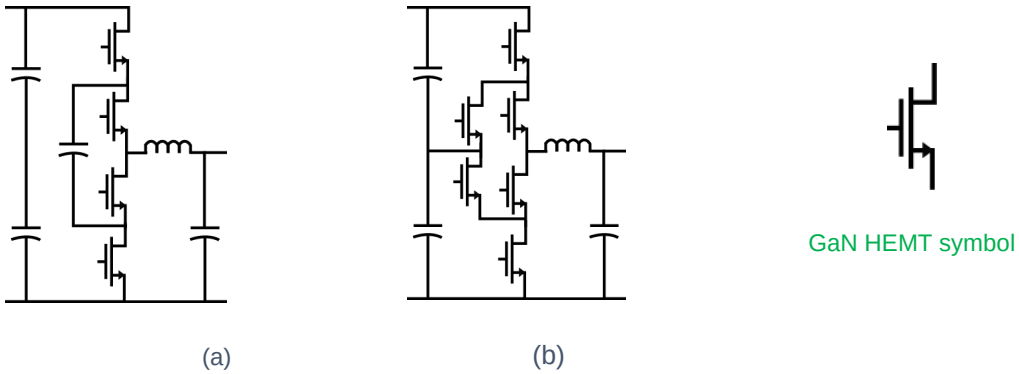
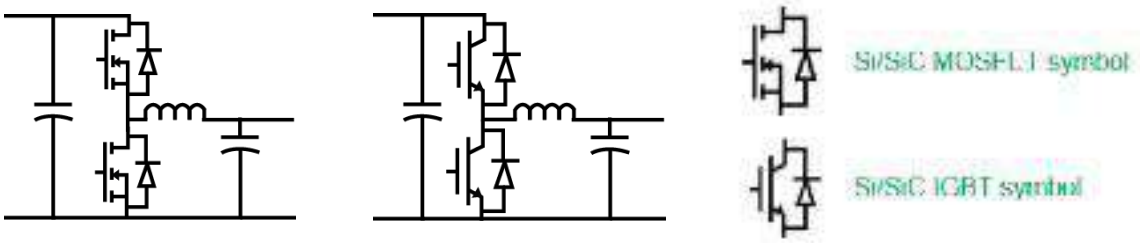


Figure 1.1: Possible multilevel half-bridge-based PEBBs, (a) Flying capacitor leg. (b) Neutral point clamped leg.

These multilevel half-bridge configurations can possibly be based on a flying capacitor (FC) leg (as shown in Figure 1.1(a)) or a neutral point clamped (NPC) leg (as shown in Figure 1.1(b)). The major problem of multilevel configurations is that they require a complex control scheme and more switches (as in the NPC) or more high voltage capacitors (as in the FC). The

two level half-bridge-based PEBB is the most popular topology in literature and is composed of two transistors, these transistors can be either Si or SiC MOSFETs (shown in Figure 1.2(a)) or IGBTs (shown in Figure 1.2(b)). This PEBB architecture is limited by the rated voltage of the transistors and suffers from high switching and conduction losses.



(a) (b)

Figure 1.2: Two level half-bridge-based PEBB, (a) Using Si/SiC MOSFETs. (b) Using Si/SiC IGBTs.

As a solution to extend the operating voltage of the PEBB beyond the rated voltage of the single transistors, a multilevel neutral-point-clamped (NPC) half-bridge can be a PEBB.

The rated voltage of this PEBB = (number of levels – 1) X rated voltage of each transistor. In [48], and [49], a NPC half-bridge-based PEBB built with SiC MOSFETs is presented. This NPC can be built with Si/SiC MOSFETs (as shown in Figure 1.3(a)), Si/SiC IGBTs (as shown in Figure 1.3(b)), or GaN HEMTs (as shown in Figure 1.1(b)). The major disadvantages of this PEBB architecture:

- Requires high number of semiconductor devices.
- Requires a complex control scheme.

Another architecture that can be used to extend the rated voltage of the PEBB beyond the rated voltage of the single transistors is a flying-capacitor (FC) half-bridge-based PEBB, where a FC half-bridge is used as a PEBB.

The rated voltage of this PEBB = (number of levels – 1) X rated voltage of each transistor.

This FC can be built with Si/SiC MOSFETs (as shown in Figure 1.4(a)), Si/SiC IGBTs (as shown in Figure 1.4(b)), or GaN HEMTs (as shown in Figure 1.1(a)). The major disadvantages of this PEBB architecture:

- Requires high number of capacitors, which increases the weight and size.
- Requires a complex control scheme.

(a) (b)

Figure 1.3: NPC-based PEBB, (a) Using Si/SiC MOSFETs. (b) Using Si/SiC IGBTs.

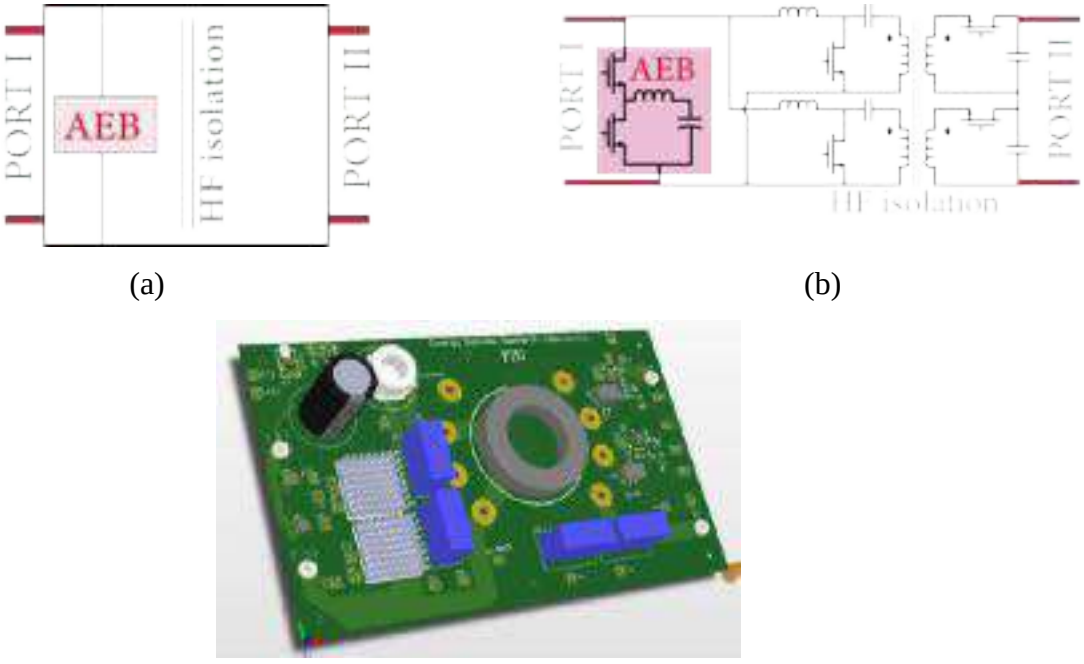
(a) (b)

Figure 1.4: FC-based PEBB, (a) Using Si/SiC MOSFETs. (b) Using Si/SiC IGBTs.

1.3 Isolated Power Electronic Building Blocks

The isolated power electronic building block (I-PEBB) is basically an isolated generic power electronic structure that can be used to perform any dc-dc, dc-ac, ac-dc, or ac-ac process. This I-PEBB can be based on the bidirectional version of any dc-dc converter (e.g.

flyback, forward, isolated SEPIC, isolated Ćuk, etc.). . A design example of an I-PEBB based on a modular bi-directional isolated SEPIC converter with an active energy buffer (AEB) is shown in Figure 1.5, where the block diagram of the I-PEBB is shown in Figure 1.5(a) and it consists of an input port (port I), output port (port II), high frequency (HF) isolation, and an AEB. The AEB can be achieved using two transistors in push-pull configuration with a small LC filter, as shown in Figure 1.5(b).



(a) (b)

(c)

Figure 1.5: Design example of a modular-SEPIC-based I-PEBB (a) Block diagram. (b) Circuit diagram. (c) 3D PCB layout.

The AEB acts as an active power decoupling stage between two consecutive I-PEBBs. The HF magnetic isolation is integrated on the PCB of the I-PEBB, as shown in Figure 1.5(c).

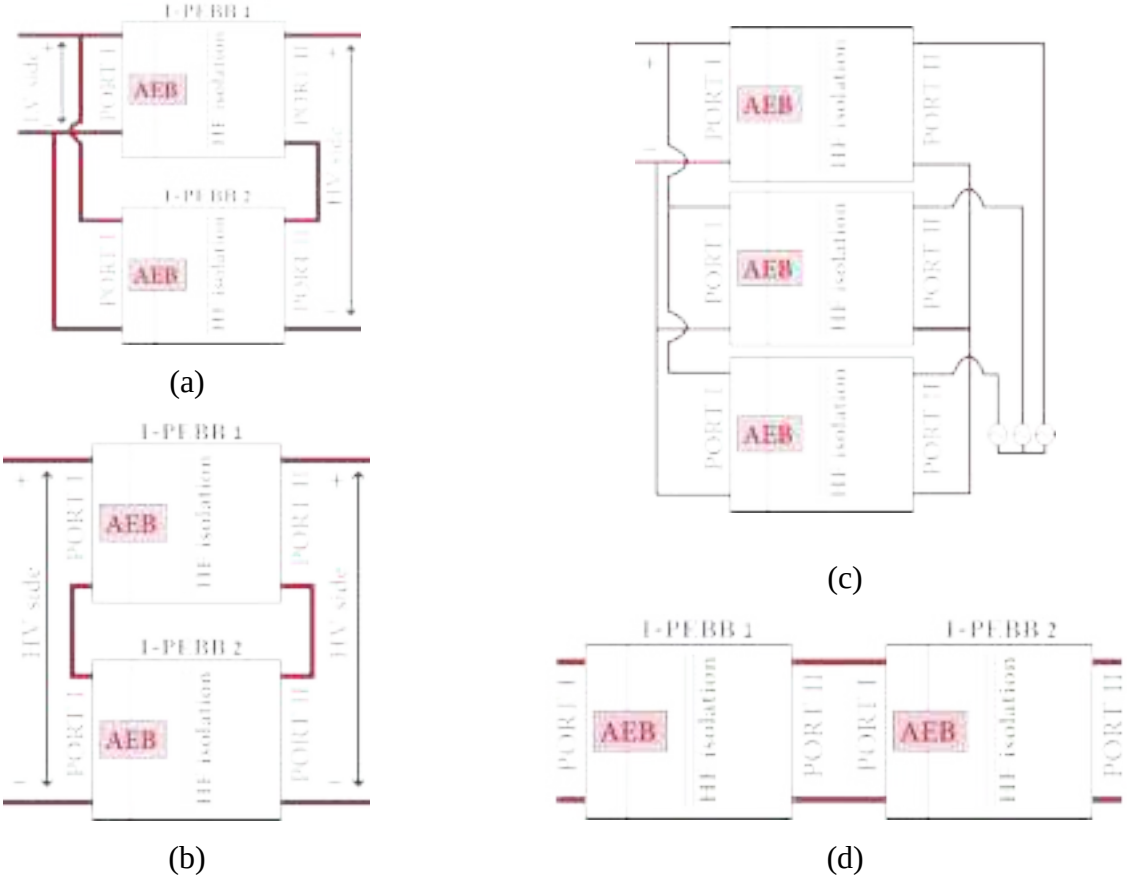


Figure 1.6: Possible configurations using the I-PEBB (a) IPOS. (b) ISOS. (c) Three phase differential-mode DC-AC system. (d) Consecutive stacking.

The I-PEBB provides galvanic isolation between the input and output ports, hence, it can be used to synthesize any power processing system based on "Input-Parallel-Output-Series" (IPOS), or "Input-Series-Output-Series" (ISOS) architectures, as shown in Fig. 1.6(a) and Fig. 1.6(b), respectively. Both ISOS and IPOS architectures can be used to synthesize power converters that can be used for medium and high voltage applications. Isolated DC/AC power processing systems can be synthesized using two I-PEBBs (for single phase) or using three I-PEBBs (for three phase) systems, as shown in Fig. 1.6(c). Consecutive stacking of the I-PEBBs can be used to synthesize more complex systems such as AC/AC power processing systems.

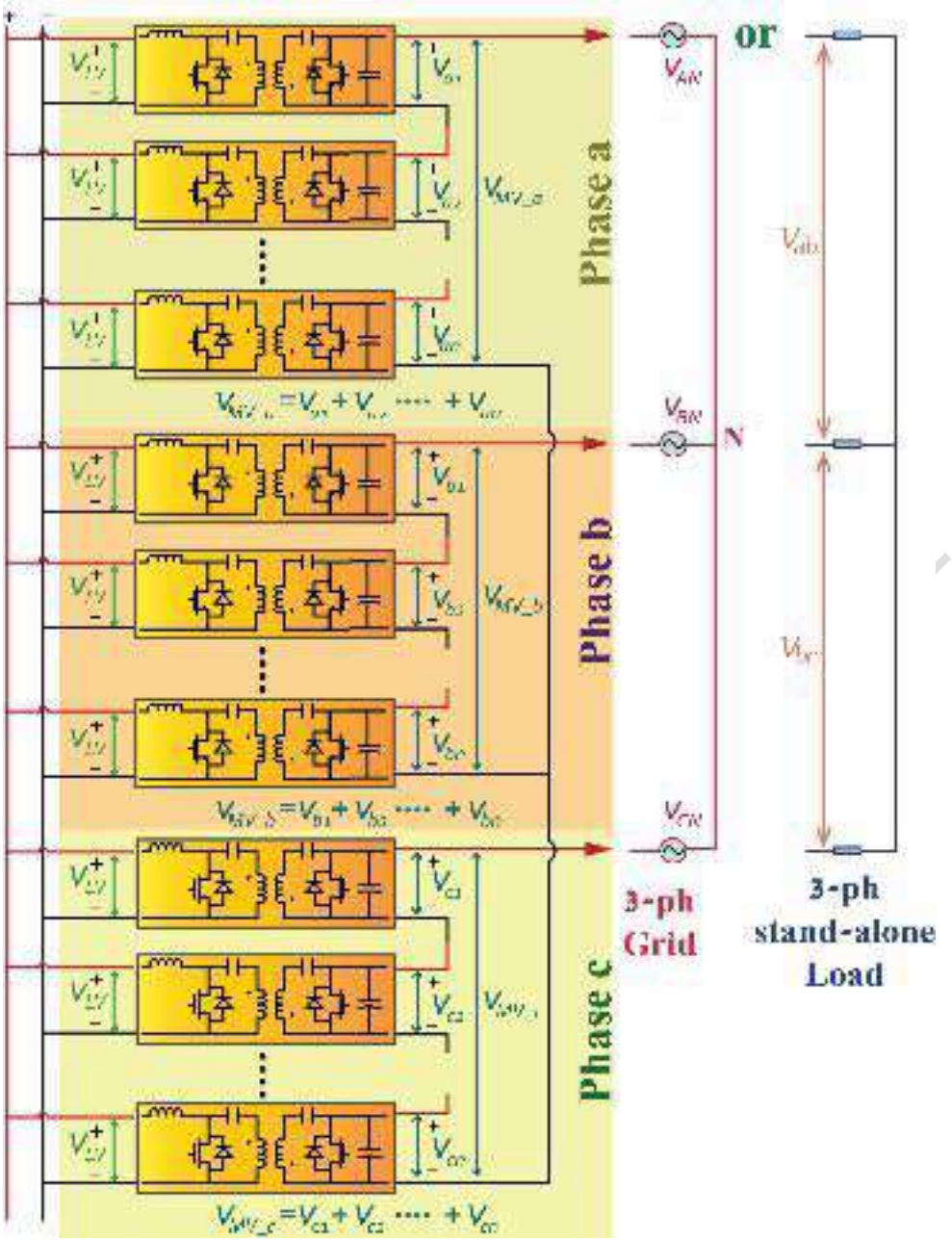


Figure 1.7: A three-phase modular isolated inverter system based on the bidirectional version of the isolated Ćuk converter.

A three-phase modular inverter based on the bidirectional Ćuk converter is shown in Figure 1.7, as each phase is composed of an IPOS system. This topology is an example of an I-PEBB based on the Ćuck converter-based I-PEBB.

1.4 Transformerless High-Order Power Electronic Building Blocks

In the past decade solid-state transformers (SST) have emerged as a promising compact solution to interface low voltage sources/loads to the MVDC bus of the ship by utilizing transformers operating at high frequencies (1kHz < frequency < 100kHz).

The advent of wide-bandgap (WBG) semiconductor devices (i.e. Silicon Carbide (SiC), and Gallium Nitride (GaN) devices) which can switch efficiently at frequencies higher than 100 kHz, enables the power electronic stages to operate at these high switching frequencies.

With the advancements taking place to these WBG devices and the increasing capability to switch at much higher frequencies, the utilization of the SST with high-frequency transformers faces a big challenge. This challenge is due to the increasing core losses of these transformers which puts a limit to the reduction of the power electronic stage size and weight.

Adopting multilevel switching networks have the following advantages:

1) Distribution of the voltage stress over the power transistors, which enables the utilization of transistors with low voltage rating, which leads to a more efficient power conversion process.

2) The effective frequency that is used to design the passive components (inductors, and capacitors) equals $(n-1).f_s$, where n, and f_s are the number of levels of the switching network, and the switching frequency, respectively. This feature minimizes the needed capacitance and inductance of the converter, leading to minimization of the passive components size. For instance, if f_s = 100 kHz, and n = 16, the effective switching frequency used to design the passive components = 1.5 MHz.

The generic structure of a converter with a multilevel switching network is shown in Figure 1.8. It is composed of an array of transistors and an intermediary circuit. This intermediary

circuit is usually a capacitor network (i.e. flying capacitor network), or a diode network (i.e. neutral point clamped network), and this intermediary network distributes the voltage stress equally across the transistors.

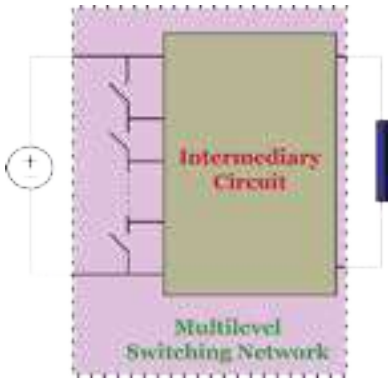


Figure 1.8: Generic structure of a power converter with an integrated multilevel network.

Adopting High-Order Impedance networks have the following advantages:

1) Enhancing the voltage gain of the power electronic stage.

2) Reducing the voltage stress on the power transistors.

The high impedance network is composed of a number of capacitors and inductors to enhance the voltage gain of the power converter and enable it to reach high values without the need for a transformer.

It is worth mentioning that, for high frequency operation (>1MHz), the inductors will work in continuous conduction mode (CCM) with ripple current less than 5%, thus, the core losses of the inductors of the high impedance networks can be neglected.

A generic architecture of a converter with high-order impedance networks is shown in Figure 1.9. The impedance networks can either be before the switching network, after the switching network, or in both locations.

The impedance network after the switching network enhances the voltage gain and reduces the voltage stress on the transistors, while the other impedance network enhances the voltage gain further.

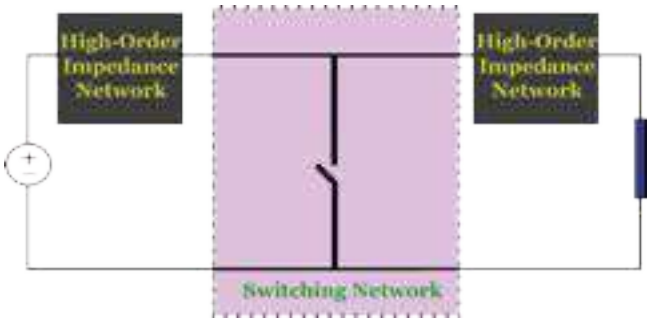


Figure 1.9: Generic structure of a power converter with an integrated high-order impedance network

Adopting High-Order Impedance and multilevel switching networks have the following advantages:

1) High voltage gain without the need for a transformer.

2) Less voltage stress on the transistors compared to conventional multilevel architecture, which makes it feasible to implement this family of converters with transistors with low voltage ratings.

(Note: Transistors with lower rated voltage have the capability to switch much faster and more efficiently compared to their counterparts with higher rated voltage).

3) The effective frequency of the proposed high-order multilevel converters can be optimized to be in the Mega-hertz range, by properly selecting the number of levels of the switching network, and optimally designing the high impedance networks.

4) Absence of core losses, because of the absence of transformers, and operating the inductors in CCM mode with low current ripples.

A generic architecture of the proposed converters with multilevel high-order impedance networks is shown in Figure 1.10.

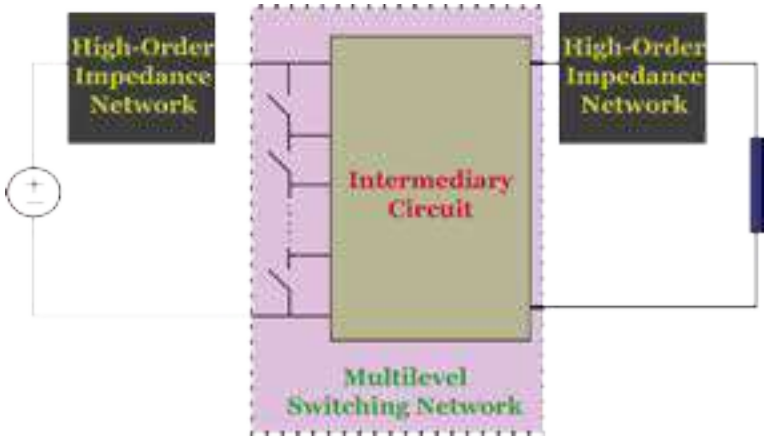


Figure 1.10: Generic structure of a power converter with an integrated multilevel high-order impedance networks.

1.5 Series-Stacked WBG Devices for High-Voltage Applications.

Currently the maximum breakdown voltage of available semiconductor switching devices is lower than the voltage needed for medium-voltage and high-voltage power systems. In order to increase the breakdown voltage of semiconductor switching devices, it is meaningful to use multiple of them in series connection. However, this approach is impeded by the non-ideality of the switches, leading to transit unequal voltage sharing across the series switches, which may in turn result in cascaded failure of the switches [51]. An investigation is needed when using devices in series, since both static (steady-state) and dynamic (switching transition) voltage balancing of devices are very critical and need to be satisfied.

The major concern in using semiconductor switching devices in series is identical voltage sharing between them in static and dynamic operation. When the switches are OFF (static),

the difference between their leakage currents and also their output capacitances cause unequal blocking voltage across them. Static voltage balancing can be simply achieved by using a resistor with optimized value in parallel with each device. In switching transitions (dynamic), it is more difficult to guarantee equal voltage sharing between devices [52].

The methods for solving dynamic voltage sharing issue of series devices can be classified into load-side and gate-side techniques. The simplest technique is to use a passive snubber circuit in the load-side. In this approach, excessive power losses is introduced in the snubber resistors specifically in high-power applications [52]. To solve this problems, active gate control techniques are introduced in which a control loop is designed to control the devices voltage using an active gate control circuit. This approach requires a complex drive circuit, has low reliability and high switching loss [51], [53].

Recently, another category of techniques has been proposed that utilize simple auxiliary voltage balancing circuits in the gate-side of series connected semiconductor switching devices. These techniques that are usually referred to as quasi-active gate controllers, have less complex gate driver, lower switching losses, lower cost, and higher reliability compared to active gate control schemes [51]-[53].

So far, a lot of studies are conducted on series connection of Si switching devices and also SiC MOSFETs to enhance the breakdown voltage. Yet there appears to be a lack of a comprehensive study on series-connected GaN-HEMTs. As explained, GaN-HEMTs offer some superior characteristics compared to other switching devices. Increasing the breakdown voltage by connecting devices in series would make GaN-HEMTs one of the most promising candidates for high-voltage and high-frequency applications.

1.6 Research Objectives

The main research objectives of this dissertation is to develop new power electronic structures that can operate efficiently under wide range of voltage conversion ratios and are suitable for high-voltage and high power applications. In addition, the developed new architectures provide high power density, high specific power, and minimal EMI filtering requirement. Accordingly, the features of the proposed new topologies can be summarized in the following points:

1) Continuous input current im order to prolong the lifetime of the power source (i.e. battery, ultra-capacitor, fuel cell, etc.) connected to the converter.
2) Wide voltage conversion ratios to be able to operate at moderate duty cycle values, hence, have an acceptable efficiency throughout the broad range of voltage gain.
3) The potential difference between the grounds of the ports of the converters should be constant in order to minimize the leakage currents, hence, reduce the required periodic maintenance.

In order to understand the effect of the potential difference between the grounds of the power converter's ports on the operation, we need to depict the converter equivalent circuit including the parasitic capacitance between the grounds, as shown in Figure 1.11:

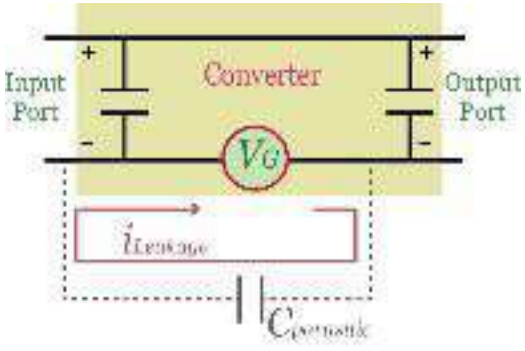


Figure 1.11: The generic equivalent circuit of a dc-dc converter including the parasitic capacitance between its grounds.

The parasitic capacitance ($C_{parasitic}$) depicted in Fig. J is usually caused by the package or casing of the power converter. The potential difference between the grounds of the input and output ports is depicted by (V_G) in Figure 1.11. When V_G is zero (= common ground) or a constant voltage, the leakage current $i_{Leakage} = 0$. When V_G is a high-frequency ac voltage, high leakage current will flow between the grounds through $C_{parasitic}$, as shown in Figure 1.11. Based on that, the major aspects of this dissertation are:

1) Develop new transformerless unidirectional dc-dc power converters with wide voltage gain range in order to suite fuel cell and renewable energy systems.
2) Develop new transformerless bidirectional dc-dc power converters with wide voltage gain range in order to suite electric vehicles and energy storage systems.
3) Design novel isolated high-frequency link dc-ac power converters with reduced switch count for medium-voltage supercharging stations for electric vehicles.
4) Developing high-voltage Gallium-Nitride (GaN) switching modules using series stacking, and using these modules in developing high voltage power electronic building blocks.

1.7 Original Contribution of This Thesis

The main contributions of this dissertation are the following:

1) Developing a new multilevel dc-dc converter that is based on a three-level flying-capacitor switching network and an LC^2D network. This converter has wide voltage gain, low voltage stress on the power switches, and a common ground between the

input and output ports. This converter is unidirectional, hence, it can be used in fuel cell and renewable energy applications.

2) Developing a new single-switch dc-dc converter with universal input voltage, high semiconductor utilization factor, and a common ground between its input and output ports. This converter integrates an $L^2C^3D^2$ with a boost converter to widen its gain range and reduce the voltage stress on its power switches. This converter is suitable for fuel cell and renewable energy applications.
3) Designing a novel single-switch dc-dc converter that is based on the SEPIC converter with an integrated dual-switched-capacitor network. This converter has broad voltage gain, low voltage stress on its passive and active devices, and a constant potential difference between its input and output ports. This converter is suitable for fuel cell and renewable energy applications.
4) Developing a new SEPIC based dc-dc converter that utilizes a discontinuous current quasi-Z-source network and a dual-switched-capacitor switching networks. The converter supports unidirectional power flow, thus, it suites the renewable energy and fuel cell systems.
5) Design and implementation of a new bidirectional buck-boost converter that has broad voltage gain range, as it supports the buck and boost operations in both power flow directions. This converter can be used in electric vehicles as an interface between the battery pack and the dc-link of the three-phase inverter.
6) Analysis and development of a novel bidirectional transformerless dc-dc converter with wide voltage conversion ratios, a common ground between the ports of the converter, and continuous current at the low voltage port. This converter is suitable for

energy storage systems that have wide voltage swings in their output voltage (i.e. ultra-capacitors).

7) Design and development of a new extendable bidirectional dc-dc converter with high voltage conversion ratios. This converter can directly interface the energy storage systems that have low output voltage to the load bus with voltage gain ≥20, without the need to any magnetic coupling components (i.e. coupled inductor or high-frequency transformer).
8) Development of high-voltage series-stacked GaN module and utilized it in a high-voltage power electronic building block.
9) Development of two new high-frequency ac link systems with reduced switch count. These two proposed dc/ac converters provide galvanic isolation and can be used for the electric vehicle's supercharging stations that are connected to the medium-voltage ac grid.

1.8 Dissertation Organization

Chapter 2 gives an overview and full literature review of the non-isolated unidirectional and bidirectional dc-dc converters in literature. In addition, it gives a thorough literature review of the isolated high-frequency ac-link dc-ac converters that can be used for medium-voltage applications.

In chapter 3, a three-level step-up converter that is based on a flying-capacitor switching network and an integrated LC^2D network is analyzed and proposed. Its voltage gain, voltage stress on the semiconductor devices, and the current stresses on its active and passive components are derived. In the end, the experimental results are given and compared with the theoretical analysis.

In chapter 4, a new single-switch unidirectional converter with universal input voltage is discussed for the application of electric vehicles with fuel cells. The current and voltage stresses on the power switches and diodes and analyzed. Additionally, the voltage gain of the converter and a comparative study with other step-up converters are given. The experimental verification and the conclusion are presented at the end of the chapter.

In chapter 5, a novel single-switch converter that integrates a SEPIC dc-dc converter with a dual-switched-capacitor network is discussed and analyzed. The electrical stresses on its active and passive components are mathematically derived and verified by the experimental results at the end of the chapter.

In chapter 6, a SEPIC-based dc-dc converter that utilizes a discontinuous current quasi-Z-source network and a switched-capacitor network for fuel cell vehicles is proposed and mathematically analyzed. The design of the passive and active components is given, and the electrical stresses on the power switch and diodes are discussed and experimentally verified.

In chapter 7, a new transformerless buck-boost dc-dc converter that can perform the buck and boost operations in both power flow directions is presented and analyzed. The design of the active and passive components and the electrical stresses on the power switches are given. At the end of this chapter, the experimental validation and the conclusion are presented.

In chapter 8, a novel non-isolated dc-dc bidirectional converter with wide voltage conversion ratios is presented and discussed for the application of energy storage systems. The selection of components and a comparative study with other bidirectional dc-dc converters are given, and the experimental validation is given at the end of the chapter.

In chapter 9, a new extendable bidirectional dc-dc converter that has high voltage conversion ratios is discussed. The mathematical analyses of its voltage gain and electrical stresses on its power switches are derived and verified by the experimental results.

In chapter 10, two cascaded high-frequency-ac-link converter for super charging stations' applications are discussed and analyzed. A novel current controller is discussed and the control strategy during grid faults is presented. Simulation results from MATLAB/SIMULINK software are given at the end of the chapter to verify the theoretical analyses.

In chapter 11, A two-level power electronic building block built with GaN high electron mobility transistors (HEMTs) and a Nanocrystalline inductor is discussed. The possible dc-dc, single-phase/three-phase dc-ac topologies are presented, and the isolated gate drivers are discussed. The experimental results are given at the end of the chapter.

In chapter 12, a high-voltage series-stacked GaN HEMT module for electric vehicle applications is discussed and analyzed. The comparative study with its Silicon and Silicon Carbide counterparts are presented. The LTspice simulation results and the experimental results at the end of the chapter are used to verify the theoretical analysis.

In chapter 13, a power electronic building block with series-stacked GaN modules is discussed. The possible dc-dc, single-phase/three-phase dc-ac converter topologies are analyzed and presented. Different applications are discussed at the end of the chapter.

In chapter 14, a conclusion of this dissertation and an insight on recommended future work are given.

Chapter 2 Power Electronic Building Blocks for Renewable, Electric Vehicle, and Energy Storage Applications: Literature Review

2.1 Introduction

The declining costs of sustainable energy systems and the global interest in reducing the CO_2 emissions and the reliance on fossil fuels, the electrification of the means of transportation has attracted a lot of interest [54],[55]. Electric vehicles (EVs) powered with fuel cells are important players in the clean energy vehicles segment as the fuel cell is a clean source of energy with zero emissions, also it has high output current density and high efficiency [16], [17]. Nevertheless, the fuel cell has soft output characteristics where its output voltage drops noticeably as the output current increases, hence, it cannot be used to directly feed the inverter of the EV. A step-up dc-dc converter has to be used as an interface between the fuel cell and the dc-link of the inverter, as shown in Figure 2.1, where the dc-dc converter solves the mismatch between the fuel cell voltage and dc-link voltage.

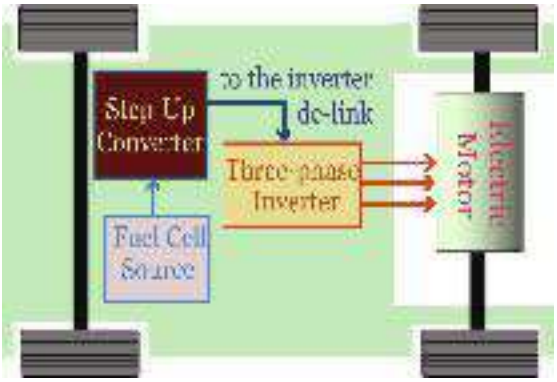


Figure 2.1: The typical powertrain of a fuel-cell powered electric vehicle.

Another approach to reduce the CO_2 emissions is by increasing the integration of renewable energy systems. The output voltage of the renewable energy source changes based on the environmental conditions and the operating load point (can be varied using a MPPT). Figure

2.2 shows a photovoltaic system connected to the grid via a dc-dc converter followed by a power inverter. A dc-dc converter with wide voltage gain range is needed to solve the mismatch in voltage levels between the renewable energy source and the dc-link bus of the inverter.

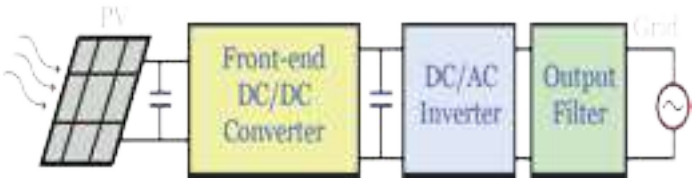


Figure 2.2: The typical architecture of a grid-connected PV system.

Due to the increasing demand of energy, and environmental concerns associated with electrical energy generation from fossil fuels, the development of microgrids integrating renewable energy sources has attracted major interest. The increasing penetration of these intermittent renewable energy systems can impose disturbances to the power grid. This requires integration of energy storage units (ESUs) to smoothen the fluctuations in power generation by maintaining the balance between renewable power generation and consumption.

The generic architecture of a dc microgrid with renewable energy generation and assisted by ESUs is shown in Figure 2.3. The renewable sources are connected to the dc bus of the microgrid via unidirectional power electronic converters, while the ESU is decoupled from the dc bus by a bidirectional dc-dc converter. This bidirectional dc-dc converter allows the ESU to absorb the excessive energy when the power generation exceeds the demand, and release energy when the demand exceeds generation.

Additionally, the EV powertrain is another version of microgrids, where the bidirectional dc-dc converter pushes power from the ESU to the dc-link of the three-phase inverter in the motoring mode, and absorbs power from the dc-link back to the ESU in the regenerative braking mode.

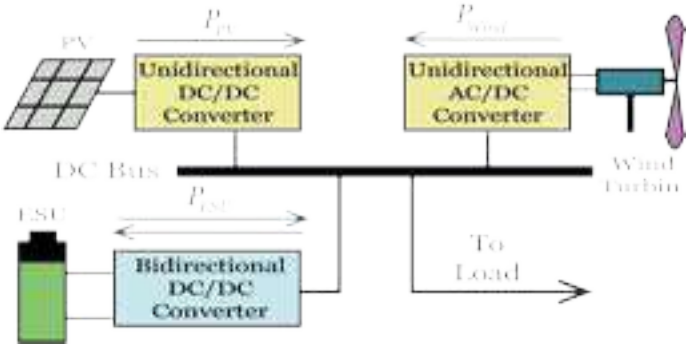


Figure 2.3: The typical architecture of a dc microgrid supported with renewable energy sources and energy storage units.

Figure 2.4 shows the typical architecture of the powertrain of an electric vehicle. The ESU is connected to the dc-link bus of the three-phase inverter via a bidirectional dc-dc converter.

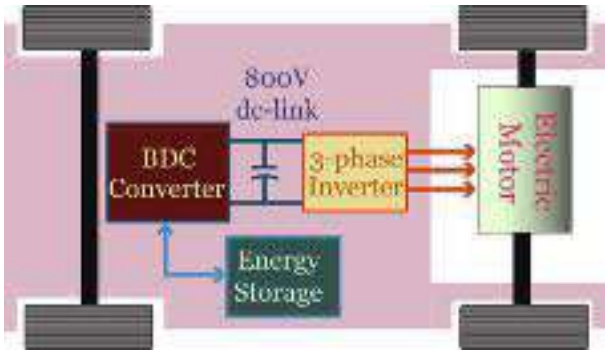


Figure 2.4: The typical architecture of an EV powered by energy storage units.

2.2 Non-Isolated Unidirectional Conventional DC-DC Structures

Non-isolated unidirectional dc-dc converters process the power in one power flow direction. It has many applications such as in renewable energy systems, fuel cell systems, and consumer electronics. In this subsection, we cover the two-level unidirectional conventional dc-dc converter, the multilevel unidirectional dc-dc converters, switched-capacitor unidirectional dc-dc converters, switched inductor unidirectional dc-dc converters, and quadratic unidirectional dc-dc converters.

2.2.1 Two-Level Unidirectional Conventional DC-DC Converter

The topology of this converter is shown in Figure 2.5, as it is composed of one switch, one diode, one capacitor, and one inductor. This converter is very popular for step-up due to its simple structure, having a common ground between its input and output ports, having a continuous input current, and simple gate driving. Nevertheless, this converter cannot be used for applications that require high step-up conversion ratios (> 5), due to the existence of parasitic components in its passive and active components. Additionally, at high step-up voltage gains the efficiency of this converter deteriorates noticeably due to the high voltage and current stresses on its semiconductor devices.

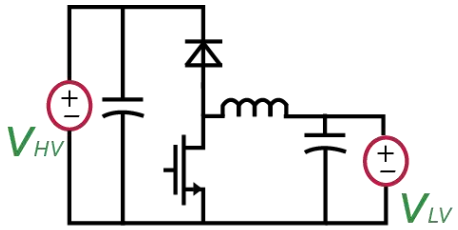


Figure 2.5: The two-level unidirectional conventional dc-dc converter.

2.2.2 Multilevel Unidirectional DC-DC Converters

The multilevel dc-dc converter topologies aim to reduce the voltage stresses on the semiconductor devices of the dc-dc converter, hence, power switches and diodes with lower rated voltage can be utilized which yields better efficiency compared to the two-level converter [56]-[80]. Another advantage is that the frequency of the ripple current of the input inductor increases as the number of levels increases, which results in more compact dc-dc converters with smaller and lighter power inductors.

The three-level boost (TLB) converter is one of the most commonly adopted multilevel dc-dc converters due to the low number of passive and active components compared to the other multilevel dc-dc converter. Its unidirectional version is shown in Figure 2.6, as it is composed

of two switches, two diodes, one inductor, and two capacitors. The voltage stress on its switches and diodes equal half of its output voltage. The voltage gain of this converter is similar to that of the two-level converter, which means it is not suitable for high step-up applications. Additionally, it lacks a common ground between its input and output ports which result in higher electromagnetic interference (EMI) noise and requires more filtering.

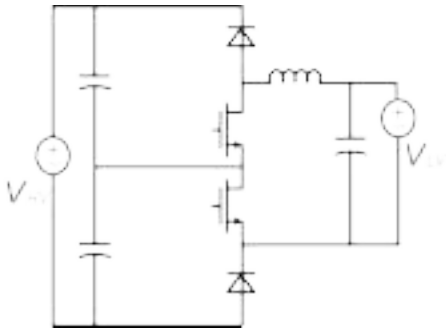


Figure 2.6: The three-level unidirectional conventional dc-dc converter.

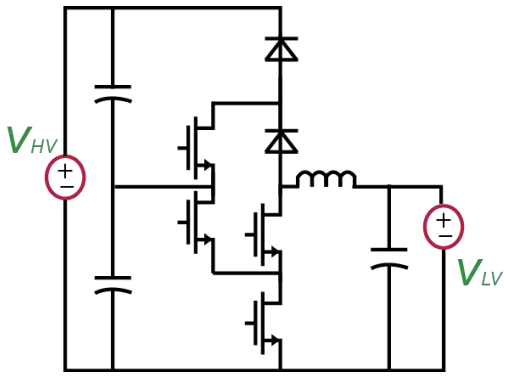


Figure 2.7: A unidirectional neutral-point-clamped dc-dc converter.

The neutral point clamped converter is another popular multilevel dc-dc converter, as it also reduces the voltage stresses on the semiconductor devices and diminishes the size of the input inductor. It has a common ground between its input and output ports and has a continuous input current. The circuit structure of this converter is given in Figure 2.7.

The voltage gain of this converter is similar to that of the two-level converter, which means it is not suitable for high step-up applications. Additionally, it requires a higher number of power switches compared to the other multilevel dc-dc converters.

The flying-capacitor converter is another attractive step-up multilevel dc-dc converter, as it also reduces the voltage stresses on the semiconductor devices and reduces the size of the input inductor. It has a common ground between its input and output ports and has a continuous input current. The circuit structure of this converter is given in Figure 2.8.

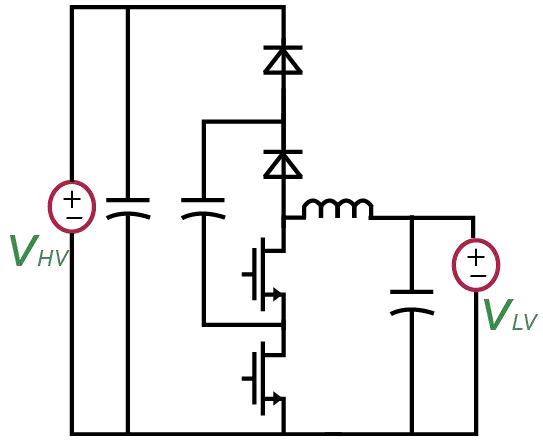


Figure 2.8: A unidirectional flying-capacitor dc-dc converter.

The voltage gain of this converter is similar to that of the two-level converter, which means it is not suitable for high step-up applications. Additionally, it requires a higher number of capacitors compared to the other multilevel dc-dc converters.

2.2.3 Switched- Capacitor Unidirectional DC-DC Converters

The switched-capacitor dc-dc converter is an attractive way to step-up the voltage using a charge pump circuit which is adopted in a lot of converters. The voltage level stepping-up using the charge pump circuit takes place from the transfer of capacitive energy and does not require any magnetic components. The switches capacitor converters are very popular

topologies as they have a modular structure, thus, their voltage gain can be systematically enhanced by increasing the number of switched capacitor cells [81]-[107].

One of the major drawbacks of the switched-capacitor topologies is the high inrush current during the start instant, which may affect the efficiency, the power density, and the specific power of the dc-dc converter. One of the ways to reduce the high inrush currents in the switched-capacitor converters is by putting an inductor at the output port to construct a buck converter in the already existing power switch(es). This way provides efficient voltage regulation and reduces the inrush currents, which is known as soft charging switched-capacitor converter.

Figure 2.9 a unidirectional switched-capacitor dc–dc converter with the common features of the switched-capacitor converters such as compact size and low weight. This converter has a continuous input current.

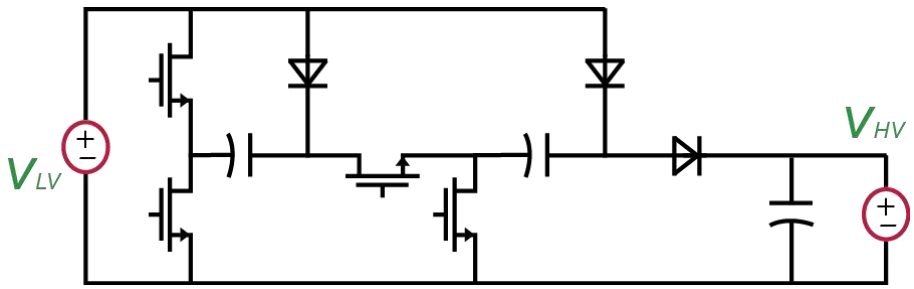


Figure 2.9: A unidirectional switched-capacitor dc-dc converter with diode-capacitor multipliers.

Another switched-capacitor dc–dc converter with a resonant operation is presented in Figure 2.10. In this converter, a resonant small inductor is utilized in the first stage to realize zero-current switching. Accordingly, the inrush that usually takes place in conventional switched-capacitor converters can be minimized.

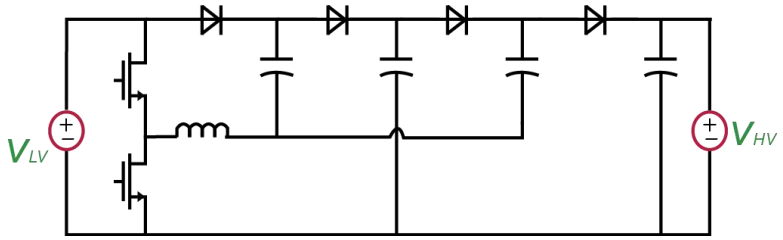


Figure 2.10: A unidirectional switched-capacitor dc-dc converter with diode-capacitor multipliers and a small resonant inductor.

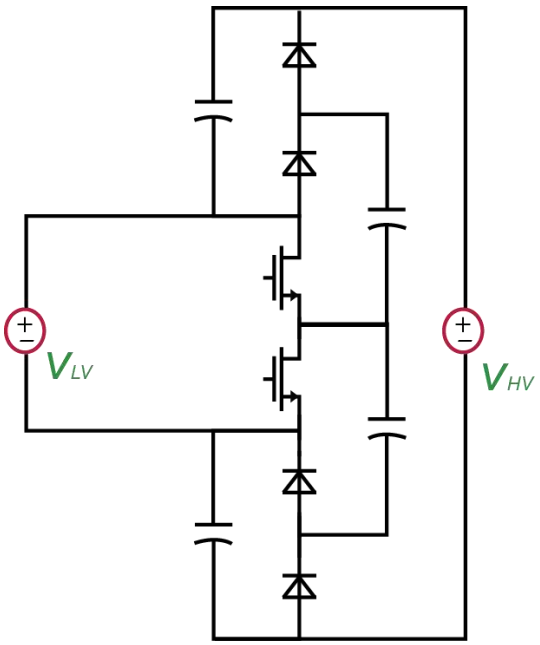


Figure 2.11: A modular asymmetrical switched-capacitor dc-dc converter.

Figure 2.11 presents a modular asymmetrical switched-capacitor dc–dc converter with a shared capacitor voltage rating. Due to the modularity feature of its circuit, this topology is capable of realizing high voltage conversion ratios and needs output capacitors with low capacitance and low voltage rating. This converter utilizes only two power switches. The voltage gain of this converter can be simply extended by increasing the number switched capacitor cells. In addition, the control of this topology is simple and voltage stress on the semiconductor devices is low.

Voltage multiplier circuits are attracting a lot of attention in the applications that require high step-up voltage conversion ratios as they have a simple circuit structure. Figures 2-12 to 2-18 present some of the important structures known as voltage multiplier cell dc–dc converters. Some of these architectures have only diodes and capacitors (as in Figure 2-12, Figure 2-13, and Figure 2-14) and thus they are called in the literature as diode-capacitor voltage multiplier cell dc-dc converters. Other voltage multiplier cell dc-dc converters have more active components, such as an auxiliary power switch (Figure 2-15), while other voltage multiplier cell dc-dc converters utilize inductors to enhance the step-up voltage gain (Figure 2-16 and Figure 2-17). Some topologies of the voltage multiplier cell dc-dc converters with vertical structures have been introduced, as the topology shown in Figure 2-13.

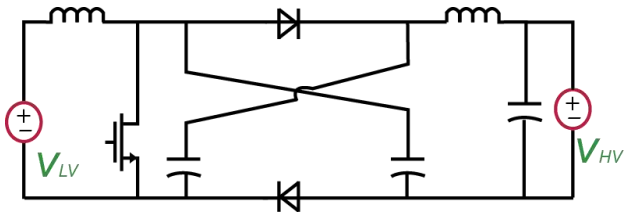


Figure 2.12: Unidirectional voltage multiplier cell dc-dc converter 1.

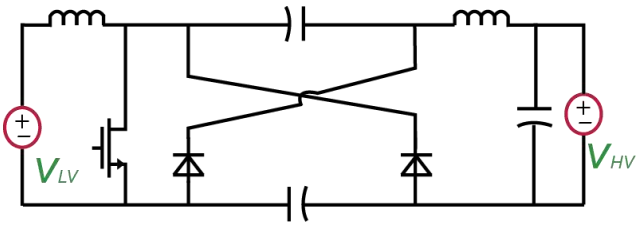


Figure 2.13: Unidirectional voltage multiplier cell dc-dc converter 2.

The operation and dynamic performance of the voltage multiplier cell converters presented in Figure 2-12, Figure 2-13, and Figure2-14 are identical and their voltage gain relationships are similar: (1+ D)/(1 - D), as D is the duty cycle of the main switch. When a small inductor (typically between 1 to 4 μH) is used in the voltage multiplier cell dc-dc converters in Figure

2-14, a zero current switching (ZCS) transition can be be realized for the diodes and switch, which can noticeably improve the efficiency of the converter by reducing the switching losses.

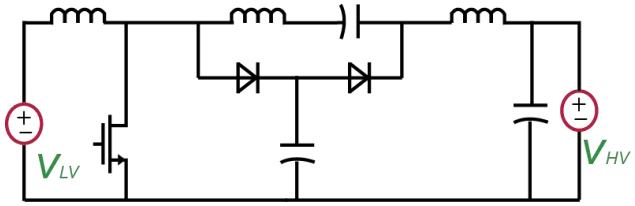


Figure 2.14: Unidirectional voltage multiplier cell dc-dc converter 3.

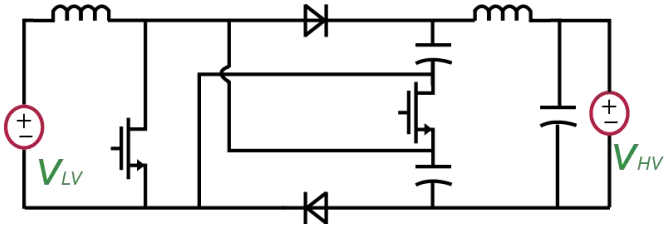


Figure 2.15: Unidirectional voltage multiplier cell dc-dc converter 4.

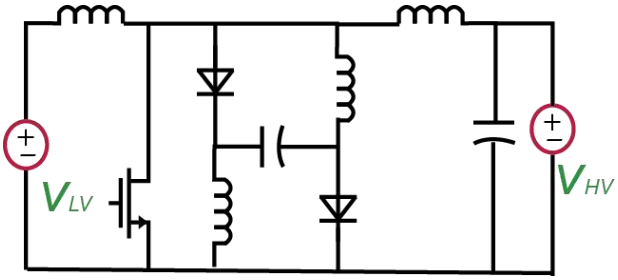


Figure 2.16: Unidirectional voltage multiplier cell dc-dc converter 5.

The voltage multiplier cell dc-dc converter in Figure 2-16 utilizes an inductor and a capacitor in order to enhance the voltage conversion ratio of the dc-dc converter. The voltage multiplier cell dc-dc converter in Figure 2-17 has the highest voltage gain compared to the other voltage multiplier cell dc-dc converters, nevertheless, the voltage stress on its switch is high.

In the voltage multiplier cell converter in Figure 2-14, a single inductor connected in first stage is capable of realizing the zero current switching on all the semiconductor devices.

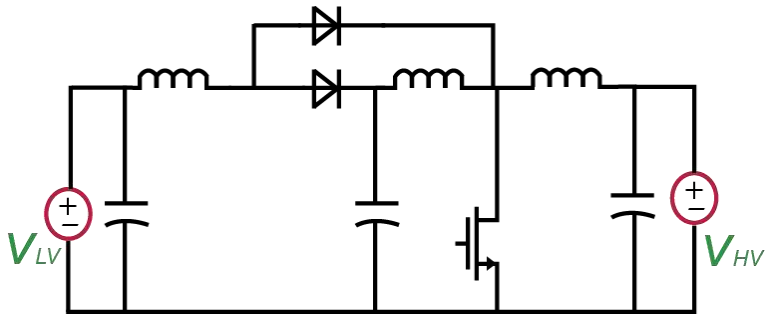


Figure 2.17: Unidirectional voltage multiplier cell dc-dc converter 6.

2.2.4 Switched-Inductor Unidirectional DC-DC Converters

The Voltage Lift structure is an alternative useful technique that is widely utilizes in dc–dc converters to enhance voltage conversion ratio. This method is based on charging a capacitor to a specific voltage level (e.g., voltage of the input port) and then boosting the output voltage (stepping-up the voltage) with the level of voltage of the charged capacitor [108]-[119]. When repeating this method with the insertion of other capacitors to form a re-lift, triple-lift, and quadruple-lift topologies, the level of the output voltage can be enhanced. A lot of boost dc–dc topologies have been proposed by Luo, and the voltage lift approach has been utilized in the literature in a large number of dc-dc converters, like Ćuk, SEPIC, and Zeta topologies.

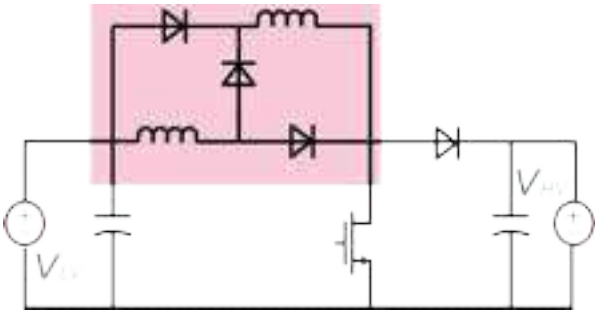


Figure 2.18: Unidirectional voltage Lift cell dc-dc converter 1.

In order to enhance the voltage gain of the dc-dc converter, more the one lift circuits can be cascaded. Voltage Lift Switched Inductor dc-dc converters are presented in Figure 2-18, Figure 2-19, and Figure 2-20.

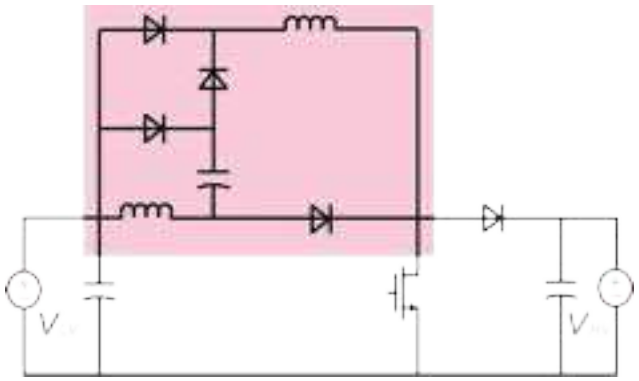


Figure 2.19: Unidirectional voltage Lift cell dc-dc converter 2.

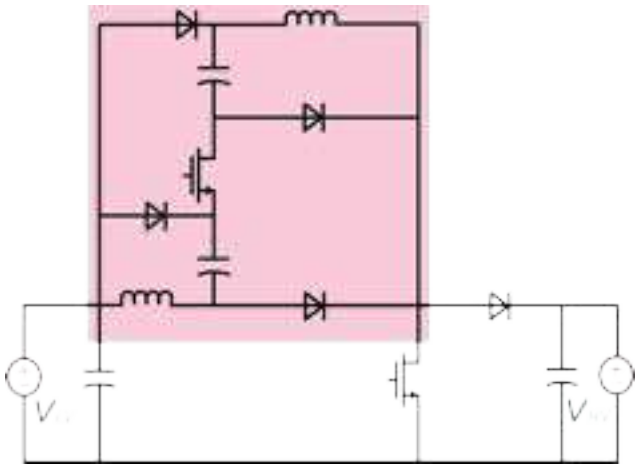


Figure 2.20: Unidirectional voltage Lift cell dc-dc converter 3.

The basic switched-inductor dc-dc converter is shown in Figure 2-18. In switched-inductor dc-dc converter, the inductors are charged in parallel and discharged in series. Where the two inductors have similar inductances and have the same conditions of operation, they can be coupled into one core in to diminish the size and reduce the weight of the dc-dc converter.

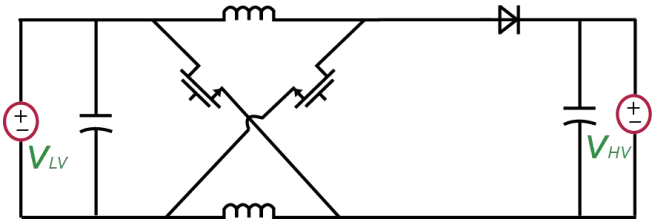


Figure 2.21: Unidirectional active-switched-inductor dc-dc converter 1.

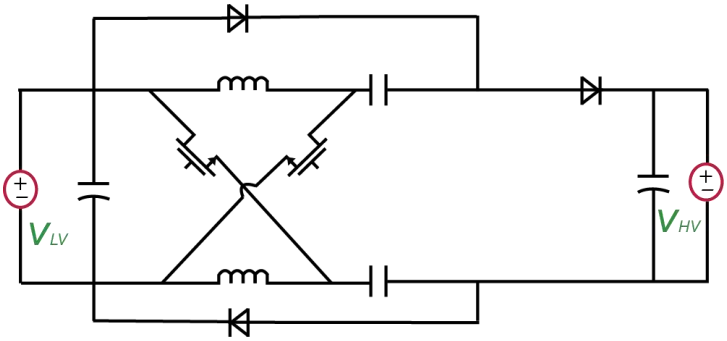


Figure 2.22: Unidirectional active-switched-inductor dc-dc converter 2.

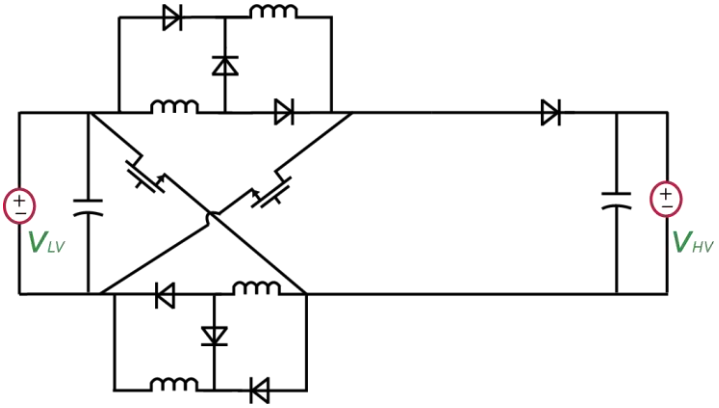


Figure 2.23: Unidirectional active-switched-inductor dc-dc converter 3.

Implementing a voltage lift structure with elementary cell in a switched-inductor dc-dc converter results in a self-lift switched-inductor dc-dc converter, as shown in Figure 2-19. When an additional diode and capacitor are added to a self-lift switched-inductor dc-dc

converter, a double self-lift switched-inductor dc-dc converter is produced, as shown in Figure 2-20. Other high order switched-inductor dc-dc converters that can achieve high step-up gain have been discussed in literature.

As an alternative structure to that with three diodes, as in the basic voltage Lift cell dc-dc converter 1 in Figure 2-18, only two power switches are used in what so-called active switched-inductor network and there is no need for an additional power switch in the power converter circuit. A number of unidirectional active-switched-inductor dc-dc converters are shown in Figure 2-21, Figure 2-22, and Figure 2-23.

2.2.5 Quadratic Unidirectional DC-DC Converters

Figure 2.24 depicts a cascaded unidirectional boost converter that consists of two consecutive boost converters. The voltage stress on the first boost dc-dc converter is relatively low, thus, its operating frequency can be high which can result in high power density. Nevertheless, the second boost dc-dc converter has to operate at low frequency in order to decrease the switching losses. The quadratic converter aims to reduce the number of power switches and reduce the complexity of the converter structure and the gate driving circuits [120]-[137]. Nevertheless, one major disadvantage of the quadratic boost dc-dc converters is that the duty cycles of the two boost converters can no longer be controlled independently, unlike the cascaded boost structure in Figure 2.24. The structure of a quadratic boost dc-dc converter is presented in Figure 2.25. Figure 2.26 depicts a three-level quadratic boost dc–dc converter that was proposed for high step-up applications. Other basic quadratic boost dc-dc converter topologies are presented in Figure 2.27 to Figure 2.30. The quadratic boost dc-dc converters have wider ranges of voltage conversion ratios than the conventional PWM boost dc–dc converter.

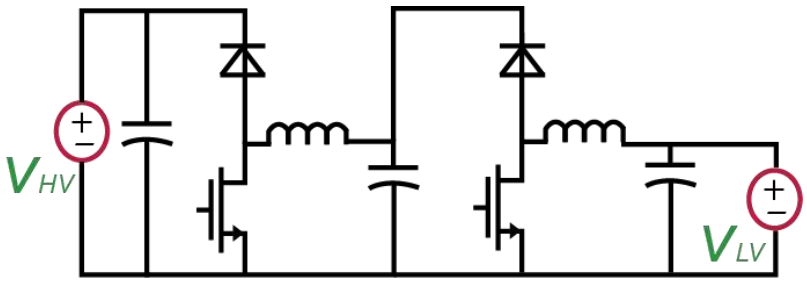


Figure 2.24: Cascaded unidirectional boost dc-dc converters.

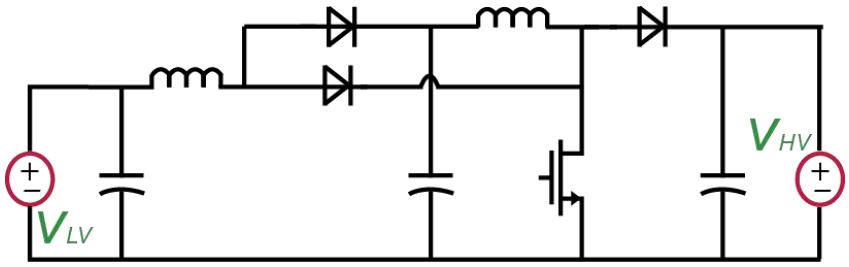


Figure 2.25: The basic unidirectional quadratic boost dc-dc converter.

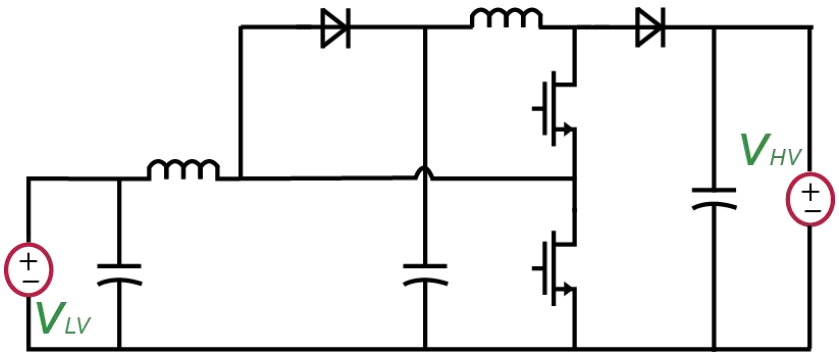


Figure 2.26: Three-level unidirectional quadratic boost dc-dc converter.

For the applications where the voltage conversion ratio is limited, the quadratic boost dc-dc converters can work with narrower changes in the values of duty cycle than that in the conventional boost dc–dc converters, which results in a simple design procedure and an improved performance.

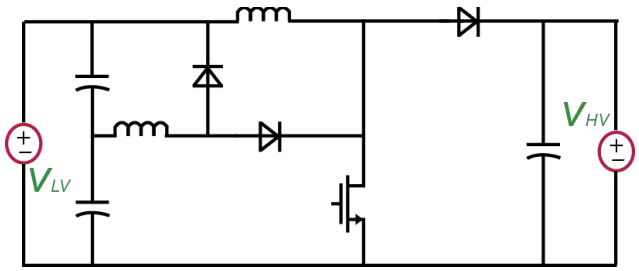


Figure 2.27: A quadratic boost dc-dc converter with low capacitor voltage.

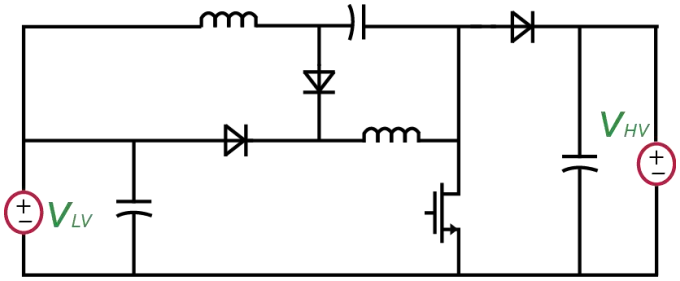


Figure 2.28: Basic quadratic boost dc-dc converter 1.

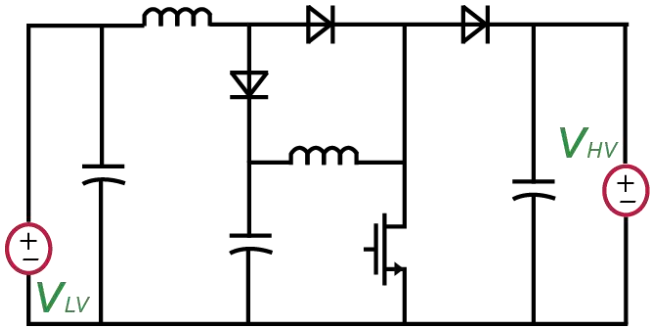


Figure 2.29: Basic quadratic boost dc-dc converter 2.

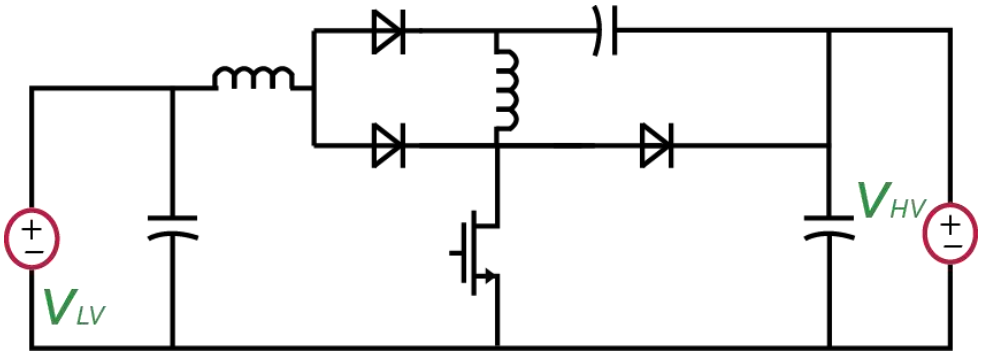


Figure 2.30: Basic quadratic boost dc-dc converter 3.

Added to that, the quadratic boost dc-dc converters have several advantages for low power applications as they avoid sophisticated magnetic designs. Figure 2.27 presents a quadratic boost dc-dc converter with low voltage stress on its capacitor. In Figure 2.28 and Figure 2.29, two topologies of quadratic boost dc-dc converters with similar components but only differ in terms of the placement of the buffer capacitor. A lot of modified versions of the quadratic boost dc-dc converter have been proposed and discussed in literature. Generally, cascaded and quadratic boost dc-dc converters, such as those in Figure 2.24 to Figure 2.30, usually have four semiconductor devices, with at least one of them is an active power switch. They usually also contain a one inductor and one capacitor for each stage of the dc-dc converter.

2.3 Non-Isolated Bidirectional DC-DC Converters

Non-isolated bidirectional dc-dc converters process the power in both power flow directions (from the high voltage port to the low voltage port in the step-down mode, and from the low voltage port to the high voltage port in the step-up mode). It has many applications such as in energy storage systems, battery-powered electric vehicles, and uninterruptible power supplies. In this subsection, we cover the two-level bidirectional conventional dc-dc converter, the multilevel bidirectional dc-dc converters, switched-capacitor bidirectional dc-

dc converters, switched inductor bidirectional dc-dc converters, and quadratic bidirectional dc-dc converters.

2.3.1 Two-Level Bidirectional Conventional DC-DC Converter

The topology of this converter is shown in Figure 2.31, as it is composed of two switches that work in a complementary fashion, two capacitors, and one inductor. This converter is very popular for bidirectional buck/boost applications due to its simple structure, having a common ground between its input and output ports, having a continuous current at the low voltage port, and simple gate driving. Nevertheless, this converter cannot be used for applications that require high voltage conversion ratios, due to the existence of parasitic components in its passive and active components. Additionally, at high voltage conversion ratios the efficiency of this converter deteriorates noticeably due to the high voltage and current stresses on its semiconductor devices.

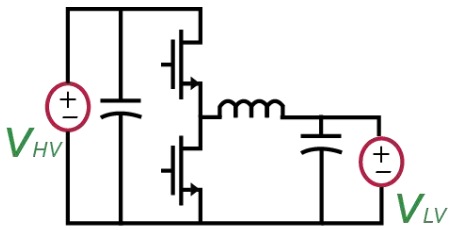


Figure 2.31: The two-level Bidirectional conventional dc-dc converter.

2.3.2 Multilevel Bidirectional DC-DC Converters

The multilevel bidirectional dc-dc converter topologies aim to reduce the voltage stresses on the power switches of the dc-dc converter and reduce the size of the magnetic components. The bidirectional versions of the three-level bidirectional converter, the neutral point clamped converters are shown in Figure 2.32.

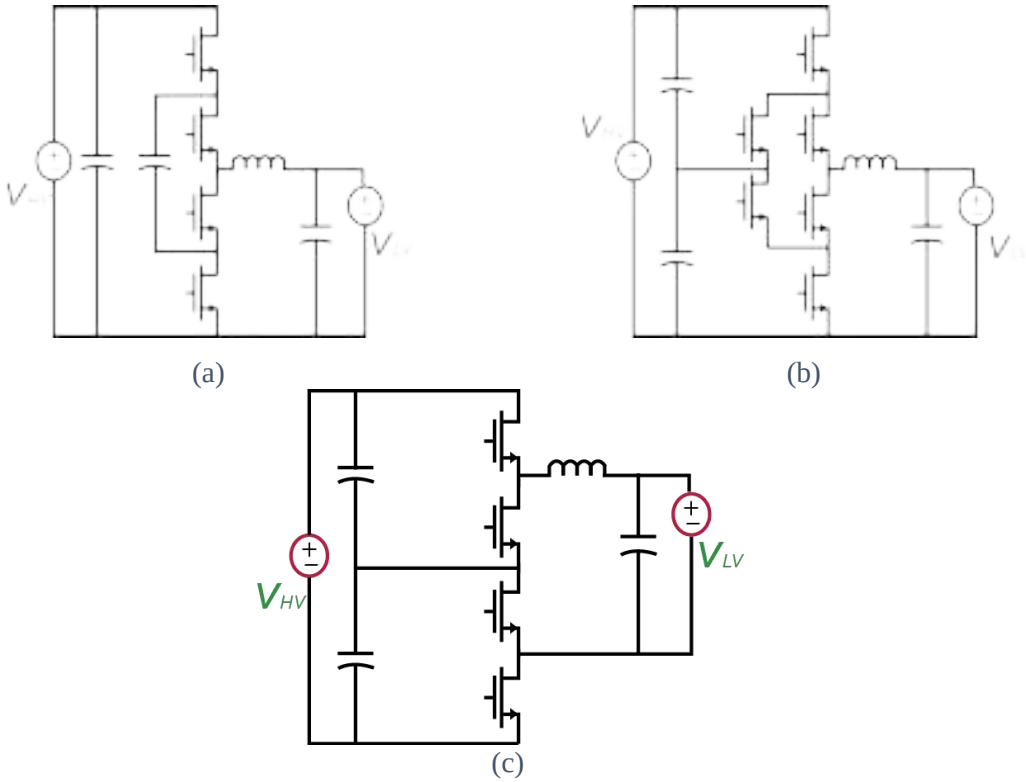
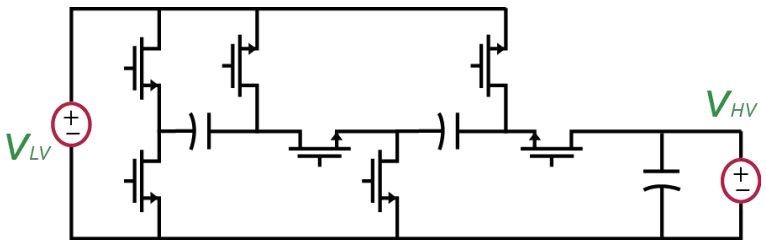


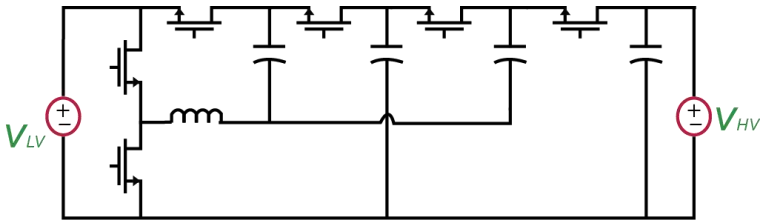
Figure 2.32: The bidirectional versions of (a) The flying capacitor converter. (b) The neutral point clamped converter. (c) The three-level converter.

2.3.3 Switched- Capacitor Bidirectional DC-DC Converters

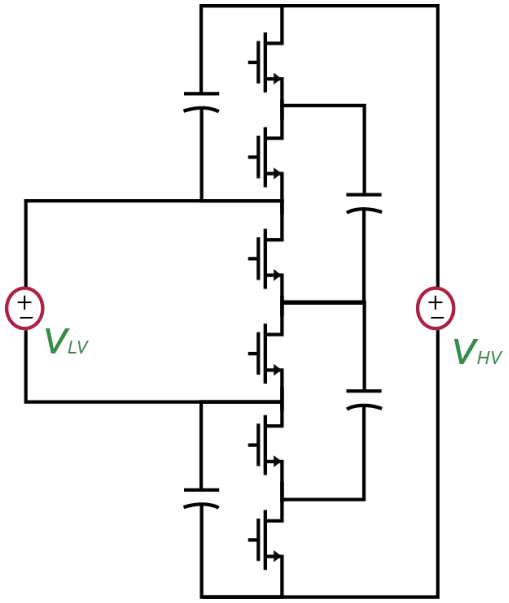
The switched-capacitor bidirectional dc-dc converters have the same operational concepts as those unidirectional ones discussed in subsection 2.2.3. The bidirectional versions of these converters can be directly derived by replacing the diodes with power switches, as shown in Figure 2.33, in order to allow power flow in both directions.



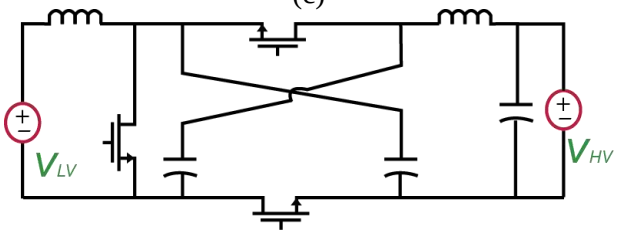
(a)



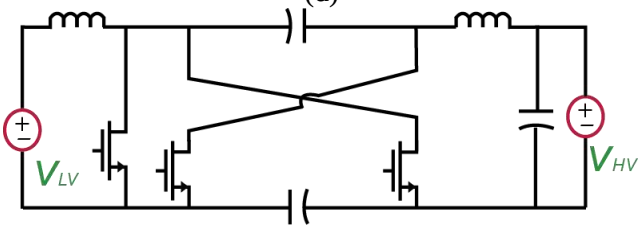
(b)



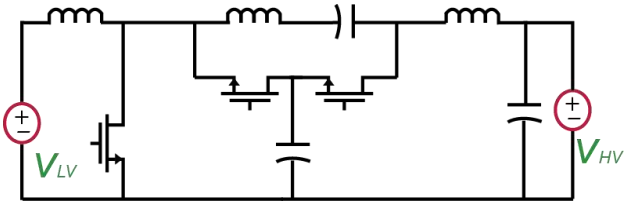
(c)



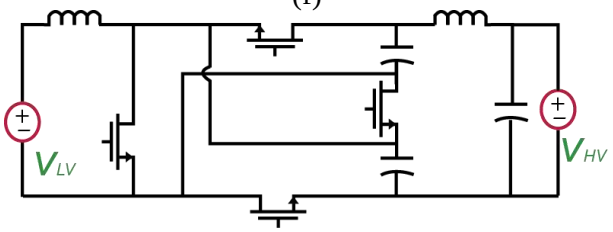
(d)



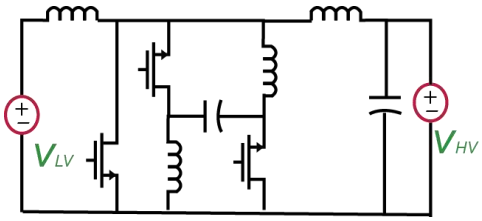
(e)



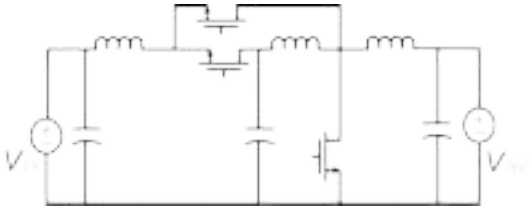
(f)



(g)



(h)

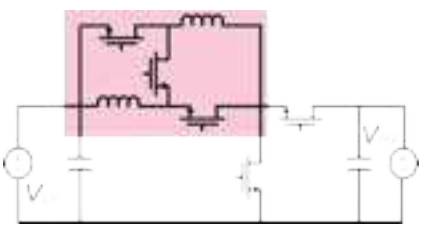


(i)

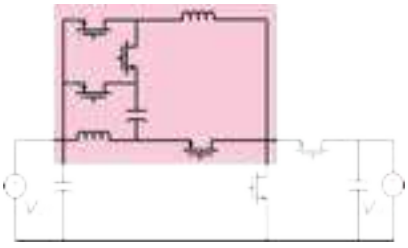
Figure 2.33: The bidirectional versions of the switched-capacitor converters discussed in subsection 2.2.3.

2.3.4 Switched- Inductor Bidirectional DC-DC Converters

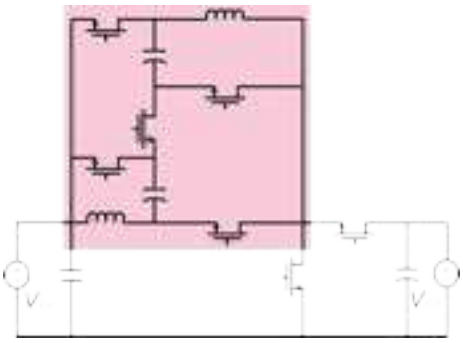
The switched-inductor bidirectional dc-dc converters have the same operational concepts as those unidirectional ones discussed in subsection 2.2.4. The bidirectional versions of these converters can be directly derived by replacing the diodes with power switches, as shown in Figure 2.34, in order to allow power flow in both directions.



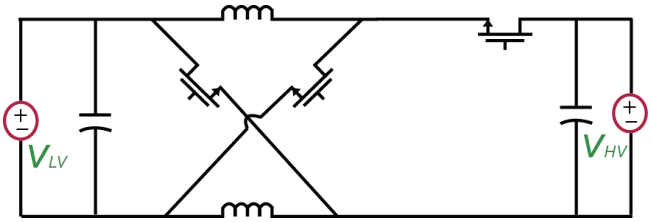
(a)



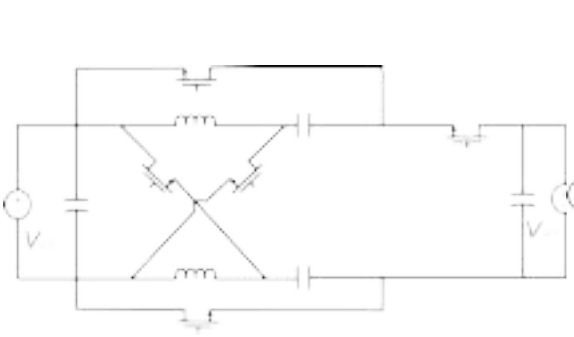
(b)



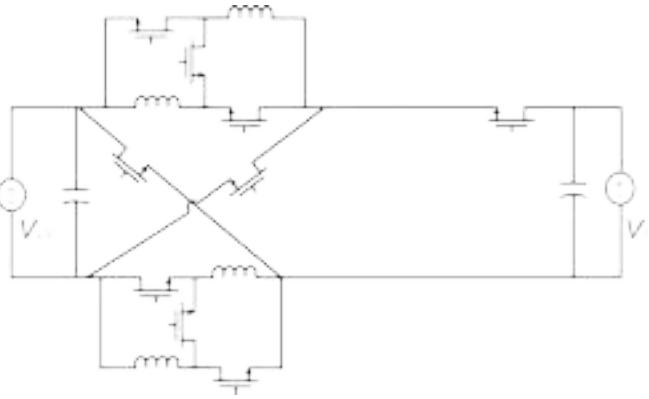
(c)



(d)



(e)

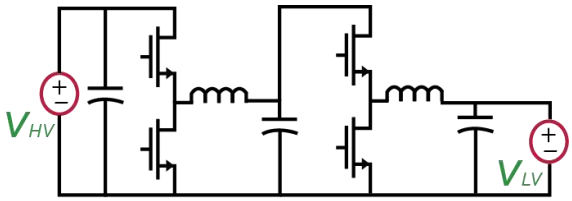


(f)

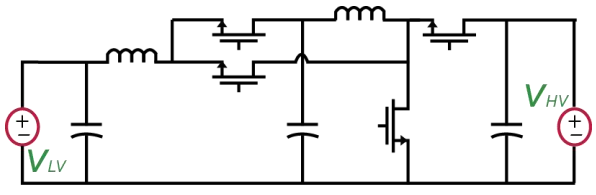
Figure 2.34: The bidirectional versions of the switched-inductor converters discussed in subsection 2.2.4.

2.3.5 Quadratic Bidirectional DC-DC Converters

The quadratic bidirectional dc-dc converters have the same operational concepts as those unidirectional ones discussed in subsection 2.2.5. The bidirectional versions of these converters can be directly derived by replacing the diodes with power switches, as shown in Figure 2.35, in order to allow power flow in both directions.



(a)



(b)

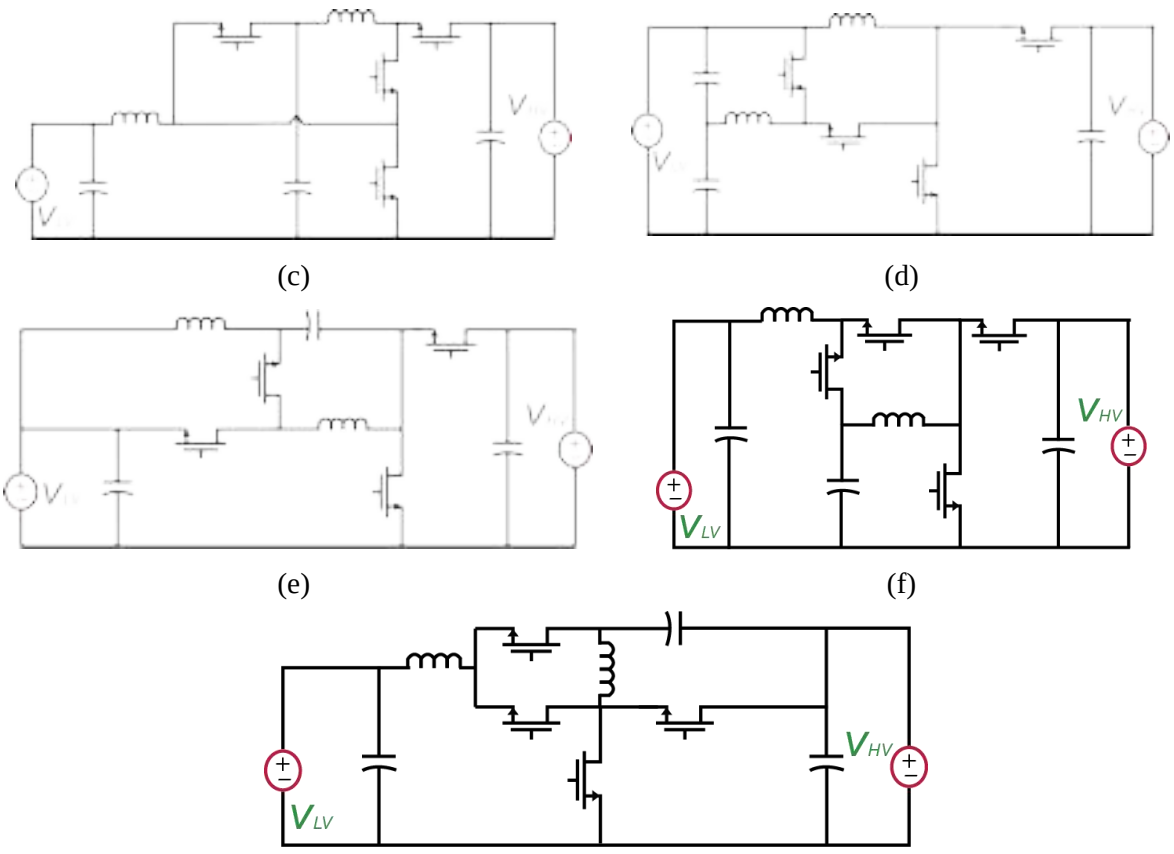
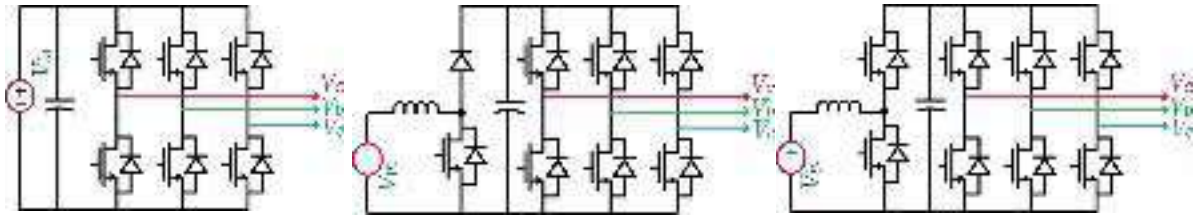


Figure 2.35: The bidirectional versions of the quadratic converters discussed in subsection 2.2.5.

2.4 Non-Isolated DC-AC Structures

The six-step buck VSI, shown in Figure 2.36, is the most commonly utilized three-phase inverter; it is composed of three legs in push-pull configuration. A common-mode voltage has to be added to the output of each leg. In this three-phase buck VSI, there are six switches operating at high frequency.

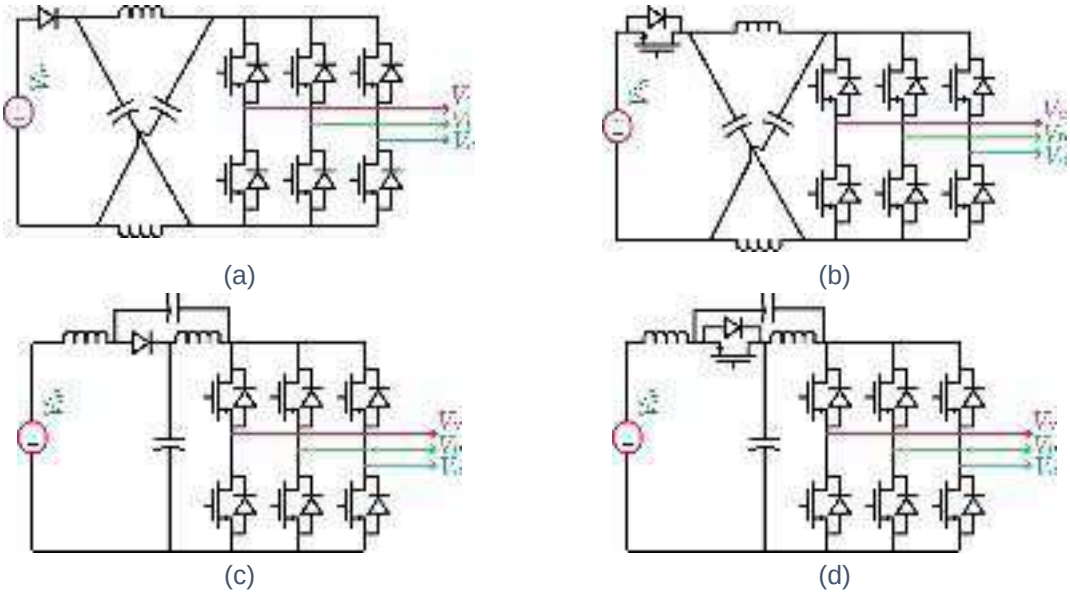
A boost stage can be added before the three-phase buck VSI to increase the voltage level of the dc supply (V_{in}). This boost converter can be unidirectional, as in Figure 2.36 (b), or bidirectional, as in Figure 2.36 (c). For systems shown in Figure 2.36 (b) and Figure 2.36 (c) there are at least seven switches operating at high frequency.



(a) (b) (c)

Figure 2.36: Three-phase voltage source inverter, (a) for Buck operation only, (b) With a unidirectional boost converter. (c) With a bidirectional boost converter.

The Z-source inverter (ZSI) is a single-stage buck-boost inverter, where the dc supply voltage level can be pushed up without the need to a separate boost converter. The first versions of the ZSI are shown in Figure 2.37 (a) and Figure 2.37 (b), as Figure 2.37 (a) shows the unidirectional version and Figure 2.37 (b) shows the bidirectional version.



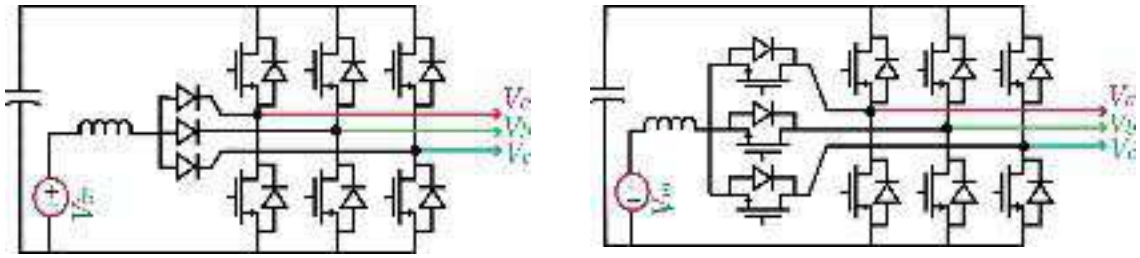
(a) (b) (c) (d)

Figure 2.37: (a) Unidirectional ZSI, (b) Bidirectional ZSI, (c) Unidirectional qZSI, (d) Bidirectional qZSI.

The quasi ZSI (qZSI) is the improved version of the ZSI as it has a smooth input current, making it suitable for renewable energy and energy storage systems. The unidirectional version of the qZSI is presented in Figure 2.37 (c) and the bidirectional version is shown in

Figure 2.37 (d). Both of ZSI and qZSI have six switches operating at high frequency. A lot of literature have covered different structures of the ZSI and qZSI [138]-[162].

The split-source inverter (SSI) is an alternative to the ZSI and qZSI [163]-[166], where the dc supply voltage can be stepped up without the need to a separate boost converter. The SSI has six switches operating at high frequency (note: the other three switches, in the bidirectional version, operate at low frequency). The unidirectional version of the SSI is depicted in Figure 2.38 (a), and the bidirectional version of the SSI is depicted in Figure 2.38 (b).



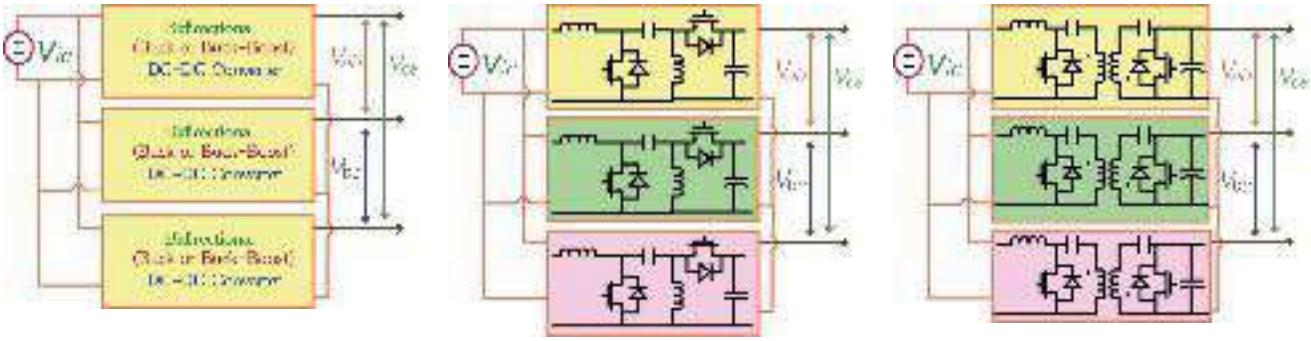
(a) (b)

Figure 2.38: (a) Unidirectional SSI, (b) Bidirectional SSI.

The basic construction of the (differential-mode inverter) DMI is three bidirectional buck or buck-boost dc-dc converters connected in such a way that all of them have a common ground, as shown in Figure 2.39 (a) [167]-[175]. Each converter generates an "ac voltage component" with a dc offset, such that the sum is either in the positive or negative voltage plane. Many dc-dc converters can be used to synthesize the DMI, like: Sepic, Ćuk, buck-boost, ….., etc. The least number of switches operating at high frequency for a three-phase DMI is six switches.

Two examples of the three-phase DMI are shown in Figure 2.39 (b) and Figure 2.39 (c). In Figure 2.39 (b), a DMI is synthesized with three bidirectional non-isolated Ćuk converters,

while Figure 2.39 (c) shows a DMI that is synthesized with three bidirectional isolated Ćuk converters.



(a) (b) (c)

Figure 2.39: (a) Generic DMI connection diagram, (b) Non-isolated Ćuk DMI, (c) Isolated Ćuk DMI.

2.5 Isolated DC-AC Structures

The isolated dc-ac inverter systems have many applications such as in renewable energy systems where they step-up the voltage level of the renewable energy source (by means of the turns ratio of the magnetic coupling component), and they minimize the leakage currents. Added to that, the galvanic isolation between the dc-source and the ac load provides inherent protection to the renewable energy sources against faults in the power grid.

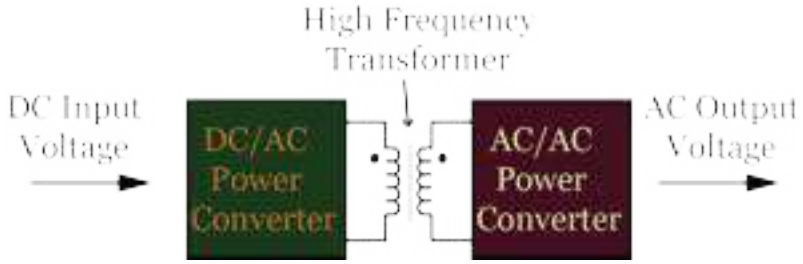


Figure 2.40: The generic structure of an isolated dc-ac inverter.

The differential-mode inverter that is shown in Figure 2.39 (c) is an example of isolated dc-ac structures. Nevertheless, the most common architecture of the isolated dc-ac structures is given in Figure 2.40

As depicted in Figure 2.40, this type of isolated dc-ac inverters is composed on a dc-ac stage to convert the input dc voltage to high frequency ac voltage to drive the high frequency transformer. An ac-ac power stage follows the high frequency transformer in order to convert the high frequency ac voltage from the transformer to an ac voltage with the low nominal frequency required by the ac load. Typically this kind of isolated inverters is categorized based on the structure of their ac-ac stage to either high frequency dc-link converters or high frequency ac-link converters.

2.5.1 High-Frequency DC-Link Converter

The typical topology of this converter is shown in Figure 2.41, as it is composed of a single-phase dc-ac inverter to convert the input dc voltage to high frequency ac voltage to drive the high frequency transformer, a single-phase rectifier to convert the high-frequency ac voltage from the transformer's secondary to dc voltage, and finally an inverter to convert this dc voltage to ac voltage with the voltage magnitude and frequency required by the ac load. This converter has a simple circuit structure and simple control. Nevertheless, the dc-link capacitor following the ac-dc rectifier reduces the power density of the converter and affects its reliability.

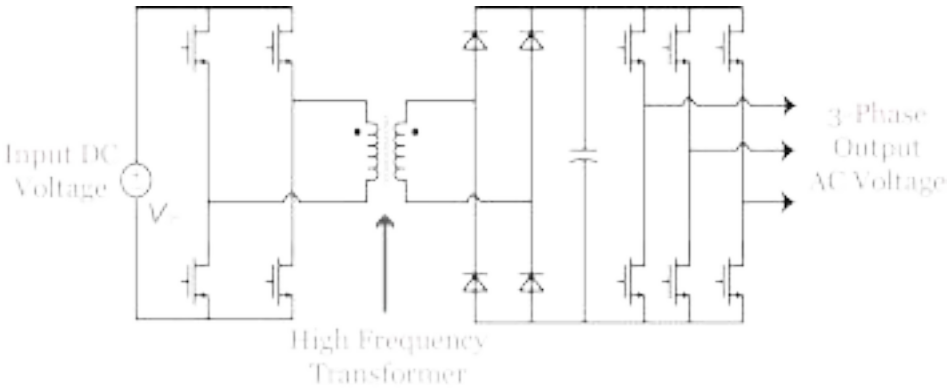


Figure 2.41: The topology of the high-frequency dc-link dc-ac inverter.

2.5.2 High-Frequency AC-Link Converter

The typical topology of this converter is shown in Figure 2.42, as it is composed of a single-phase dc-ac inverter to convert the input dc voltage to high frequency ac voltage to drive the high frequency transformer, a matrix converter to directly convert the high-frequency ac voltage from the transformer's secondary to ac voltage with the voltage magnitude and frequency required by the ac load. This converter eliminates the need for dc-link capacitors, thus its power density and reliability are better compared to the high-frequency dc-link converter. Nevertheless, the circuit structure and the required gate drivers are relatively more complex.

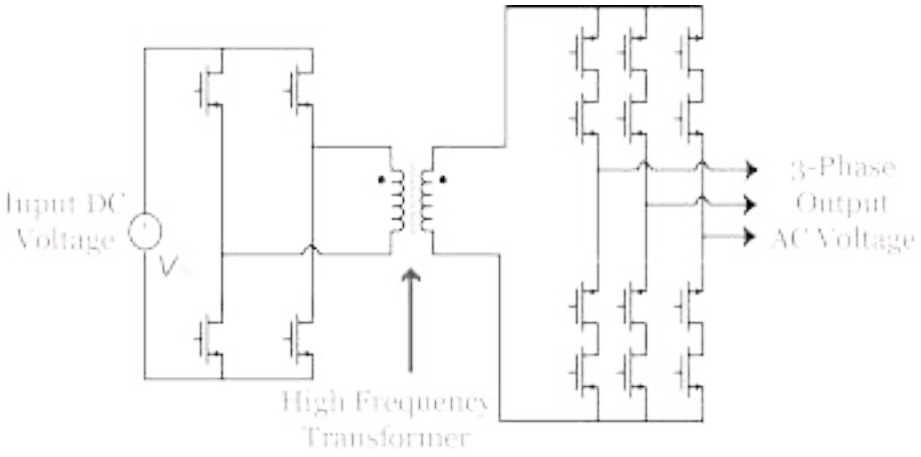


Figure 2.42: The topology of the high-frequency dc-link dc-ac inverter.

2.6 Conclusion

This chapter surveyed of the state of the art power electronic building blocks, as it reviewed the unidirectional and bidirectional dc-dc structures with integrated switched-capacitor, switched-inductor, quadratic , and multilevel networks. In addition, it reviewed the popular non-isolated and isolated dc-ac inverters.

Chapter 3 Analysis and Design of a Three-Level Boost Converter with Wide Gain Range for Fuel Cell Automotive Applications

3.1 Introduction

In this chapter, a new three-level boost converter with continuous input current, common ground, reduced voltage stress on the power switches, and wide voltage gain range is proposed. The proposed converter is composed of a three-level flying capacitor switching cell and an integrated LC^2D output network. The LC^2D output network enhances the voltage gain of the converter and reduces the voltage stress on the power switches. The proposed converter is a good candidate to interface fuel-cells to the dc-link bus of the three-phase inverter of the electric vehicle (EV). Full steady-state analysis of the proposed converter in the continuous conduction mode (CCM), converter components design is given in this chapter. A 1.2 kW scaled-down laboratory setup was built using Gallium Nitride (GaN) transistors and Silicon Carbide (SiC) diodes to verify the feasibility of the proposed converter.

3.2 Structure and Operating Principles of the Proposed Converter

3.2.1 General Structure of the Proposed Converter

The proposed converter is presented in Figure. 2, where it is composed of two active switches (Q_1, Q_2), three diodes (D_1, D_2, D_3), two inductors (L_1, L_2), and four capacitors (C_1, C_2, C_3, C_4). The fuel cell is depicted as a dc voltage source (V_{in}). The network of (Q_1, Q_2, D_1, D_2, C_2, C_3) forms a three-level flying-capacitor switching cell. The LC^2D output network enhances the voltage gain and reduces the voltage stress on the power switches.

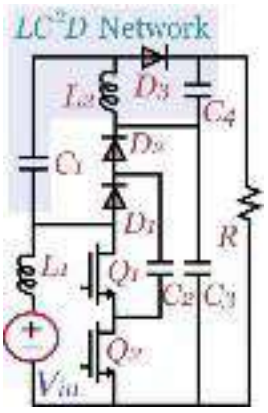
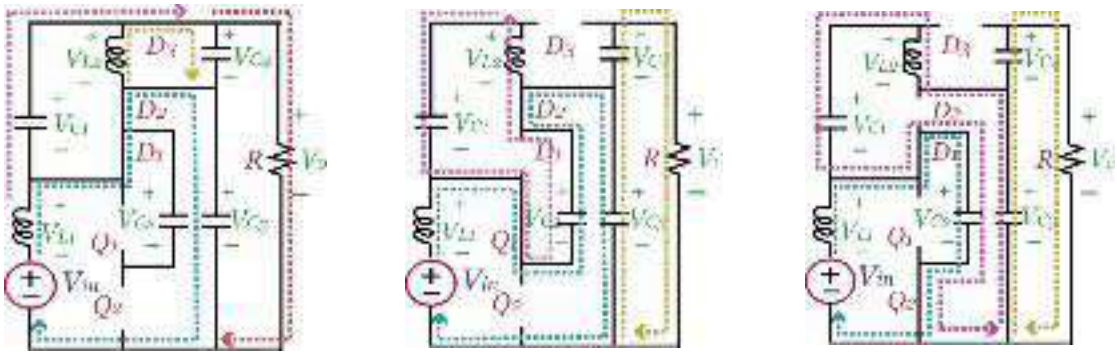


Figure 3.1: The schematic of the proposed converter

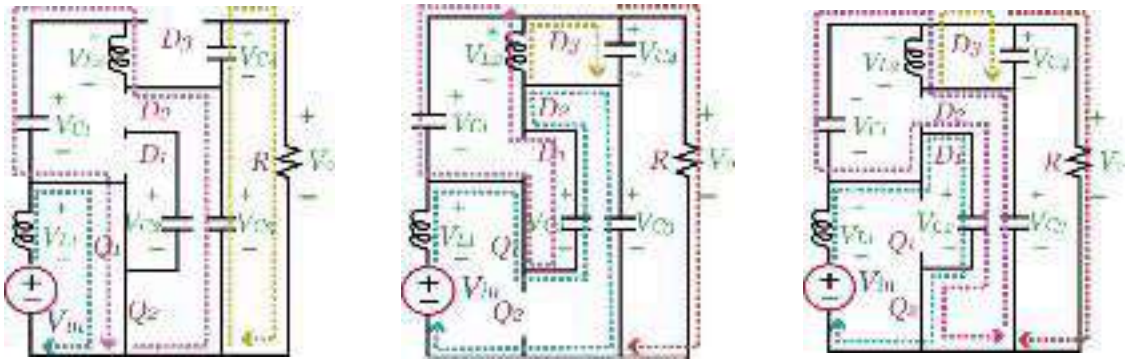
3.2.2 Operation Modes

The proposed converter has two active switches, hence, it has four possible switching states for Q_1 and Q_2. These switching states are: S_1 S_2 = {00, 01, 10, and 11}, as S_1 and S_2 are the triggering signals of Q_1 and Q_2, respectively.



(a) (b) (c)

Figure 3.2: Current flow paths when D < 0.5. (a) S1S2 = 00. (b) S1S2 = 10. (c) S1S2 = 01.



(a) (b) (c)

Figure 3.3: Current flow paths when D > 0.5. (a) S1S2 = 11. (b) S1S2 = 10. (c) S1S2 = 01.

The triggering signals S_1 and S_2 are generated via comparing two phase-shifted 180° carrier signals with a modulation signal (D). This means that there are three possible switching sequences, based on the value of D. When $D > 0.5$, the switching sequence of S_1 S_2 is {10, 11, 01, 11, and 10}. When $D < 0.5$, the switching sequence of S_1 S_2 is {10, 00, 01, 00, and 10}. When $D = 0.5$, the switching sequence of S_1 S_2 is {10, 01, and 10}. The key waveforms of the proposed TLB converter are presented in Figure 3.4, and the current flow paths when $D < 0.5$ and $D > 0.5$ are shown in Figure 3.2 and Figure 3.3, respectively.

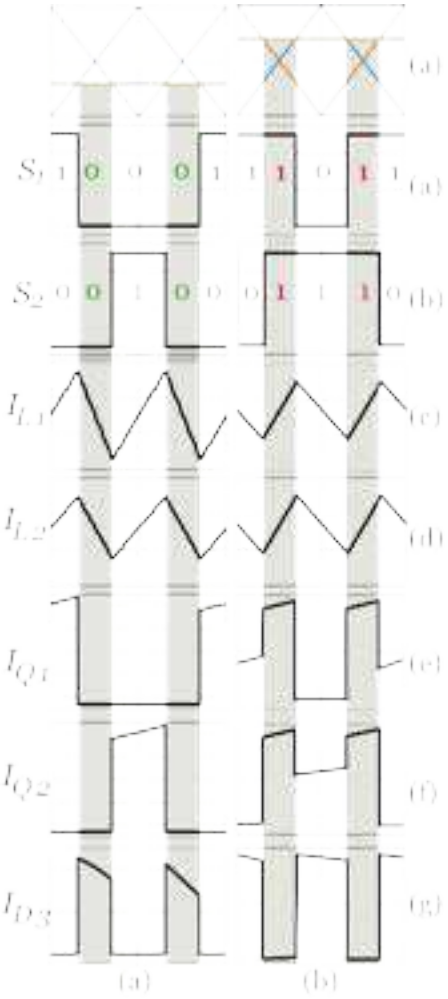


Figure 3.4: Key waveforms of the proposed converter (a) D < 0.5. (b) D > 0.5.

3.2.3 Analysis of Operating States

In this subsection, the proposed converter is analyzed during each of the four switching states, to be used after that in calculating the voltage gain and the voltage stress associated with each switching sequence.

When $S_1\ S_2$ = 01, shown in Figure 3(c) and 4(c), by applying the *Kirchhof's Voltage Law* (KVL) we get equations (1) and (2).

$$V_{L1} = V_{in} - V_{c2} \tag{1}$$

$$V_{L2} = V_{C1} + V_{C2} - V_{C3} \tag{2}$$

When $S_1\ S_2$ = 10, shown in Figure 3(b) and 4(b), by applying the KVL we get equations (3) and (4).

$$V_{L1} = V_{in} + V_{C2} - V_{C3} \tag{3}$$

$$V_{L2} = V_{C1} - V_{C2} \tag{4}$$

When $S_1\ S_2$ = 11, shown in Figure 4(a), by applying the KVL we get equations (5) and (6).

$$V_{L1} = V_{in} \tag{5}$$

$$V_{L2} = V_{C1} - V_{C3} \tag{6}$$

When $S_1\ S_2$ = 00, shown in Figure 3(a), by applying the KVL we get equations (7) and (8).

$$V_{L1} = V_{in} - V_{C3} \tag{7}$$

$$V_{L2} = V_{C1} \tag{8}$$

3.2.4 Wide Voltage Gain

In this subsection the voltage gain of the proposed converter is derived for $D > 0.5$ and $D < 0.5$. To simplify the analysis, all inductors and capacitors are assumed to be ideal and very large to apply the small ripple approximation. When $D > 0.5$, as shown in Fig. 6(b), the switching sequence of $S_1\ S_2$ is {10, 11, 01, 11, and 10}. In this switching sequence the time of

state {01}, T_{01}, the time of state {10}, T_{10}, and the time of state {11}, T_{11}, are defined as shown in (9):

$$\begin{cases} T_{01} = (1-D)T \\ T_{10} = (1-D)T \\ T_{11} = (2D-1)T \end{cases} \quad (9)$$

As T is the periodic time of the carrier signals.

By applying the volt-second balance rule on L_1 and L_2, we get equations (10) and (11):

$$V_{C3} = \frac{V_{in}}{1-D} \quad (10)$$

$$V_{C1} = \frac{D}{1-D} V_{in} \quad (11)$$

The output voltage V_o can be defined as the biggest value of the sum of "V_{C3}" and "V_{L2}". Thus, when $D > 0.5$, V_o can be calculated as following:

$$V_o = V_{C3} + V_{C1} - V_{C2} \quad (12)$$

Since C_2 and C_3 are the two capacitors of a three-level flying capacitor network, thus, V_{C2} is half V_{C3}, hence:

$$V_o = \frac{V_{C3}}{2} + V_{C1} \quad (13)$$

By substituting by (10) and (11) in (13), we get:

$$V_o = \frac{0.5+D}{1-D} V_{in} \quad (14)$$

Thus the voltage gain, M, is defined by (15):

$$M = \frac{V_o}{V_{in}} = \frac{0.5+D}{1-D} \quad (15)$$

When $D < 0.5$, as shown in Fig. 6(a), the switching sequence of S_1 S_2 is {10, 00, 01, 00, and 10}. In this switching sequence T_{01}, T_{10}, and the time of state {00}, T_{00}, are defined as following:

$$\begin{cases} T_{01} = DT \\ T_{10} = DT \\ T_{00} = (1-2D)T \end{cases} \quad (16)$$

By applying the volt-second balance rule on L_1 and L_2, we get equations (17) and (18):

$$V_{C3} = \frac{V_{in}}{1-D} \quad (17)$$

$$V_{C1} = \frac{D}{1-D} V_{in} \quad (18)$$

In this switching sequence V_o can be defined as the biggest value of the sum of "V_{C3}" and "$-V_{L2}$". Thus, when $D < 0.5$, V_o can be calculated as following:

$$V_o = V_{C3} + V_{C1}$$

(19) By substituting by (17) and (18) in (19), we get:

$$V_o = \frac{1+D}{1-D} V_{in} \quad (20)$$

Thus the voltage gain, M, is defined by (21):

$$M = \frac{V_o}{V_{in}} = \frac{1+D}{1-D} \quad (21)$$

The equations derived for $D > 0.5$ case can be applied for $D = 0.5$.

When $S_1 S_2$ is {10, or 01}, the states of L_1 and L_2 depend on the value of D. From equations (1)-(4), the voltage across L_1 and L_2 can be defined as following:

$$V_{L1} = \frac{0.5-D}{1-D} V_{in} \quad (22)$$

$$V_{L2} = \frac{D-0.5}{1-D} V_{in} \quad (23)$$

By means of equations (22), and (23), and the voltage polarities shown in Figures 3 and 4, both L_1 and L_2 are charging when D is less than 0.5, while they are discharging when D is greater than 0.5.

3.2.5 Voltage Stress Analysis

The voltages across C_4 equals ($V_o - V_{C3}$). The voltages across C_1, C_2, and C_3 are described by equations (24), and (25)

$$V_{C2} = \frac{V_{C3}}{2} = \begin{cases} \frac{V_o}{2(1+D)} & D < 0.5 \\ \frac{V_o}{1+2D} & D \geq 0.5 \end{cases} \quad (24)$$

$$V_{C1} = \begin{cases} \frac{D\,V_o}{(1+D)} & D < 0.5 \\ \frac{D\,V_o}{(0.5+D)} & D \geq 0.5 \end{cases} \quad (25)$$

The voltage across Q_1, Q_2, D_1, D_2, and D_3 can be expressed by (26).

$$V_{Q1} = V_{Q2} = V_{D1} = V_{D2} = V_{D3} = \frac{V_{C3}}{2} = \begin{cases} \frac{V_o}{2(1+D)} & D < 0.5 \\ \frac{V_o}{1+2D} & D \geq 0.5 \end{cases} \quad (26)$$

3.2.6 Current Stress Analysis

In this subsection the current stresses on both the semiconductor devices and inductors are derived. The analysis is divided into two parts, depending on the value of D. In the following equations, the output load current is I_o, the average currents of inductors L_1 and L_2 are I_{L1} and I_{L2}, respectively, the average charging currents of capacitors C_1, C_2, C_3, and C_4 are I_{C1_ch}, I_{C2_ch}, I_{C3_ch}, and I_{C4_ch}, respectively, and the average discharging currents of capacitors C_1, C_2, C_3, and C_4 are I_{C1_disch}, I_{C2_disch}, I_{C3_disch}, and I_{C4_disch}, respectively.

(For $D > 0.5$)

The current stresses can be obtained as following:

$S_1 S_2 = 11$:

In this switching state C_3 discharges, C_1 charges, C_2 neither charges nor discharges, and C_4 discharges. Diode D_3 is reverse biased. By applying *Kirchhof's Current Law* (KCL), the relationships between the inductor and capacitor currents can be expressed as following:

$$I_{C3\_disch} = - I_{L2} \quad (27)$$

$$I_{C1\_ch} = - I_{L2} \quad (28)$$

$$I_{C4\_disch} = - I_{L2} = - I_o \quad (29)$$

$S_1 S_2 = 10$:

In this switching state C_3 charges, C_1 discharges, C_2 discharges, and C_4 charges. Diode D_3 is forward biased. We get the following equations:

$$I_{C3\_ch} = - I_{C2\_disch} - I_{L2} \quad (30)$$

$$I_{C4\_ch} = I_{C1\_disch} \quad (31)$$

$$I_{C1\_disch} = - I_{C2\_disch} + I_{L1} \quad (32)$$

$S_1 S_2 = 01$:

In this switching state C_3 discharges, C_1 discharges, C_2 charges, and C_4 charges. Diode D_3 is forward biased. We get the following equations:

$$I_{C3\_disch} = - I_{L2} \quad (33)$$

$$I_{C4\_ch} = I_{C1\_disch} \quad (34)$$

$$I_{C1\_disch} = - I_{C2\_ch} + I_{L1} \quad (35)$$

By using the capacitor charge-second balance rule on capacitors C_1, C_2, C_3, and C_4, the following relationships can be obtained:

$$I_{C1\_disch} = \frac{2D-1}{2(1-D)} I_{L2} \quad (36)$$

$$I_{C2\_ch} = - I_{C2\_disch} = I_{L1} - I_{C1\_disch} \quad (37)$$

$$I_{C3\_ch} = - I_{C2\_disch} - I_{L2} \quad (38)$$

$$I_{C4\_ch} = I_{L2} + I_{C1\_disch} - I_o \quad (39)$$

$$I_{L2} = I_o \quad (40)$$

Assuming a lossless operation, the relationship between I_o and I_{L1} can be obtained as following:

$$V_{in}\, I_{L1} = V_o\, I_o \tag{41}$$

$$I_{L1} = \frac{(0.5+D)Io}{(1-D)} \tag{42}$$

When $D > 0.5$, diode D_3 conducts only during $S_1\, S_2 = \{10, \text{and } 10\}$, and the instantaneous current flowing through D_3 during T_{01} and T_{10} is I_{D3}. During $S_1\, S_2 = \{11\}$, the instantaneous current flowing through Q_1, and Q_2 is I_{Q_11}. During $S_1\, S_2 = \{10\}$, the instantaneous currents flowing through Q_1, Q_2, D_1, and D_2 are I_{Q1_10}, I_{Q2_10}, I_{D1_10}, and I_{D2_10} respectively. During $S_1\, S_2 = \{01\}$, the instantaneous currents flowing through Q_1, Q_2, D_1, and D_2 are I_{Q1_01}, I_{Q2_01}, I_{D1_01}, and I_{D2_01} respectively.

$$I_{D3} = \frac{1}{2(1-D)}\, I_{L2} \tag{43}$$

$$I_{Q\_11} = I_{L1} + I_{L2} \tag{44}$$

$$I_{Q1\_10} = I_{Q2\_01} = I_{D2\_10} = I_{D1\_01} = I_{C2\_ch} \tag{45}$$

$$I_{Q1\_01} = I_{Q2\_10} = I_{D1\_10} = I_{D2\_01} = 0 \tag{46}$$

The root-mean-square (rms) values of currents flowing through the components of the converter are essential for loss analysis. The rms values of I_{Q1}, I_{Q2}, I_{D1}, I_{D2}, I_{D3}, I_{C1}, I_{C2}, I_{C3}, and I_{C4} are I_{Q1_rms}, I_{Q2_rms}, I_{D1_rms}, I_{D2_rms}, I_{D3_rms}, I_{C1_rms}, I_{C2_rms}, I_{C3_rms}, and I_{C4_rms}, respectively. Using equations (9), (27)-(46) we can obtain the following equations:

$$I_{Q1\_rms} = I_{Q2\_rms} = \sqrt{(2D-1)\,(I_{L1} + I_{L2})^2 + (1-D)\left(I_{L1} - I_{C1\_disch}\right)^2} \tag{47}$$

$$I_{D1\_rms} = I_{D2\_rms} = \sqrt{(1-D)\left(I_{L1} - I_{C1\_disch}\right)^2} \tag{48}$$

$$I_{D3\_rms} = I_{L2} = I_o \tag{49}$$

$$I_{C1\_rms} = \sqrt{(2D-1)\,(I_{L2})^2 + 2(1-D)\left(\frac{2D-1}{2(1-D)} I_{L2}\right)^2} \quad (50)$$

$$I_{C2\_rms} = \sqrt{2(1-D)\left(I_{L1} - I_{C1\_disch}\right)^2} \quad (51)$$

$$I_{C3\_rms} = \sqrt{(D)\,(I_{L2})^2 + (1-D)\left(I_{C2\_disch} - I_{L2}\right)^2} \quad (52)$$

$$I_{C4\_rms} = \sqrt{(2D-1)\,(I_o)^2 + 2(1-D)\left(I_{C1\_disch}\right)^2} \quad (53)$$

(For $D < 0.5$)

The current stresses can be obtained as following:

$S_1 S_2 = 00$:

In this switching state C_3 charges, C_1 discharges, C_2 neither charges nor discharges, and C_4 charges. Diode D_3 is forward biased. By applying the KCL rule, the relationships between the inductor and capacitor currents can be expressed as following:

$$I_{C3\_ch} = I_{L1} - I_{C1\_disch} - I_{L2} \quad (54)$$

$$I_{C4\_ch} = I_{L2} + I_{C1\_disch} - I_o \quad (55)$$

$S_1 S_2 = 10$:

In this switching state C_3 charges, C_1 charges, C_2 discharges, and C_4 discharges. Diode D_3 is reverse biased. We get the following equations:

$$I_{C3\_ch} = - I_{C2\_disch} - I_{L2} = I_{L1} \quad (56)$$

$$I_{C2\_disch} = - I_{L1} - I_{L2} \quad (57)$$

$$I_{C1\_ch} = - I_{L2} \quad (58)$$

$S_1 S_2 = 01$:

In this switching state C_3 discharges, C_1 charges, C_2 charges, and C_4 discharges. Diode D_3 is reverse biased. We get the following equations:

$$I_{C3\_disch} = - I_{L2} \tag{59}$$

$$I_{C2\_ch} = I_{L1} + I_{L2} \tag{60}$$

$$I_{C1\_ch} = - I_{L2} \tag{61}$$

By using the capacitor charge-second balance rule on capacitors C_1, C_2, C_3, and C_4, the following relationships can be obtained:

$$I_{C1\_disch} = \frac{2D}{1-2D} I_{L2} \tag{62}$$

$$I_{C2\_ch} = - I_{C2\_disch} = I_{L1} + I_{L2} \tag{63}$$

Assuming a lossless operation and using equation (41), the relationship between I_o and I_{L1} can be obtained as following:

$$I_{L1} = \frac{(1+D)Io}{(1-D)} \tag{64}$$

When $D < 0.5$, diode D_3 conducts only during $S_1 S_2 = \{00\}$, and the instantaneous current flowing through D_3 during T_{00} is I_{D3_00}. During $S_1 S_2 = \{00\}$, the instantaneous current flowing through D_3 ia I_{D3_00}. The relationship between transistor, diode, and inductor currents can be obtained as following:

$$I_{D3\_00} = \frac{1}{1-2D} I_{L2} \tag{65}$$

$$I_{Q1\_10} = I_{Q2\_01} = I_{D2\_10} = I_{D1\_01} = I_{L1} + I_{L2} \tag{66}$$

$$I_{Q1\_01} = I_{Q2\_10} = I_{D1\_10} = I_{D2\_01} = 0 \tag{67}$$

Using equations (16), (52)-(66) the rms values of transistor, diode, and capacitor currents can be expressed as following:

$$I_{Q1\_rms} = I_{Q2\_rms} = \sqrt{D\ (I_{L1} + I_{L2})^2} \tag{68}$$

$$I_{D1\_rms} = I_{D2\_rms} = \sqrt{D\ (I_{L1} + I_{L2})^2 + (1-2D)(\left(I_{L1} - I_{C1_{disch}}\right)^2} \tag{69}$$

$$I_{D3\_rms} = I_{L2} = I_o \tag{70}$$

$$I_{C1\_rms} = \sqrt{(2D)\,(I_{L2})^2 + 2(1-D)\left(\frac{2D}{1-2D} I_{L2}\right)^2} \tag{71}$$

$$I_{C2\_rms} = \sqrt{2D\,(I_{L1} + I_{L2})^2} \tag{72}$$

$$I_{C3\_rms} = \sqrt{(1-2D)\,(I_{L2})^2 + D\left(I_{L1} - I_{C1\_disch} - I_{L2}\right)^2 + D\,(I_{L1})^2} \tag{73}$$

$$I_{C4\_rms} = \sqrt{(1-2D)\left(I_{C1\_disch}\right)^2 + 2D\,(I_{L2})^2} \tag{74}$$

3.2.7 Comparative Study With Other Three-Level Boost Converters

Based on the derived equations (15), (21), and (26), that define the voltage gain and stress of the proposed converter, comparative analysis can be made between the proposed converter and other multilevel converters, as shown in TABLE 3.1. In this comparison, the proposed converter is compared with the conventional TLB converter, a three-level quasi-z-source (TL-QZS) converter in [176], and an input-parallel-output-series (IPOS) converter in [177].

The conventional TLB converter has an ideal voltage gain of 1/(1-*D*). The voltage stress across the semiconductor devices of the conventional TLB converter is V_o /2. In [176], this converter has a voltage gain 2/(3-4*D*), and voltage stress across the semiconductor devices V_o /2. The duty cycle of this converter is limited between 50% to 75%, which makes the converter very sensitive to any change in duty. In [177], the converter discussed in this paper has a voltage gain 2/(1-*D*), and voltage stress across the power switches V_o/2. Table 3.1 presents a peer-to-peer comparison between the proposed converter, the TL-QZS converter in [176], and the IPOS converter in [177].

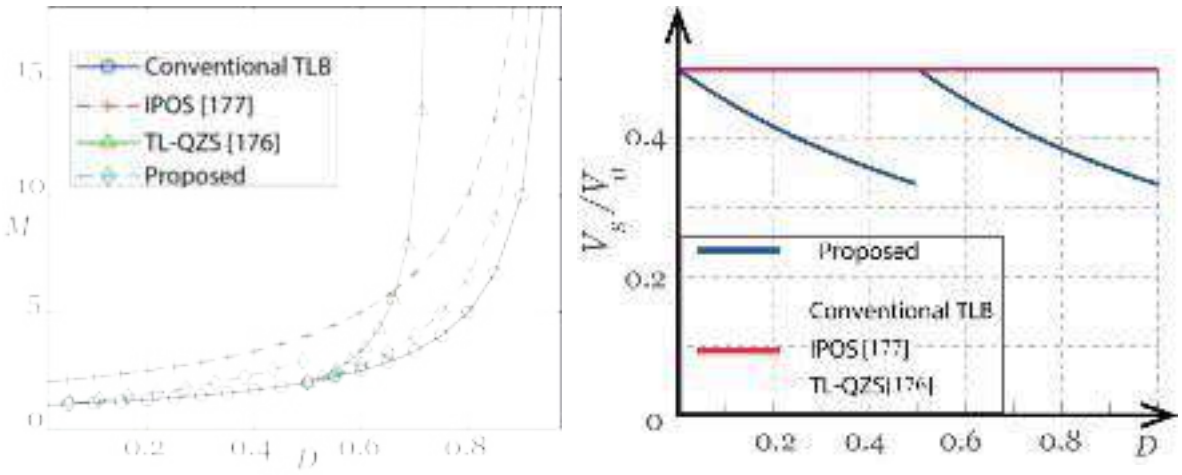
Table 3.1: Comparisons Between Proposed and Other Step-Up Solutions Comparisons Between Proposed and Other Step-Up Solutions

	Conventional TLB Converter	TL-QZS Converter in [12]	IPOS Converter in [22]	Proposed Converter
Voltage Gain	$\frac{1}{1-D}$	$\frac{2}{3-4D}$ ($0.5 \leq D <$ 0.75)	$\frac{2}{1-D}$ ($0 \leq D < 1$)	$\frac{1+D}{1-D}$, ($0 < D < 0.5$) $\frac{0.5+D}{1-D}$, ($D \geq 0.5$)
Voltage Stress	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2}$	$\frac{V_o}{2(1+D)}$, ($0 < D < 0.5$) $\frac{V_o}{1+2D}$, ($D \geq 0.5$)
Number of Transistors	2	2	2	2
Number of Diodes	2	3	3	3
Number of Inductors	1	2	2	2
Number of Capacitors	2	4	3	4

Figure 3.5 (a) and Figure 3.5 (b) show a comparison of the voltage gain *M* versus duty cycle *D*, and the normalized voltage stress (V_s/V_o) versus *D* among the four converters, respectively. This comparison shows that the proposed converter has a higher voltage gain compared to the conventional TLB converter. The TL-QZS converter has a higher voltage gain compared to the proposed converter, but the main drawback for the TL-QZS converter is the limited

operational range ($0.5 \leq D < 0.75$). The IPOS converter in [177] has the highest voltage gain, however, the proposed converter has the least voltage stress on the semiconductor devices, which means that it can be built using semiconductor devices with lower rated voltage, leading to higher efficiency, less cooling system requirement, hence, higher power density.

From equation (26), the stress voltage in the proposed converter depends on both V_O and D, and the stress voltage swings between 50% of V_O and 33.33% of V_O.



(a) (b)

Figure 3.5: Comparison between the proposed converter and other step-up converters. (a) Gain vs. duty cycle. (b) Voltage stress vs. duty cycle.

3.3 Component Parameters Design

3.3.1 Selection of The Semiconductor Devices

From equations (15), (21), and (26) the voltage stress across the semiconductor devices depends on both the output voltage and the value of D, as depicted in Fig. 7(b). The peak current flowing through Q_1, and Q_2 when the proposed converter is operating at $D < 0.5$ and $D > 0.5$ is the sum of the input and output currents. The peak current flowing through D_1, and D_2 when the proposed converter is operating at $D < 0.5$ and $D > 0.5$ is described by (75). Equations (43) and (65) show the peak instantaneous current that flows through D_3.

$$I_{d1\_peak} = I_{d2\_peak} = \begin{cases} I_{L1} + I_{L2} & D < 0.5 \\ I_{L1} - I_{L2}\frac{2D-1}{2(1-D)} & D \geq 0.5 \end{cases} \quad (75)$$

With the growing advancements in the area of wide bandgap (WBG) semiconductor devices, utilizing these devices in the proposed converter enhances the efficiency of the converter, leading to reduction in the cooling system requirement, which in the end yields high power density and high specific power. For diodes D_1, D_2, and D_3, Silicon Carbide (SiC) schottky diodes can be utilized since they have zero reverse recovery charges ($Q_{rr} = 0$), which alleviates the problem of the reverse recovery current that causes EMI problems. For Q_1, and Q_2, there are three major technologies available in the market for transistors, namely: SiC metal oxide field effect transistor (SiC MOSFET), Gallium Nitride (GaN) enhancement high electron mobility transistor (E-HEMT), and GaN cascode HEMT. The lateral GaN HEMT is based on the piezoelectric effect between a layer of GaN and a layer of Aluminum Gallium Nitride (AlGaN), which results in a 2-D electron gas (2-DEG) electron gas layer between the drain (D) and source (S) of the GaN HEMT, which reduces the on resistance of the device. The GaN E-HEMT has the lowest on resistance (R_{on}) and the lowest gate charge (Q_{GD}) compared to SiC MOSFETs, and GaN cascode HEMTs. The driving of GaN E-HEMTS is very challenging since they are very sensitive to the parasitics of the printed circuit board (PCB). The GaN cascode HEMT is composed of a high voltage depletion GaN die and a low voltage enhancement Silicon (Si) MOSFET, and it does not have the driving circuits' problems as in the GaN E-HEMT as the GaN cascode HEMT is driven like a typical Si MOSFET. The GaN cascode HEMT has a slightly higher R_{on} and Q_{GD} compared to the GaN E-HEMT, thus, if the power electronics designer can afford the time to optimize the PCB to minimize the power-loop and the gate-to-source-loop parasitic inductances, the utilization of the GaN E-HEMT is recommended. In Table 3.2, a peer-to-peer comparison between three

WBG transistors available in the market. This shows that if the converter is built using GaN E-HEMTs, it will have lower conduction and switching losses.

Table 3.2: COMPARISON BETWEEN WBG TRANSISTORS AVAILABLE IN THE MARKET

	SCT2120AF	**TPH3212PS**	**GS66508T**
Manufacturer	ROHM	Transphorm	GaN Systems
Semiconductor Material	SiC	GaN	GaN
Transistor Technology	MOSFET	Cascode HEMT	Enhancement HEMT
I_D Continuous	29 A	27 A	30 A
Device Package	TO220AB	TO-220	GaNPX-4
Switch Dimensions	-	15X10 mm^2	7X4.5 mm^2
R_{on}	120 mΩ	72 mΩ	55 mΩ
Q_{GD}	17 nC	14 nC	1.8 nC
Q_{rr}	53 nC	90 nC	0
Junction to Case Thermal Resistance	0.86 °C/W	1.2 °C/W	0.5 °C/W
Figure of Merit (Q_{GD} X R_{on})	2040	1008	99

3.3.2 Design of The Inductors

If the maximum allowed current ripples allowed for L_1, and L_2 are ΔI_{L1} and ΔI_{L2}, respectively, both inductors can be designed as following: The inductances can be calculated in the charging state:

$$L_1 = \frac{\Delta T}{\Delta I_{L1}} V_{L1} \tag{76}$$

$$L_2 = \frac{\Delta T}{\Delta I_{L2}} V_{L2} \tag{77}$$

Where ΔT is the charging time, which is T_{11} (when $D > 0.5$), and is T_{10} or T_{01} (when $D < 0.5$). The values of L_1, and L_2 can be determined using (78).

$$L_1 \text{ or } L_2 = \begin{cases} \frac{D(0.5-D)}{\Delta I_L f_s (1-D)} V_{in} & D < 0.5 \\ \frac{(2D-1)(D-0.5)}{\Delta I_L f_s (1-D)} V_{in} & D > 0.5 \end{cases} \quad (78)$$

Where f_s is the switching frequency, and ΔI_L can be ΔI_{L1} or ΔI_{L2}.

3.3.3 Design of Capacitors

Assuming that the maximum allowed voltage ripples allowed for C_1, C_2, C_3, and C_4 are ΔC_1, ΔC_2, ΔC_3 and ΔC_4, respectively, the capacitances of these four capacitors can be calculated as following where ΔT can be the charging time or the discharging time. The following relationships define the correlation between the capacitors' ripple voltages and their capacitances.

$$\begin{aligned} C_1 &= \frac{\Delta T}{\Delta V_{C1}} I_{C1} \\ C_2 &= \frac{\Delta T}{\Delta V_{C2}} I_{C2} \\ C_3 &= \frac{\Delta T}{\Delta V_{C3}} I_{C3} \\ C_4 &= \frac{\Delta T}{\Delta V_{C4}} I_{C4} \end{aligned} \quad (79)$$

$$C_1 = \begin{cases} \frac{D\, I_o}{\Delta V_{C1} f_s} & D < 0.5 \\ \frac{(2D-1)\, I_o}{\Delta V_{C1} f_s} & D > 0.5 \end{cases} \quad (80)$$

$$C_2 = \begin{cases} \frac{D\,(I_{L1}+I_o)}{\Delta V_{C2} f_s} & D < 0.5 \\ (I_{L1} - \frac{2D-1}{2(1-D)} I_o)(\frac{1-D}{\Delta V_{C2} f_s}) & D > 0.5 \end{cases} \quad (81)$$

$$C_3 = \begin{cases} \frac{D\, I_o}{\Delta V_{C3}\, f_s} & D < 0.5 \\ \frac{(1-D)\, I_o}{\Delta V_{C3}\, f_s} & D > 0.5 \end{cases} \quad (82)$$

$$C_4 = \begin{cases} \frac{D\, I_o}{\Delta V_{Co}\, f_s} & D < 0.5 \\ \frac{(2D-1)\, I_o}{\Delta V_{C4}\, f_s} & D > 0.5 \end{cases} \quad (83)$$

3.4 Loss Analysis

The losses in the proposed converter can be divided into five major contributors, namely: conduction and switching losses of the transistors Q_1, and Q_2, losses of the diodes D_1, D_2, and D_3, losses of the inductors (L_1, and L_2), and losses of the capacitors (C_1, C_2, C_3, and C_4).

3.4.1 Conduction Loss of Transistors

Since the rms currents flowing through Q_1, and Q_2 are the same, as shown in equations (47), and (68), and assuming that both transistors have the same on resistance, R_{on}, hence, the total conduction loss of both Q_1, and Q_2 can be calculated by (84).

$$P_{tr\_cond} = 2\, I_{Q1\_rms}^2\, R_{on} \quad (84)$$

3.4.2 Switching Loss of Transistors

In a typical transistor, there are four major contributors to the switching loss, namely: 1) The overlap of the transistor current and voltage at the instant of turning on and off, 2) Gate charge losses, and this power loss component is caused by the charge stored in the gate capacitance. 3) The loss caused by the parasitic capacitance of the transistor, this loss component is caused by the energy stored in C_{OSS} when the transistor is off, 4) The loss caused by the reverse recovery charge of the body diode of the transistor (since the experimental work was implemented with GaN E-HEMTs, which do not have a body diode and have zero reverse

recover charge, this loss component can be neglected). Equation (85) describes the total switching loss of the two transistors of the proposed converter, where f_s is the switching frequency, t_r, and t_f are the rise and fall times of the transistor, Q_T is the gate charge, and V_G is the gate driver voltage. The drain-to-source voltage of the E-HEMTs equals half V_{C3}, thus, depicted as V_{C2}.

$$P_{tr\_sw} = 2\, f_s\, (0.5\, V_{C2}\, I_{Q1}\, (t_r + t_f) + 0.5\, V_{C2}^2\, C_{OSS} + Q_T\, V_G) \quad (85)$$

3.4.3 Diode's Losses

Since the experimental setup is implemented using SiC schottky diodes, the reverse recovery switching loss of the diodes is neglected, however, the loss caused by the capacitive charge (Q_C) of the Schottky diodes is considered. The conduction loss of these diodes depends on the forward voltage and the rms currents flowing through the diodes. Equation (86) calculates the total losses of the three diodes of the proposed converter:

$P_d = V_{fd}\, (2\, I_{D1\_avg} + I_{D3\_avg}) + Q_C\, V_{C2}\, f_s$ (86) Where V_{fd}, and Q_C are the forward voltage, and the total capacitive charge of the SiC diode, respectively.

3.4.4 Inductor's Losses

The inductors have two main loss components, namely: the conduction loss, and the core loss. The conduction loss is caused by the dc current component flowing in the inductors' windings, while the core loss is caused by the inductors' ripple currents. The core loss equation should be provided by the core manufacturer. The inductors' total conduction loss, P_{L_cond}, can be calculated using (87), the inductors' core loss, P_{L_core}, can be calculated using (88), and the total losses in the inductors, P_{L_tot}, using (89).

$$P_{L\_cond} = I_{L1}^2 \, R_{L1} + \, I_{L2}^2 \, R_{L2} \tag{87}$$

Where R_{L1} and R_{L2} are the series parasitic resistances of L_1 and L_2, respectively.

$$P_{L\_core} = \frac{f}{\frac{a}{B^3}+\frac{b}{B^{2.3}}+\frac{c}{B^{1.65}}} + (\mathrm{df^2B^2}) \tag{88}$$

Equation (88) is provided by "Micrometals" (the manufacturer of the inductor cores used in the experimental prototype), where the equation's parameters can be derived from the datasheet of each specific core size and dimensions:

$$P_{L\_tot} = P_{L\_core} + P_{L\_cond} \tag{89}$$

3.4.5 Capacitor's Losses

The losses of the capacitors in the proposed converter are calculated as the conduction loss of these capacitors caused by their equivalent series resistance, ESR. The power loss of the four capacitors of the proposed converter, P_C is expressed by (90), where ESR_{C1}, ESR_{C2}, ESR_{C3}, and ESR_{C4} are the equivalent series resistances of the four capacitors.

$$P_C = I_{C1\_rms}^2 \, ESR_{C1} + I_{C2\_rms}^2 \, ESR_{C2} + I_{C3\_rms}^2 \, ESR_{C3} + I_{C4\_rms}^2 \, ESR_{C4} \tag{90}$$

3.5 Experimental Results and Analysis

A scaled-down experimental prototype was built, as shown in Figure 3.6, in order to validate the proposed converter topology and its theoretical analysis. In this experimental work, the fuel cell is depicted by a dc-voltage source. The converter is controlled by a TMS320f28377s microcontroller, and the currents are sensed by a hall-effect current transducer ACS730KLCTR-40AB-T. The power circuit is constructed using GS66508T E-HEMTs (rated voltage is 650 V, and rated current is 30 A), and C3D10065E SiC Schottky diodes (rated voltage is 650 V, and rated current is 32 A). The switching frequency, f_s, is 100 kHz, and the values of the two inductors L_1, and L_2 are 350µH and 250µH, respectively. The

capacitors C_1, C_2, C_3, and C_4 have the same value (capacitance = 80µF, and rated dc-voltage = 700 V). The load is represented by a 120 Ω resistance, R_L.

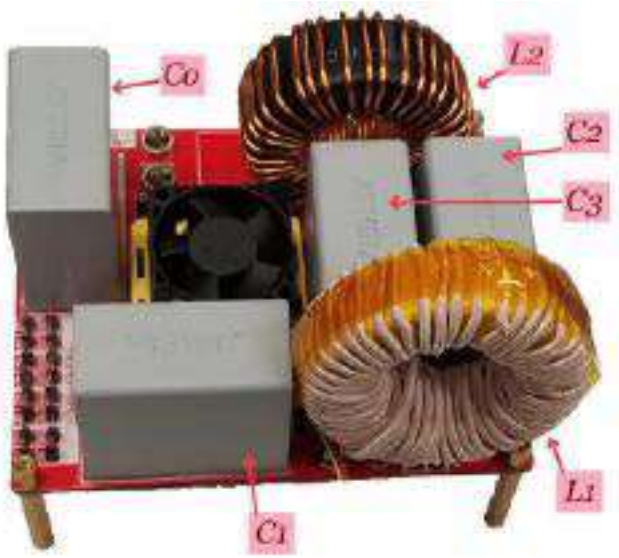


Figure 3.6: Experimental setup.

Table 3.3: MAIN EXPERIMENTAL PARAMETERS OF THE PROPOSED CONVERTER

Components and parameters	Values
Output power (P_{out})	1.15 kW, 1.3 kW
Input dc-voltage (V_{in})	200 V, 100 V
Switching frequency (f_s)	100 kHz
Inductor (L_1)	350 µH
Inductor (L_2)	250 µH
Capacitors (C_1, C_2, C_3, C_4)	80 µF, 700 V
E-HEMTs (Q_1, Q_2)	GS66508T (from GaN Systems)
Diodes (D_1, D_2, D_3)	C3D10065E (from Cree)
Load (R_L)	120 Ω

The main experimental parameters of the proposed converter prototype are shown in table 3.3.

In this experimental work, two case studies are investigated:

1) Case study I: V_{in} = 200 V, D = 0.3, R_L = 120Ω.

2) Case study II: V_{in} = 100 V, D = 0.7, R_L = 120Ω.

The experimental results of case study I are intended to verify the theoretical analysis of the converter when D < 0.5, and are presented in Figure 3.7, while the experimental results of case study II are intended to verify the theoretical analysis of the converter when D > 0.5, and are presented in Figure 3.8.

(Case Study I (D = 0.3, V_{in} = 200V, R_L = 120 Ω))

When D is less than 0.5, equations (18), (20), and (24) describe the four capacitors' voltages, and hence, they can be calculated as following: V_{C1} = 85.7 V, V_{C2} = 142.9 V, V_{C3} = 285.7 V, and V_o = 371.4 V. Figure 3.7(a) validates these findings. The two inductor currents, I_{L1}, and I_{L2} are shown in Figure 3.7(b), the frequency of the ripple currents is 200 kHz, which is double the switching frequency. The currents flowing through the two inductors I_{L1}, and I_{L2} are close to 5.5 A, and 3 A, respectively, which comply with the theoretical equations (64), and (70). The voltage stresses across the E-HEMTs (Q_1 and Q_2), and the diodes (D_1, D_2, and D_3), are shown in Figure 3.7(c), and Figure 3.7(d), respectively, where the voltage stresses swing between 0 V, and 140 V (= V_{C2}), which comply with equation (26). Figure 3.7(e), and Figure 3.7(f) show the currents flowing through the E-HEMTs, and the diodes, where the currents of (Q_1, Q_2, D_1, and D_2) swing between 0 A, and 9 A, which comply with equations (66), and (67). Also, Figure 3.7(e) shows I_{D3}, where D_3 conducts only when both Q_1 and Q_2 are off, and the magnitude of I_{D3} during conduction is close to 7.5 A which complies with

equation (65). It is worth noting that the semiconductor devices should be selected with higher rated voltage and current to assure operating in the safe operation area (SOA) of these devices and account for the voltage spikes (caused by the parasitic inductance of the PCB), and current spikes (caused by the parasitic capacitance of the SiC Shottky diodes).

(Case Study II (D = 0.7, V_{in} = 100V, R_L = 120 Ω))

From equations (11), (15), and (24), the voltage across the four capacitors can be calculated as following: V_{C1} = 233.33 V, V_{C2} = 166 V, V_{C3} = 333 V, and V_o = 400 V. These findings are verified by Figure 3.8(a). Figure 3.8(b) shows the currents flowing through the two inductors. I_{L1}, and I_{L2} which have ripple currents with frequency equals double the switching frequency of the converter (the periodic time of the ripple currents = 5µS, and the periodic time of the switching = 10µS). From Figure 3.8(b), I_{L2} is close to 3.3 A, and I_{L1} is close to 13 A, which verify equations (40), and (42). Figure 3.8(c), and Figure 3.8(d) show the voltage stress across the E-HEMTs and the diodes (D_1, D_2, and D_3), respectively, where the voltage stress swings between 0 V, and 166 V, namely: between 0 V, and half the voltage across C_3, which verifies equation (26). The currents of the E-HEMTs (Q_1, and Q_2) are shown in Figure 3.8(e), each current swings between three levels, 0 A (the E-HEMT is off, and the other one is on), 11 A (the E-HEMT is on, and the other one is off), and 16 A (both of the E-HEMTs are on), which verify equations (37), (44) and (45).

Figure 3.8(e) and Figure 3.8(f) show the currents flowing through the diodes (D_1, D_2, and D_3). From equations (45), and (46), diode D_1 conducts only when S_1S_2 = {01}, while diode D_2 conducts only when S_1S_2 = {10}, and the magnitude of the current flowing during conduction = $I_{L1} - ((2D - 1)\, I_{L2} / (2D - 2))$ = 11 A, which is verified by Figure 3.8(f).

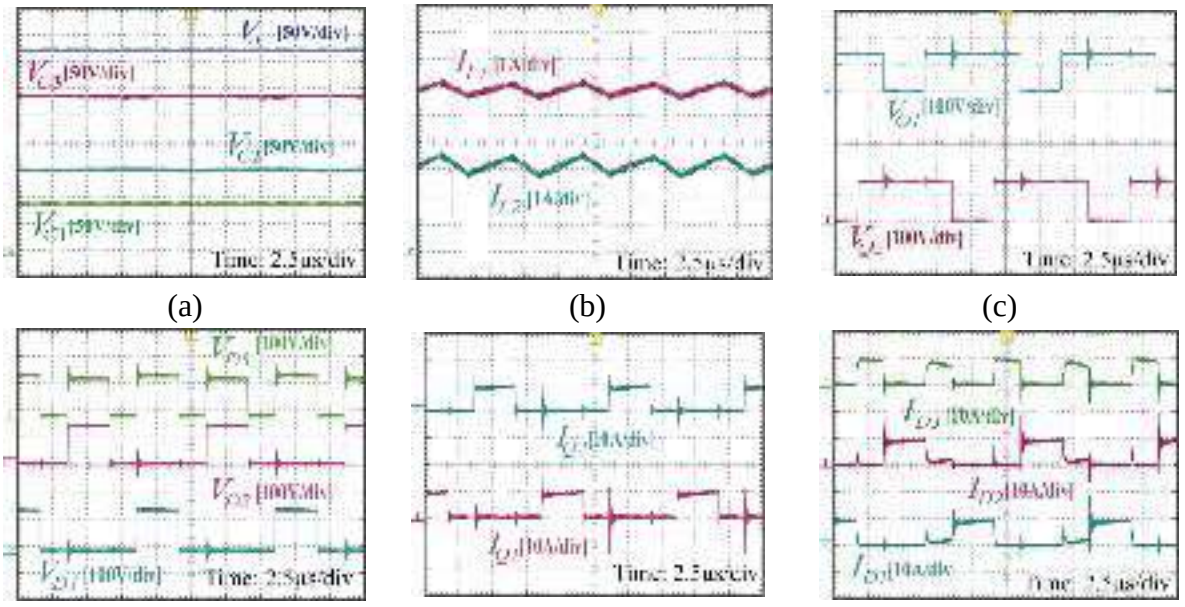


Figure 3.7: Experimental results when Vin = 200 V, D = 0.3, RL = 120Ω, Pout = 1.15 kW.

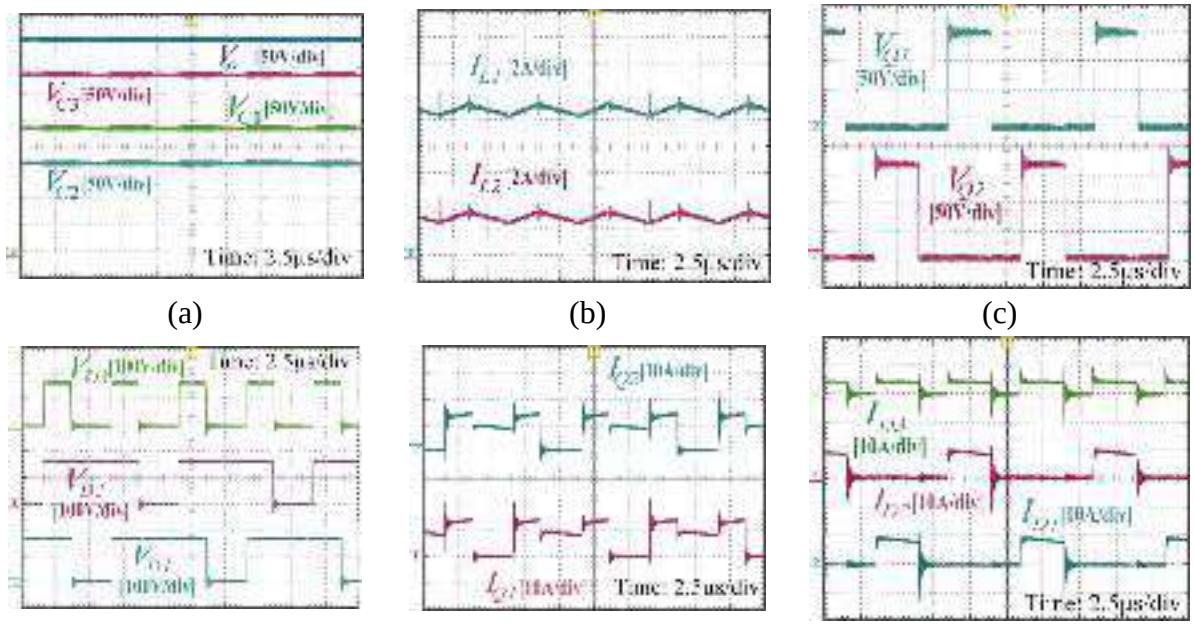
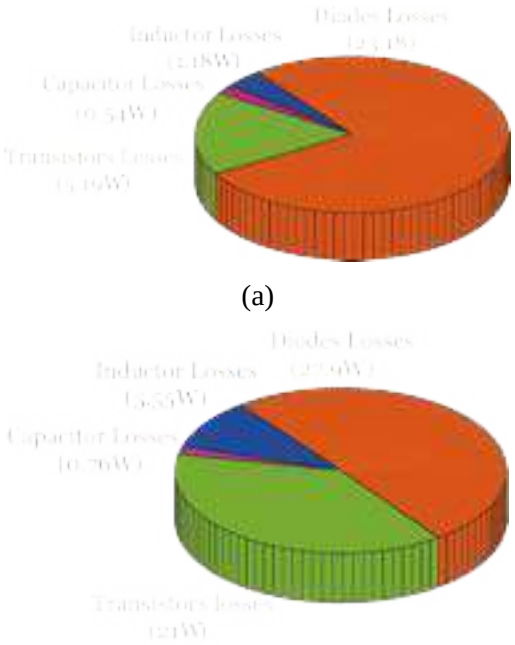


Figure 3.8: Experimental results when Vin = 100 V, D = 0.7, RL = 120Ω, Pout = 1.3 kW.

Figure 3.8(e) shows that D_3 conducts only when either of the E-HEMTs is off, and the current flowing during conduction is close to 6 A which verifies equation (43). Using equations (84)-(90) the losses of the proposed converter can be calculated for any value of V_{in}, D, and R_L. The converter losses for case studies I and III are investigated and analyzed. Figure

3.9 shows the loss distributions for the proposed converter for both case of study I and case of study II.



(a)

(b)

Figure 3.9: Calculated loss distributions for the experiment (a) When Vin = 200V, D = 0.3, and RL = 120Ω. (b) When Vin = 100V, D = 0.7, and RL = 120Ω.

Figure 3.9(a) shows the loss distributions when D = 0.3, V_{in} = 200 V, and R_L = 120 Ω, P_{out} = 1.15 kW. The total losses of the converter in this case of study equals 27.16 W, and the efficiency of the converter equals 97.6 %. The main contributor of losses in this case is the diodes (85.3% of total losses), because of their relatively high forward voltage (V_{fd}) = 1.8 V. The total losses of the E-HEMTs are 19 % of the total losses, and this is because of their low on resistance and zero reverse recovery charges. The losses of the inductors and capacitors account for 4.3 % and 2.8 % of the total losses of the proposed converter, respectively.

Figure 3.9(b) shows the loss distributions when D = 0.7, V_{in} = 100 V, and R_L = 120 Ω, P_{out} = 1.333 kW. The total losses of the converter in this case of study equals 55.21 W, and the

efficiency of the converter equals 95.86 %. The main contributor of losses in this case is also the diodes (50.5% of total losses).

The total losses of the E-HEMTs are 38 % of the total losses. The losses of the inductors and capacitors account for 10 % and 1.37 % of the total losses of the proposed converter, respectively.

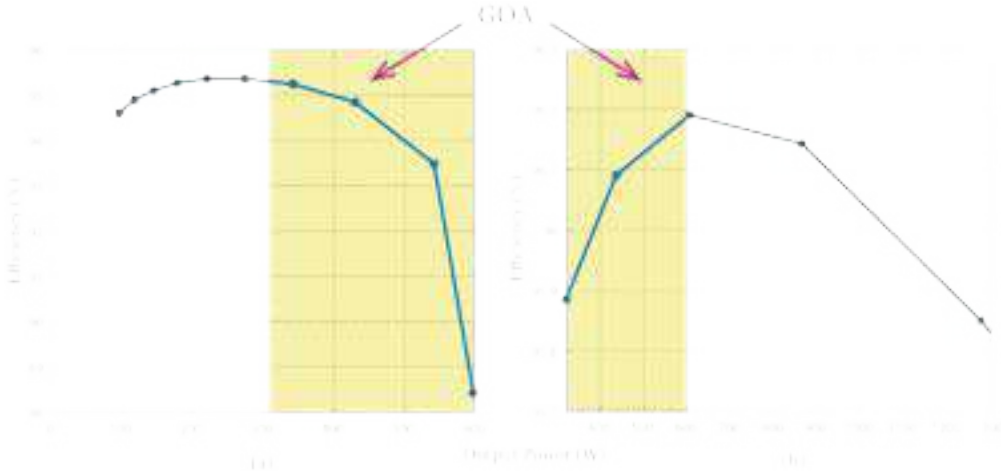


Figure 3.10: Efficiency curves of the proposed converter (Vin = 100V, RL = 120Ω) (a) When D < 0.5. (b) When D ≥ 0.5.

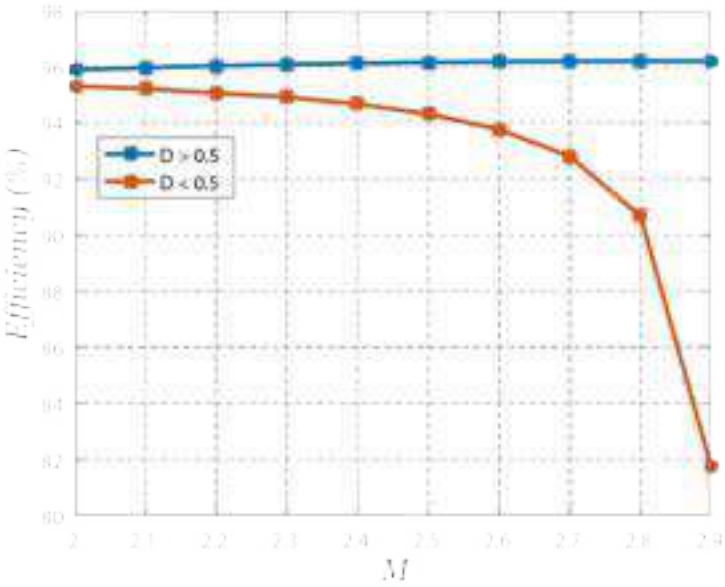


Figure 3.11: Calculated efficiency curves in the GOA (Vin = 100V, RL = 120Ω).

The efficiency curves of the proposed converter that depict the efficiency at different power levels are shown in Figure 3.9, and they were obtained from the experimental setup (V_{in} = 100 V, f_s = 100 kHz, R_L = 120 Ω). The efficiency is depicted by two curves, one for operation when $D < 0.5$, and the other one for operation when $D \geq 0.5$.

In the GOA, the same voltage gain (M) can be achieved by two different values of D, one of them is less than 0.5, and the other one is greater than 0.5. Figure 3.10 shows the calculated efficiency of the proposed converter in the GOA, when V_{in} = 100V, and R_L = 120Ω, one curve presents the efficiency versus M when D is less than 0.5, while the other curve shows the efficiency versus M when D is greater than 0.5. From Figure 3.11, it is obvious that if the desired M is in the GOA ($2 < M < 3$), the efficiency of the proposed converter is higher when D is selected to be higher than 0.5.

3.6 Conclusion

A new three-level boost (TLB) converter was introduced and presented. It can be used as an interface between the fuel cells and the dc-link bus of the three-phase inverter in the EV powertrain. It has several advantages of continuous input current, extended voltage gain, lower voltage stress on the semiconductor devices, common ground between the input and output ports, and wide voltage gain range. The steady state analysis of the proposed converter under the continuous conduction mode (CCM) was investigated. The voltage gain, the voltage stress on the semiconductor devices, and the number of the semiconductor devices and passive components of the proposed converter were compared with other three-level step-up solutions, and the importance of the proposed converter was verified experimentally. The proposed converter was built using GaN E-HEMTs and SiC Shottky diodes, and the experimental results validated the theoretical analysis.

Chapter 4 A Single-Switch Transformerless DC-DC Converter with Universal Input Voltage for Fuel Cell Vehicles: Analysis and Design

4.1 Introduction

A new single-switch high step-up dc-dc converter is proposed in this chapter for fuel cell vehicles. The proposed topology utilizes a $L^2C^3D^2$ network to obtain high voltage gain and reduce the voltage stress on the power switch. Additionally, the proposed converter has a universal input voltage in order to suit the soft output characteristics of the fuel cell. Comprehensive analyses of the steady-state operation in continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and design considerations of the proposed converter are given. Finally, a 400 V/1.6 kW scaled-down prototype is developed to validate the effectiveness and feasibility of the proposed converter.

4.2 Structure and Operating Principles of the Proposed Converter

4.2.1 Configuration of the Proposed Converter

The topology of the proposed converter is shown in Figure 4.1 It is composed of one power switch (Q), three diodes (D_1, D_2, and D_3), three inductors (L_1, L_2, and L_3), five capacitors (C_1, C_2, C_3, C_4, and C_o), and R represents a resistive load.

A conventional boost switching network is formed by (L_1, Q, D_1, and C_3), and an $L^2C^3D^2$ network formed by (L_2, L_3, C_1, C_2, C_4, D_2, and D_3) is integrated between the conventional boost switching network and the output capacitor C_o. The $L^2C^3D^2$ network enhances the voltage gain of the proposed converter and reduces the voltage stress on the power switch.

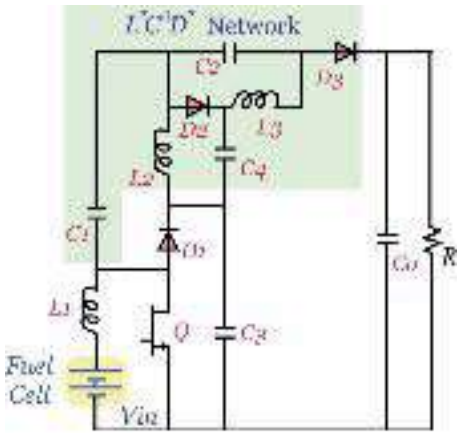


Figure 4.1: The schematic of the proposed converter.

4.2.2 Switching States Analysis

According to the conduction states of the semiconductor devices, the operation of the proposed converter can be divided into three switching states, as shown in Table 4.1. In this analysis, the following abbreviations are used: V_{in}, V_o, V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{L1}, V_{L2}, V_{L3}, I_{L1}, I_{L2}, I_{L3} and I_o, to refer to the input voltage, the output voltage, the instantaneous voltages across L_1, L_2, and L_3, the dc currents flowing through L_1, L_2, and L_3, and the output current, respectively.

Table 4.1: SWITCHING STATES OF THE SEMICONDUCTOR DEVICES

Switching state	*Q*	D_1	D_2	D_3
I (CCM & DCM)	ON	OFF	OFF	OFF
II (CCM & DCM)	OFF	ON	ON	ON
III (DCM)	OFF	OFF	OFF	OFF

Additionally, i_{C1_ch}, i_{C1_dis}, i_{C2_ch}, i_{C2_dis}, i_{C3_ch}, i_{C3_dis}, i_{C4_ch}, i_{C4_dis}, i_{Co_ch}, and i_{Co_dis}, refer to the charging and discharging currents of the five capacitors. For convenience of analysis, the following assumptions are made:

- The power switch and diodes are ideal.
- The equivalent series resistances of the inductors and capacitors equal zero.
- The capacitors and inductors are large enough, so, the small ripple principle can be applied.

1) **Switching State I:**

This switching state is for CCM and DCM operations and it takes place when the gate voltage V_{gs} of the power switch is high, and Q is turned on. In this switching state, the three diodes are reverse-biased, the three inductors are charging, C_3 and C_4 are discharging, C_1 and C_2 are charging, and C_o is discharging. Figure 4.3(a) shows the current flow paths for this switching state. By applying *Kirchhof's Voltage Law* (KVL), and *Kirchhof's Current Law* (KCL) on the equivalent circuit depicted in Figure 4.3(a), we can extract the following relationships:

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C3} - V_{C1} \\ V_{L3} = V_{C3} + V_{C4} - V_{C2} - V_{C1} \end{cases} \quad (1)$$

$$\begin{cases} i_{C1\_ch} = I_{L2} + I_{L3} \\ i_{C2_{ch}} = I_{L3} \\ i_{C3\_dis} = I_{L2} + I_{L3} \\ i_{C4\_dis} = I_{L3} \\ i_{Co\_dis} = I_o \end{cases} \quad (2)$$

2) **Switching State II:**

This switching state is for CCM and DCM operations and it takes place when V_{gs} is low, and Q is turned off. . In this switching state, the three diodes are forward-biased, the three inductors are discharging, C_3 and C_4 are charging, C_1 and C_2 are discharging, and C_o is charging.

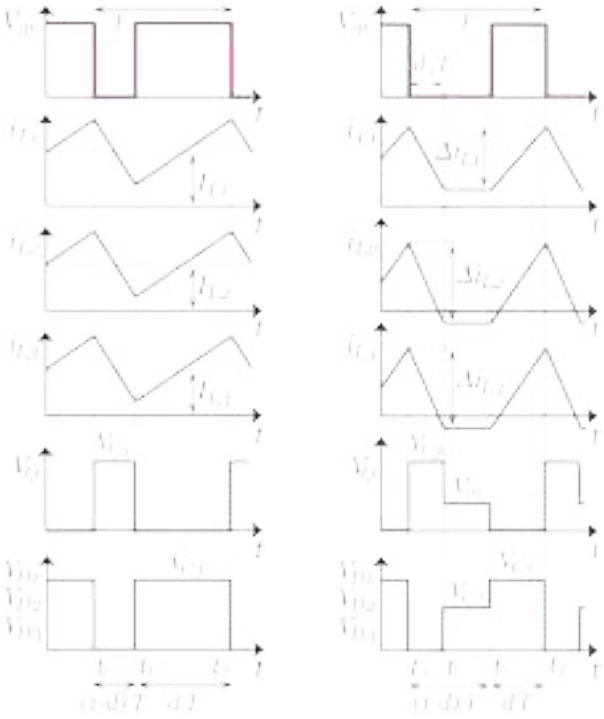
Figure 4.3(b) shows the current flow paths for this switching state. By applying KVL and KCL laws on the equivalent circuit depicted in Figure 4.3(b), we can extract the following relationships:

$$\begin{cases} V_{L1} = V_{in} - V_{C3} \\ V_{L2} = -V_{C1} = -V_{C4} \\ V_{L3} = -V_{C2} \end{cases} \tag{3}$$

$$\begin{cases} i_{C1\_dis} = i_{C2\_dis} + I_{L3} + i_{C4\_ch} - I_{L2} \\ i_{C3\_ch} = I_{L1} - i_{C1\_dis} - I_{L2} + i_{C4\_ch} \\ i_{Co\_ch} = i_{C2\_dis} + I_{L3} - I_o \end{cases} \tag{4}$$

3) **Switching State III:**

This switching state is for DCM operation and it takes place when V_{gs} is low, Q is turned off, and all the diodes are reverse-biased.



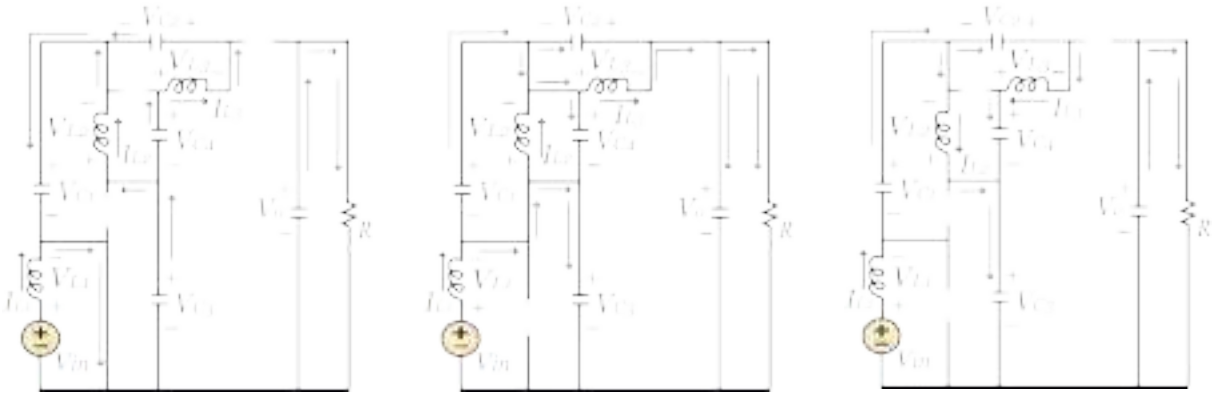
(a) (b)

Figure 4.2: Key waveforms of the proposed converter. (a) CCM operation. (b) DCM operation.

Since all the semiconductor devices do not conduct in this switching state, a positive constant current I_{L1_min} flows through L_1, and negative constant currents I_{L2_min}, I_{L3_min} flow through L_2 and L_3, as shown in Figure 4.3(c). The summation of the inductor currents is zero, and the voltages across the inductors in this switching state are null, as depicted in (5) and (6).

$$I_{L1\_min} + I_{L2\_min} + I_{L3\_min} = 0 \tag{5}$$

$$\begin{cases} V_{L1} = 0 \\ V_{L2} = 0 \\ V_{L3} = 0 \end{cases} \tag{6}$$



(a) (b) (c)

Figure 4.3: Equivalent circuits of the proposed converter. (a) Switching state I. (b) Switching state II. (c) Switching state III.

4.3 Steady-State Analysis of the Proposed Converter

4.3.1 CCM Operation

The key waveforms for this operation is presented in Figure 4.2(a). In this subsection, the voltage gain, the voltage stresses, the current stresses, and the efficiency analysis of the proposed converter operating in CCM are extracted. The operation in CCM is composed of *switching state I* (period = dT) and *switching state II* (period = (1-d) T), where d and T are the duty cycle and the periodic switching time, respectively.

1) Voltage Gain:

By applying the voltage second principle on the inductors L_1, L_2, and L_3 and using equations (1) and (3), we can obtain (7)-(9):

$$V_{C1} = V_{C2} = V_{C4} = \frac{d}{1-d} V_{in} \tag{7}$$

$$V_{C3} = \frac{1}{1-d} V_{in} \tag{8}$$

$$V_o = \frac{1+2d}{1-d} V_{in} \tag{9}$$

Thus, the voltage gain M_{CCM} can be calculated by (10):

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{1+2d}{1-d} \tag{10}$$

2) Analysis of Voltage Stress

The stress across the five capacitors is delivered by (7)-(9). As shown in Figure 4.2(a), the voltage across the semiconductor devices swings between 0V and V_{C3}, hence the voltage stress across the power switch V_Q and the voltage stress across the diodes V_D can be obtained by (11):

$$V_Q = V_D = V_{C3} = \frac{1}{1-d} V_{in} \tag{11}$$

Additionally, using (10), and (11) the voltage stress across the power switch and diodes can be represented as a function of M_{CCM}, as in (12):

$$V_Q = V_D = \frac{2+M_{CCM}}{3M_{CCM}} V_o \tag{12}$$

3) Analysis of Current Stress

Assuming the input power equals the output power of the converter (i.e. $V_{in} \times I_{L1} = V_o \times I_o$), hence, the currents I_{L2}, I_{L3}, and I_{L1} can be calculated as in (13) and (14):

$$I_{L2} = I_{L3} = I_o \tag{13}$$

$$I_{L1} = \frac{1+2d}{1-d}\, I_o = M_{CCM}\, I_o \tag{14}$$

By applying the charge-second balance principle on the five capacitors to calculate the charging and discharging currents of them, we can get (15)-(19):

$$\begin{cases} i_{C1\_ch} = 2I_o \\ i_{C1\_dis} = 2I_o\, \dfrac{d}{(1-d)} = 2I_o \left(\dfrac{M_{CCM}-1}{3}\right) \end{cases} \tag{15}$$

$$\begin{cases} i_{C2\_ch} = I_o \\ i_{C2\_dis} = I_o\, \dfrac{d}{(1-d)} = I_o \left(\dfrac{M_{CCM}-1}{3}\right) \end{cases} \tag{16}$$

$$\begin{cases} i_{C3\_ch} = 2I_o\, \dfrac{d}{(1-d)} = 2I_o \left(\dfrac{M_{CCM}-1}{3}\right) \\ i_{C3\_dis} = 2I_o \end{cases} \tag{17}$$

$$\begin{cases} i_{C4\_ch} = I_o\, \dfrac{d}{(1-d)} = I_o \left(\dfrac{M_{CCM}-1}{3}\right) \\ i_{C4\_dis} = I_o \end{cases} \tag{18}$$

$$\begin{cases} i_{Co\_ch} = I_o \dfrac{d}{(1-d)} = I_o \left(\dfrac{M_{CCM}-1}{3}\right) \\ i_{Co\_dis} = I_o \end{cases} \tag{19}$$

By means of (13)-(19), Figure 4.3(a), and Figure 4.3(b), the currents flowing through Q, D_1, D_2, and D_3 can be described as following:

$$i_Q = I_{L1} + I_{L2} + I_{L3} = \frac{3}{1-d}\, I_o \tag{20}$$

$$i_{D1} = I_{L1} - i_{C1\_dis} = \frac{1}{1-d}\, I_o \tag{21}$$

$$i_{D2} = I_{L2} + i_{C1\_dis} - I_{C2\_dis} = \frac{1}{1-d}\, I_o \tag{22}$$

$$i_{D3} = i_{C2\_dis} + I_o = \frac{1}{1-d}\, I_o \tag{23}$$

Using (10), equations (20)-(23) can be depicted as functions of M_{CCM}, as following:

$$i_Q = (M_{CCM} + 2)\, I_o \tag{24}$$

$$i_{D1} = i_{D2} = i_{D3} = \left(\frac{M_{CCM} + 2}{3}\right) I_o \tag{25}$$

The root-mean-square (rms) values of the currents flowing through the power switch, diodes, and capacitors are important in the efficiency analysis, and they can be extracted as following:

$$i_{Q\_rms} = \sqrt{(M_{CCM} + 2)(M_{CCM} - 1)}\, I_o \tag{26}$$

$$i_{D1\_rms} = i_{D2\_rms} = i_{D3\_rms} = \sqrt{\frac{M_{CCM} + 2}{3}}\, I_o \tag{27}$$

$$i_{C1\_rms} = i_{C3\_rms} = 2\sqrt{\frac{M_{CCM} - 1}{3}}\; I_o \tag{28}$$

$$i_{C2\_rms} = i_{C4\_rms} = i_{Co\_rms} = \sqrt{\frac{M_{CCM} - 1}{3}}\; I_o \tag{29}$$

4) Effect of Parasitic Elements on the Voltage Gain

In order to evaluate the effect of the parasitic elements of the passive and active components of the proposed converter on its voltage gain, some of these parasitic parameters were modeled in the proposed converter circuit, shown in Figure 4.4. In the non-ideal model of the converter, the following parameters are included: the resistances of the windings of inductors ($r_{L1} = r_{L2} = r_L$), the equivalent-series-resistances of capacitors ($r_{C1} = r_{C2} = r_{C3} = r_{C4} = r_{Co} = r_C$), the on-

resistance of the power switch (r_S), the forward voltages of the diodes ($V_{F1} = V_{F2} = V_{F3} = V_F$), and their respective on-resistances ($r_{D1} = r_{D2} = r_{D3} = r_{D4} = r_D$).

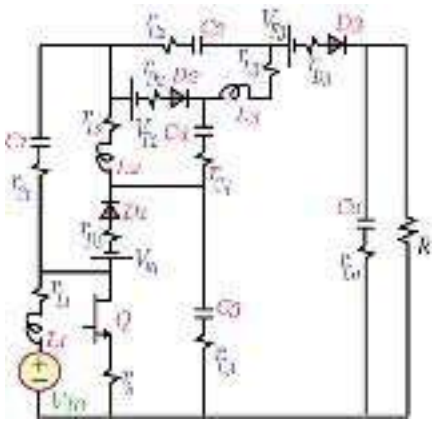


Figure 4.4: Equivalent circuit of the proposed converter with the parasitic elements.

After accounting for these parasitic parameters, the voltage gain of the proposed converter in its non-ideal model ($M\grave{}_{CCM}$) is depicted by equation (30). Figure 4.5 shows the graphical comparison between the voltage gain curves using the ideal and non-ideal models of the proposed converter, where the parasitic and operating parameters are considered as following: V_{in} = 50V, R = 100Ω, r_L = 30mΩ, r_C = 15mΩ, r_S = 20mΩ, V_F = 1V, and r_D = 70mΩ. It shows that the voltage gain of the non-ideal model of the converter is close to that of the ideal model when d is between 0 and 0.8 (where $M\grave{}_{CCM} \approx 13$) which indicates the high step-up capability of the proposed converter.

$$M\grave{}_{CCM} = \frac{R(1-d)(V_{in} - 3V_F + 3d\,V_F + 2d\,V_{in})}{V_{in}\left[R + 3r_D + 3r_L + d\left(6r_C - 2R - 3r_D + 3r_S + d(R - 6r_C + 6r_L - 12r_S)\right)\right]} \quad (30)$$

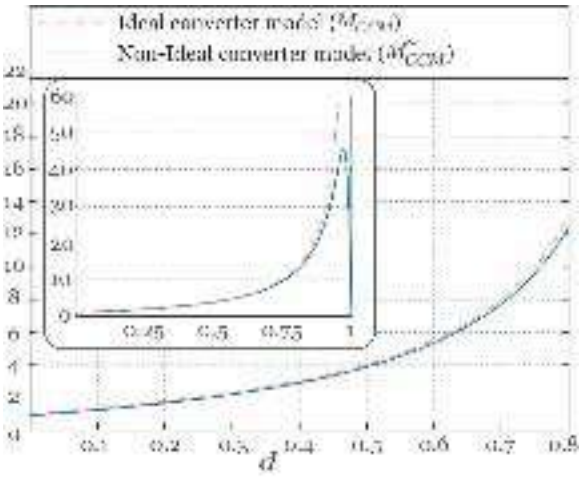


Figure 4.5: Voltage gain curves of the proposed converter.

4.3.2 DCM Operation

The key waveforms for this operation is shown in Figure 4.2(b). In this subsection, the voltage gain in DCM, boundary operating condition between CCM and DCM, and current stresses in DCM are given.

The operation in DCM is composed of *Switching State I* (period = *dT*), *Switching State II* (period = d_xT), and *Switching State III* (period = $1-(d+d_x)T$).

5) Voltage Gain

From (7)-(9), the capacitors' voltages can be rewritten as:

$$V_o = V_{C3} + 2V_{C2} \tag{31}$$

$$V_{C3} = V_{in} + V_{C2} = \frac{V_o + 2V_{in}}{3} \tag{32}$$

$$V_{C1} = V_{C2} = V_{C4} = \frac{V_o - V_{in}}{3} \tag{33}$$

By means of (1), (3), (6), (31)-(33), and applying the voltage second principle on L_1, we get the following:

$$\frac{1}{T}\left(\int_0^{dT} V_{in}dt - \int_0^{d_xT} \frac{V_o - V_{in}}{3}\, dt\right) = 0 \tag{34}$$

To solve (34) in order to extract the voltage gain in DCM, d_x should be determined.

As shown in Figure 4.6, and using equations (20)-(23), i_Q equals the summation of the three inductors' currents, and the current flowing in any of the three diodes equals one third i_Q. Thus, the peak diode current $i_{D(Peak)}$ can be calculated as following:

$$i_{D(Peak)} = \frac{1}{3}(\Delta i_{L1} + \Delta i_{L2} + \Delta i_{L3}) \tag{35}$$

The three inductors' currents in DCM can be calculated as:

$$\begin{aligned} \Delta i_{L1} &= \frac{dV_{in}}{f_s L_1} \\ \Delta i_{L2} &= \frac{dV_{in}}{f_s L_2} \\ \Delta i_{L3} &= \frac{dV_{in}}{f_s L_3} \end{aligned} \tag{36}$$

By substituting (36) into (35), we get (37):

$$i_{D(Peak)} = \frac{dV_{in}}{3f_s L_{eq}} \tag{37}$$

Where,

$$L_{eq} = \left(\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}\right)^{-1} \tag{38}$$

The average current flowing through any of the three diodes equals I_o, hence, we get the following:

$$\frac{1}{2} d_x i_{D(Peak)} = \frac{V_o}{R} \tag{39}$$

By substituting (37) into (39), we can get d_x as following:

$$d_x = \frac{6V_o}{dV_{in}} \tau \tag{40}$$

Where τ is the normalized inductor time constant, defined as:

$$\tau = \frac{L_{eq} f_s}{R} \tag{41}$$

By substituting (40) into (34), we get the following:

$$V_{in} + (V_{in} - V_o) \frac{V_o}{dV_{in}} \tau = 0 \tag{42}$$

By solving this quadratic equation (42), the voltage gain in DCM M_{DCM} can be extracted as in (43):

$$M_{DCM} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{2d^2}{\tau}}\right) \tag{43}$$

6) Boundary Operating Conduction

In boundary conduction mode (BCM) operation, M_{CCM} equals M_{DCM}, and accordingly, from (10) and (43), the boundary normalized inductor time constant τ_b can be obtained, as in (44).

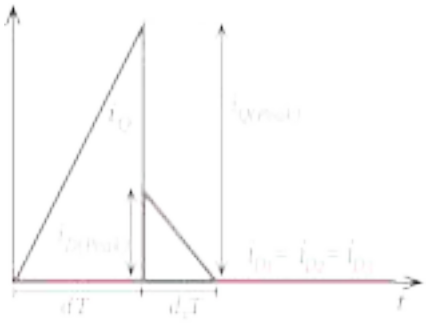


Figure 4.6: Power switch and diodes currents in DCM.

$$\tau_b = \frac{d(1-d)}{12d + 6} \tag{44}$$

The relationship between τ_b and d is presented in Figure 4.7. If $\tau > \tau_b$, then the proposed converter is working in CCM.

7) Voltage Stress Analysis

As shown in Figure 4.2(b), the voltage stress across *Q* during *Switching State I* $V_Q(I)$ *is null,* while during *Switching State II* $V_Q(II)$ and *Switching State III* $V_Q(III)$ are expressed in (45):

$$\begin{cases} V_Q(II) = V_{C3} = \dfrac{M_{DCM}+2}{3} V_{in} \\ V_Q(III) = V_{in} \end{cases} \tag{45}$$

The voltage stress across any of the three diodes during *Switching State II* $V_D(II)$ *is null,* while during *Switching State I* $V_D(I)$ and *Switching State III* $V_D(III)$ are shown in (46):

$$\begin{cases} V_D(I) = V_{C3} = \dfrac{M_{DCM}+2}{3} V_{in} \\ V_D(III) = V_{C2} = \dfrac{M_{DCM}-1}{3} V_{in} \end{cases} \tag{46}$$

8) Current Stress Analysis

Figure 4.6 depict the currents flowing through the semiconductor devices of the proposed converter in DCM. The peak currents flowing through *Q*, and the diodes, $i_{Q(Peak)}$, and $i_{D(Peak)}$, respectively, are expressed as shown in (47):

$$\begin{cases} i_{Q(Peak)} = \Delta i_{L1} + \Delta i_{L2} + \Delta i_{L3} = \dfrac{dV_{in}}{f_s L_{eq}} \\ i_{D(Peak)} = \dfrac{1}{3}(\Delta i_{L1} + \Delta i_{L2} + \Delta i_{L3}) = \dfrac{dV_{in}}{3 f_s L_{eq}} \end{cases} \tag{47}$$

The rms currents of the power switch and diodes are expressed in (48):

$$\begin{cases} i_{Q(rms)} = \dfrac{dV_{in}}{f_s L_{eq}} \sqrt{\dfrac{d}{3}} \\ i_{D(rms)} = \dfrac{dV_{in}}{3 f_s L_{eq}} \sqrt{\dfrac{d_x}{3}} \end{cases} \tag{48}$$

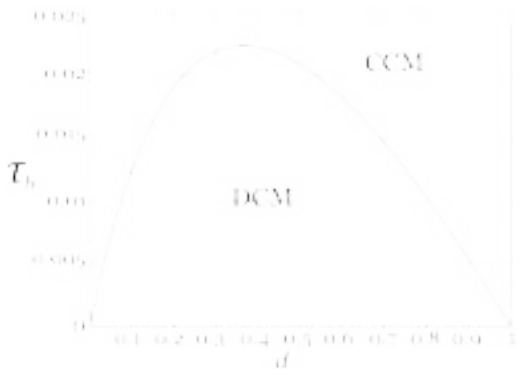
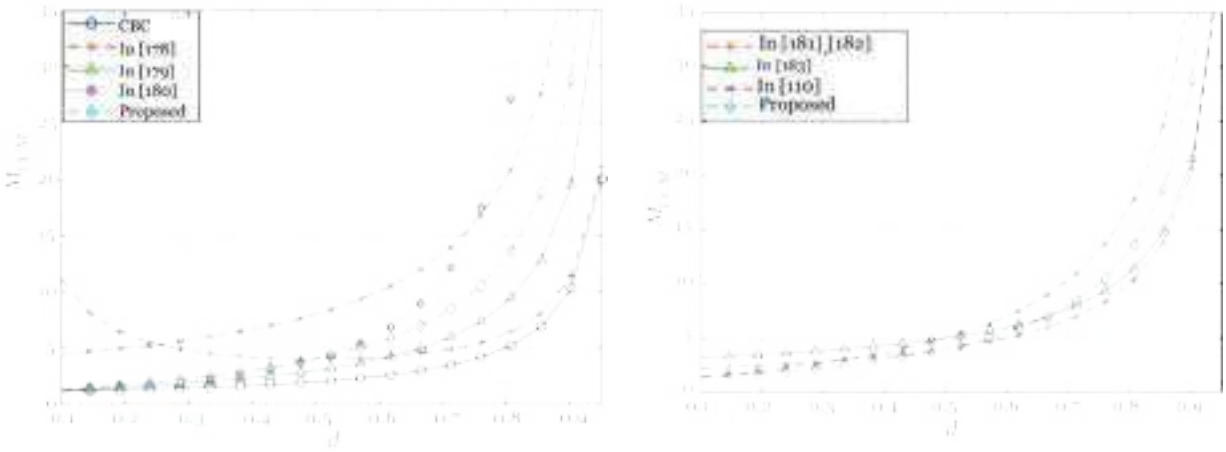


Figure 4.7: Boundary condition of the proposed converter.

4.4 Comparative Study with Other Step-Up Converters

In this section, the proposed converter is compared with other non-isolated step-up converters. The static voltage gain, the normalized voltage stress across the semiconductor devices, components counts, and the voltage gain range of these converters are summarized in Table 4.2. Figure4.8 shows M_{CCM} versus d for the compared converters, while Figure 4.9 and Figure 4.10 show the maximum normalized voltage stress across the power switches and diodes, respectively, among the compared converters.

In order to properly compare the added weight and size of the capacitors and inductors used in each topology of the compared converters, the energy stored in inductors (E_L) and the energy stored in capacitors (E_C) are calculated for each converter in Table 4.2 at the same output power, switching frequency, output voltage, voltage gain, and specific percentage of ripple current in inductors and ripple voltage in capacitors.



(a) (b)

Figure 4.8: Comparison of voltage gain M_CCM versus duty cycle d. (a) Between the proposed converter, conventional boost converter, converters in [179], [180], and [178]. (b) Between the proposed converter, converters in [181], [182], [33], and [110].

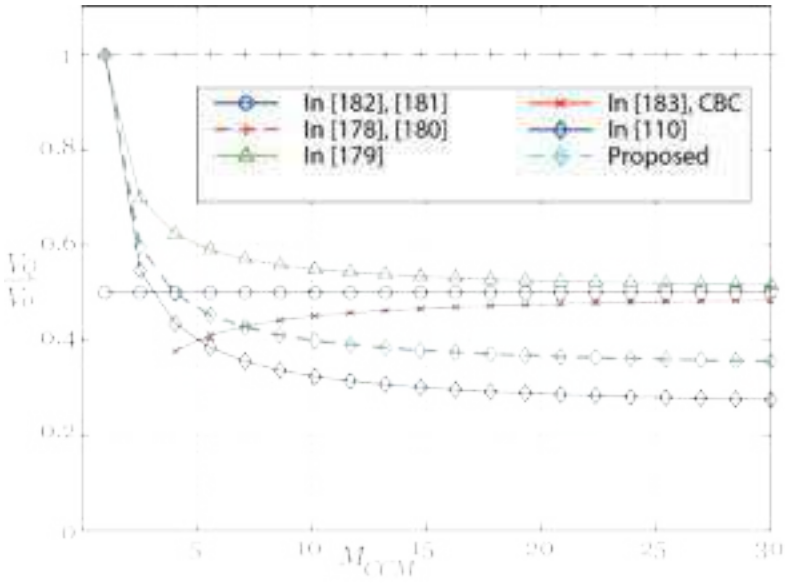


Figure 4.9: Normalized maximum voltage stress across the power switches in the compared converters

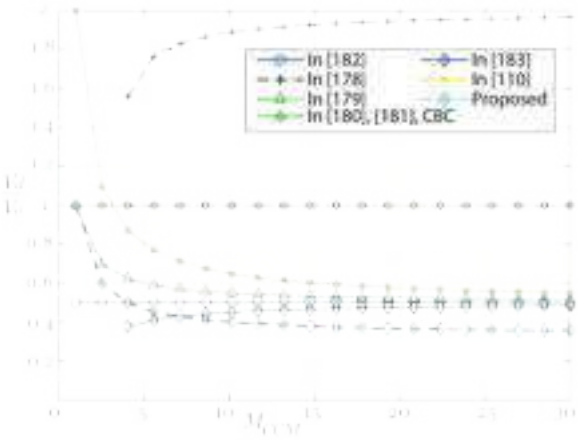


Figure 4.10: Normalized maximum voltage stress across the diodes in the compared converters

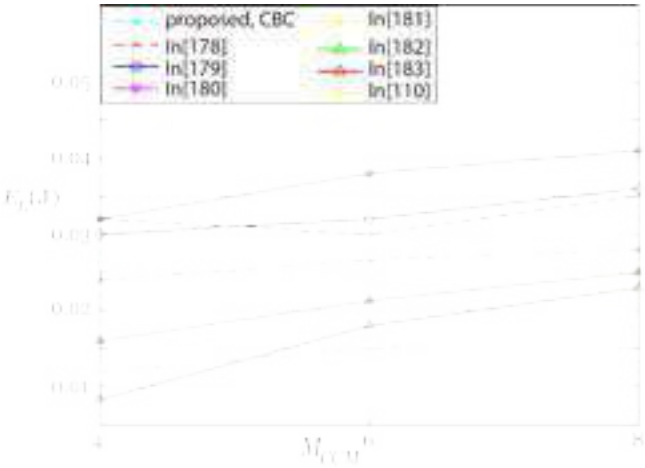


Figure 4.11: Stored energy in the inductors of the compared converters at different voltage gain values.

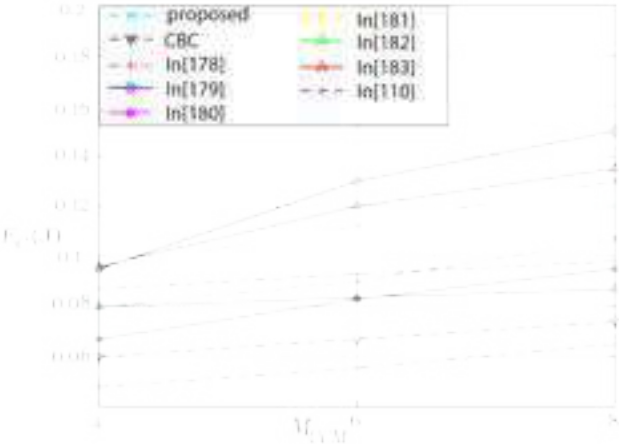


Figure 4.12: Stored energy in the capacitors of the compared converters at different voltage gains.

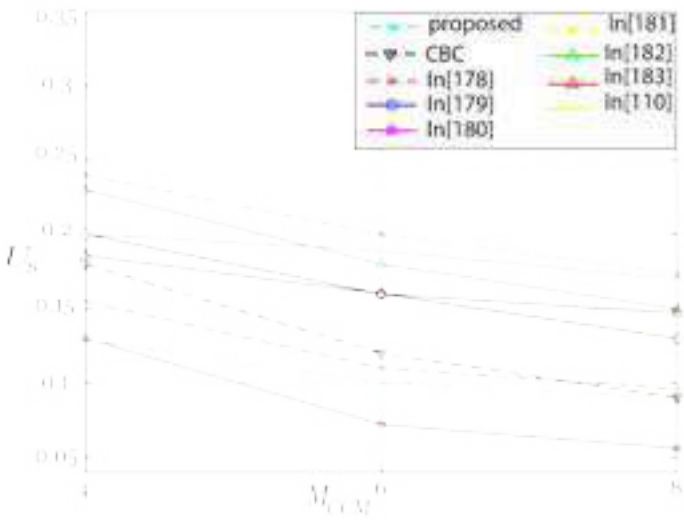


Figure 4.13: Semiconductor utilization factor of the compared converters at different voltage gain values.

The stored energy in the inductors of a converter can be calculated by (49), where d_M is the value of duty cycle at the specific voltage gain, $\Delta_L\%$ is the percentage of ripple current, V_{Li} is the voltage across inductor L_i when the main switch is on, and I_{Li} is the dc current flowing in inductor L_i.

$$E_L = \sum \frac{L_i \, I_{Li}^2}{2} = \sum \frac{I_{Li}}{2} \left(\frac{d_M \, V_{Li}}{\Delta_L\% \; f_s} \right) \tag{49}$$

The stored energy in the capacitors of a converter can be calculated by (50), where $\Delta_C\%$ is the percentage of ripple voltage, i_{Ci} is the current of capacitor C_i when the main switch is on, and V_{Ci} is the dc voltage of capacitor C_i.

$$E_C = \sum \frac{C_i \, V_{Ci}^2}{2} = \sum \frac{V_{Ci}}{2} \left(\frac{d_M \, i_{Ci}}{\Delta_C\% \; f_s} \right) \tag{50}$$

In order to compare the estimated cost of the semiconductor devices used in the converters in Table 4.2, the utilization factor of these semiconductor devices (U_S) is used, and it is defined as given in (51):

$$U_S = \frac{P_o}{\sum V_{Ki}\, I_{Ki\,(rms)}} \tag{51}$$

Table 4.2: COMPARISON BETWEEN THE PROPOSED AND OTHER STEP-UP DC-DC CONVERTERS

Topology	Voltage gain (M)	V_Q / V_o	V_D / V_o	Semiconductor devices	Inductors & Capacitors	Input current	Common ground	Voltage gain range d : 0 →0.9
CBC	$\frac{1}{1-d}$	1	1	1 Switches 1 Diodes	1 Inductor 1 Capacitors	Continuous	*No*	1→10
In [178]	$\frac{1}{d(1-d)}$	$\frac{1}{2}+\sqrt{\frac{1}{4}-\frac{1}{M_{CCM}}}$, 1	$\frac{1}{2}+\sqrt{\frac{1}{4}-\frac{1}{M_{CCM}}}$, $\frac{3}{2}+\sqrt{\frac{1}{4}-\frac{1}{M_{CCM}}}$	2 Switches 3 Diodes	2 Inductors 2 Capacitors	Continuous	*No*	-- →11
In [179]	$\frac{1+d}{1-d}$	$\frac{1+M_{CCM}}{2M_{CCM}}$	$\frac{1+M_{CCM}}{2M_{CCM}}$	1 Switch 3 Diodes	2 Inductors 3 Capacitors	Pulsating	*Yes*	1→19
In [180]	$\frac{1}{(1-d)^2}$	1	1, $\sqrt{1-\frac{M_{CCM}-1}{M_{CCM}}}$, 1-$\sqrt{1-\frac{M_{CCM}-1}{M_{CCM}}}$	1 Switch 3 Diodes	2 Inductors 2 Capacitors	Pulsating	*Yes*	1→100
In [181]	$\frac{2}{1-d}$	$\frac{1}{2}$	$\frac{1}{2}$, 1	2 Switches 2 Diodes	2 Inductors 2 Capacitors	Pulsating	*No*	2→20
In [182]	$\frac{2}{1-d}$	$\frac{1}{2}$	$\frac{1}{2}$	1 Switch 3 Diodes	1 Inductor 3 Capacitors	Continuous	*Yes*	2→20
In [183]	$\frac{3-d}{1-d}$	$\frac{M_{CCM}-1}{2M_{CCM}}$	$\frac{M_{CCM}-1}{2M_{CCM}}$	1 Switch 4 Diodes	1 Inductor 4 Capacitors	Pulsating	*No*	3→21
In [110]	$\frac{1+3d}{1-d}$	$\frac{3+M_{CCM}}{4M_{CCM}}$	$\frac{3+M_{CCM}}{2M_{CCM}}$	2 Switches 2 Diodes	3 Inductors 3 Capacitors	Pulsating	*No*	1→37
Proposed	$\frac{1+2d}{1-d}$	$\frac{2+M_{CCM}}{3M_{CCM}}$	$\frac{2+M_{CCM}}{3M_{CCM}}$	1 Switch 3 Diodes	3 Inductors 5 Capacitors	Continuous	*Yes*	1→28

Where V_{Ki} is the voltage stress on a semiconductor device K_i, and $I_{Ki\,(\mathrm{rms})}$ is the rms value of the current stress on semiconductor device K_i. Figure 4.11, Figure 4.12, and Figure 4.13 show the energy stored in inductors and capacitors and the semiconductor utilization factor

for the compared converters in Table 4.2, respectively, when V_o = 400V, P_o = 1.6kW, f_s = 100kHz, Δ_L% = 25%, Δ_C% = 10% (for the output capacitors) and 20% (for the middle capacitors), and $M_{CCM} = 4 \rightarrow 8$.

Comparing the proposed converter with the conventional boost converter (CBC), on one hand, the CBC has lower number of diodes and passive components, on the other hand, the proposed converter has higher voltage gain, lower voltage stress on the semiconductor devices, and wider voltage gain range. The converter in [178], is composed of less number of inductors and capacitors, however, it utilizes an extra power switch compared to the proposed converter, does not have a common ground and has a high voltage stress on the output diode. Additionally, the converter in [178] has a narrower voltage gain range and its voltage gain is less compared to the proposed converter for $d > 0.5$. In [179], the voltage lift-based converter has the same number of semiconductor devices, and utilizes less capacitors and less inductors compared to the proposed converter. Nevertheless, the converter in [179] has high input current ripple, narrower voltage gain range, less voltage gain, and higher voltage stress on its power switch and diodes compared to the proposed converter. The quadratic converter presented in [180], on one hand has higher voltage gain and less number of inductors and capacitors compared to the proposed converter, and on the other hand it has high input current ripple and higher voltage stress on the power switch. In [181], converter II, on one side has double the voltage gain of the conventional boost converter and utilizes less number of diodes, inductors, and capacitors compared to the proposed converter, but on the other side, it utilizes an extra power switch compared to the proposed converter, has a pulsating input current, does not have a common ground, and the voltage stress on its output diode is high. The voltage gain of the proposed converter is higher for $d > 0.5$, and the voltage stress on the

semiconductor devices of the proposed converter is less for $d > 0.5$, compared to the converter II in [181]. The boost converter that utilizes diode-capacitor voltage multipliers in [182] has less inductors compared to the proposed converter, however, to increase its voltage gain, the number of diodes of the voltage multipliers duplicates, leading to increased conduction losses and decreased efficiency. Additionally, as the number of voltage multipliers increases, the minimum boosting gain increases, rendering it not sufficient for applications with wide voltage fluctuations such as fuel cells. Comparing the hybrid boost converter in [183] with the proposed converter, the number of inductors and capacitors in the converter in [183] is less, while it utilizes an extra diode. The input current ripple of the converter in [183] is high which can affect the life time of the fuel cell. Additionally, the proposed converter has higher voltage gain for $d > 0.65$, and less voltage stress on the semiconductor devices for $M_{CCM} > 7$ compared to the converter in [183]. The converter presented in [110] has less capacitors, less diodes, and an extra power switch compared to the proposed converter. Also, it has a wider voltage gain range, and less voltage stress on the semiconductor devices. The main drawbacks of this converter are the higher number of power switches, the pulsating input current and the lack of common ground between its input and output ports, as the potential difference between the two grounds is high frequency PWM voltage which can increase the EMI and requires more maintenance.

Based on Figure 4.11, the energy stored in the inductors of the proposed converter is the same as the CBC, while it is lower than that of the converters in [178]-[180], and is higher than that of the converters in [181], [110], [183], and [182]. This means that the estimated weight and size of inductors for the proposed converter is close to that of the CBC while it is lower than that of the converters in [178]-[180], and is higher than that of the converters in

[181]-[183], and [110]. Similarly, based on Figure 4.12, the energy stored in the capacitors of the proposed converter is lower than that of the converters in [179], [181], [183] and [178] (when $M_{CCM} < 6.5$), while it is higher than that of the CBC and the converters in [180], [182], and [110]. This means that the estimated weight and size of capacitors for the proposed converter is lower than that of the converters in [179], [181], [183], and [178] (when $M_{CCM} < 6.5$), and is higher than that of the converters in [180], [182], and [110]. Figure 4.13 shows that the proposed converter has the highest utilization factor compared to all the converters in Table 4.2, which means that the estimated cost of the semiconductor devices of the proposed converter is lower than that of the other compared converters.

From the above comparisons, it is evident that the proposed converter integrates many advantages such as: high conversion ratio, wide voltage gain range, low voltage stress on the semiconductor devices, common ground between its input and output ports, low input current ripple, and utilizes a single power switch. This makes it an excellent candidate for fuel cell vehicles application.

4.5 Design Considerations and Components Selection

4.5.1 Semiconductor Devices Selection

By knowing the maximum value of M_{CCM} (max) needed by the converter, and the maximum output load current, the peak currents flowing through the power switch and diodes can be calculated using (24) and (25), respectively. From (12), the maximum voltage stress on the power switch and diodes can be calculated when M_{CCM} (max) is known. These maximum voltage and current stresses should be within the safe operating area (SOA) of the selected power switch and diodes.

4.5.2 Inductors Design

By knowing the maximum output load current and by means of (13) and (14), the currents flowing through the three inductors can be calculated. Assuming the maximum ripple currents Δi_{L1}, Δi_{L2}, and Δi_{L3} are known. The minimum required inductances can be determined using (52).

$$\begin{aligned} L_1 &\geq \frac{dV_{in}}{f_s \Delta i_{L1}} \\ L_2 &\geq \frac{dV_{in}}{f_s \Delta i_{L2}} \\ L_3 &\geq \frac{dV_{in}}{f_s \Delta i_{L3}} \end{aligned} \tag{52}$$

4.5.3 Capacitors Design

By means of (7)-(9), the voltages across the five capacitors can be calculated. Assuming the maximum ripple voltages ΔV_{C1}, ΔV_{C2}, ΔV_{C3}, ΔV_{C4} and ΔV_{Co} are known. The minimum required capacitances can be determined using (53).

$$\begin{aligned} C_1 &\geq \frac{2I_o d}{f_s \Delta V_{C1}} \\ C_2 &\geq \frac{I_o d}{f_s \Delta V_{C2}} \\ C_3 &\geq \frac{2I_o d}{f_s \Delta V_{C3}} \end{aligned} \quad , \quad \begin{aligned} C_4 &\geq \frac{I_o d}{f_s \Delta V_{C4}} \\ C_o &\geq \frac{I_o d}{f_s \Delta V_{Co}} \end{aligned} \tag{53}$$

4.6 Experimental Results and Analysis

In order to validate the theoretical analysis of the proposed converter, a scaled-down 1.6kW laboratory prototype was built, presented in Figure 4.14. The input voltage to the converter is depicted by an adjustable dc power supply, and the converter is controlled by a microcontroller TMS320f28377s.

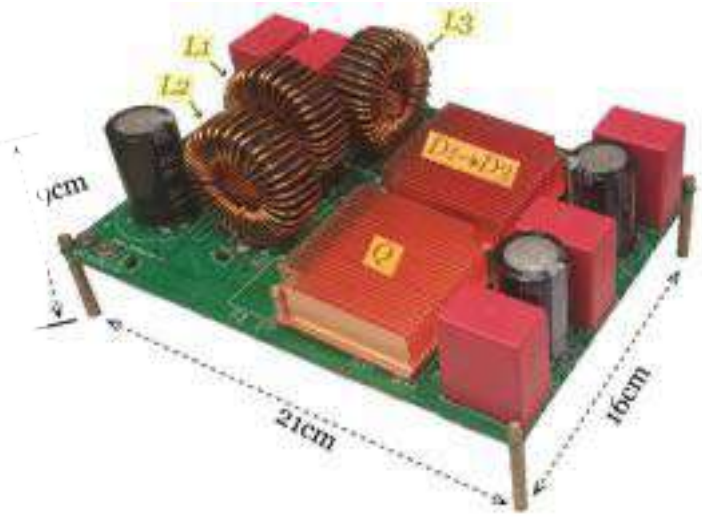


Figure 4.14: Experimental prototype.

Table 4.3: EXPERIMENT PARAMETERS

Parameters and Components	Values
Rated power P_o	1.6 kW
Output voltage V_o	400V
Power MOSFET Q	IXFP72N30X3M
Power Diodes D_1, D_2, D_3	MBRF40250TG
Inductors L_1, L_2, L_3	250 µH
Capacitors C_1, C_2	40 µF
Capacitors C_3, C_4	220 µF
Capacitor C_o	240 µF
Switching frequency f_s	100 KHz
Load R	100Ω
Microcontroller	TMS320f28377s

The power circuit is built using (IXFP72N30X3M) power MOSFET and (MBRF40250TG) Schottky diodes. The values of inductors and capacitors used in the developed prototype are as following: $L_1 = L_2 = L_3 = 250$ µH, $C_1 = C_2 = 40$ µF, $C_3 = C_4 = 220$

μF, and C_o = 240 μF. In addition, the load R = 100Ω, and switching frequency f_s = 100 KHz. The case study investigated in this section is V_{in} = 50V, and the duty cycle d = 0.7.

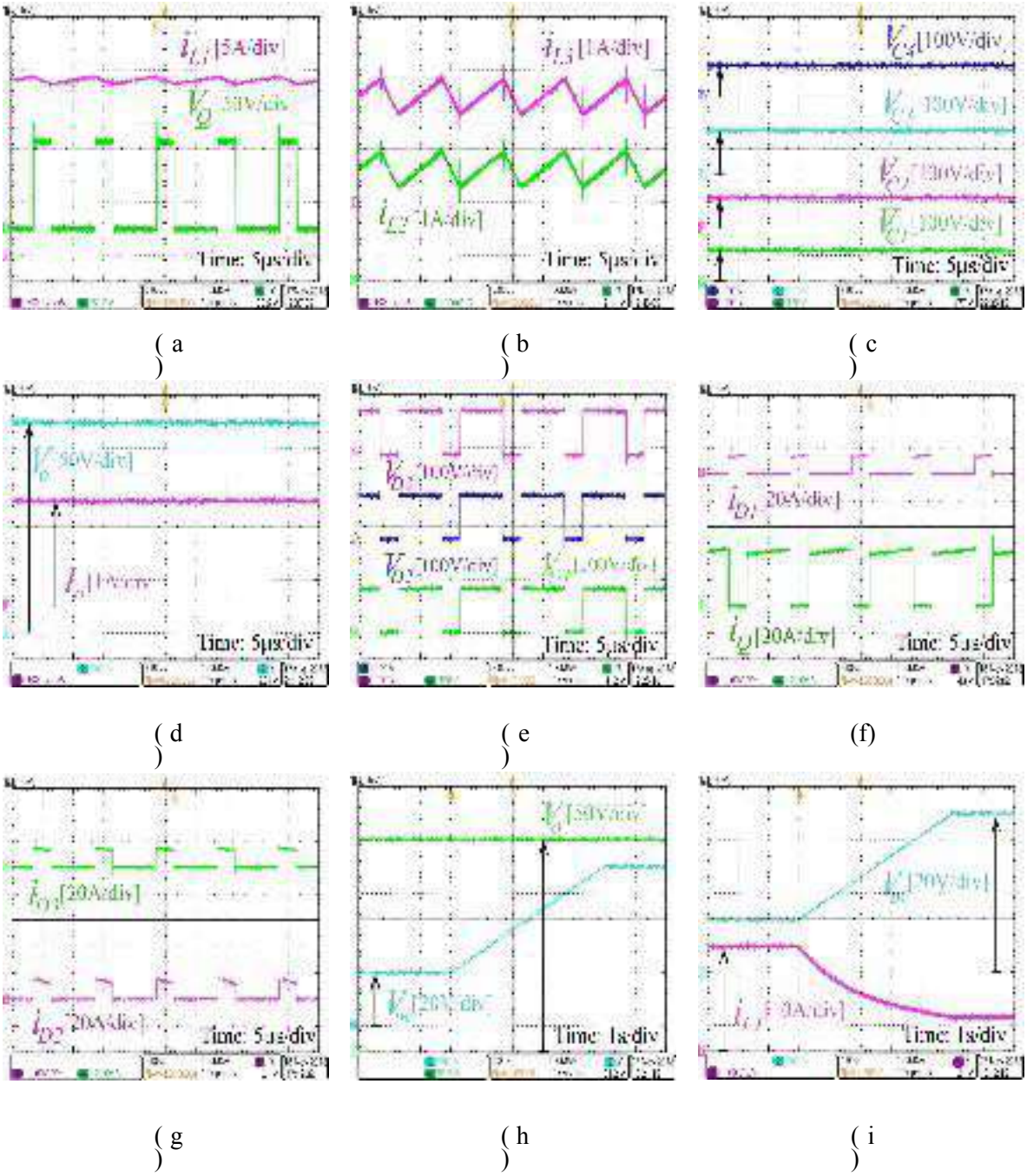
According to equations (7)-(9), the voltages across the five capacitors can be calculated as following: $V_{C1} = V_{C2} = V_{C4} \approx 116.7$V, $V_{C3} \approx 166.7$V, and $V_o \approx 400$V, which closely agree with the experimental results in Figure 4.15(c) and Figure 4.15(d).

The output current can be theoretically calculated as: $I_o = {}^{V_o}/_{R} = 4$A, which agrees with the experimental result shown in Figure 4.15(d). Accordingly, the currents of the three inductors can be calculated using (13) and (14), as following: $I_{L2} = I_{L3} = I_o = 4$A, and $I_{L1} = 32$A, which closely agree with the experimental results shown in Figure 4.15(a) and Figure 4.15(b). Additionally, the ripple currents of the three inductors can be calculated using (52), as following: $\Delta i_{L1} = \Delta i_{L2} = \Delta i_{L3} = 1.4$A, which comply with the experimental results presented in Figure 4.15(a) and Figure 4.15(b).

The voltage stresses across the power switch and the three diodes can be calculated using equation (11), as following: $V_Q = V_{D1} = V_{D2} = V_{D3} \approx 166.7$V, which closely comply with the experimental results given in Figure 4.15(a) and Figure 4.15(e). The current stresses on the power switch and the three diodes can be derived via equations (20) and (21), as following: $i_Q = 40$A, and $i_{D1} = i_{D2} = i_{D3} \approx 13.3$A, which closely agree with the experimental results shown in Figure 4.15(f) and Figure 4.15(g).

In order to test the wide-input feature of the proposed converter, Figure 4.15(h) shows the input voltage of proposed converter changed from 40V to 120V, while the output voltage is fixed at 400V. In this test, the converter is controlled by a closed-loop proportional-integral (PI) voltage controller. Figure 4.15(i) shows the effect of the change in the input voltage from 40V to 120V on the input current (current flowing in L_1) and it shows that I_{L1} =

40A when V_{in} = 40V, while $I_{L1} \approx$ 13.3A when V_{in} = 120V, as I_{L1} is directly proportional to the voltage gain of the converter (when the output current is constant).

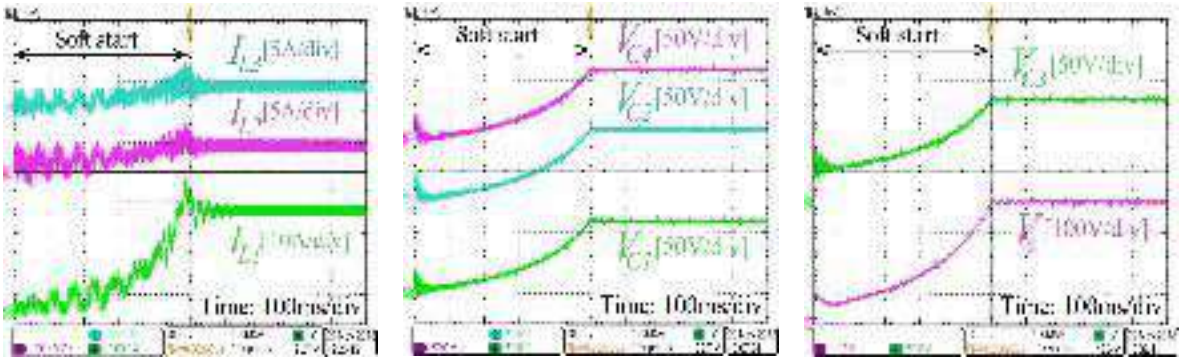


(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 4.15: Experimental results. (a) Current of L1, and voltage stress across Q, (b) Currents of L2 and L3, (c) Voltages across C1, C2, C3, and C4, (d) Output voltage and output current, (e) Voltage stresses across D1, D2, and D3, (f) Current stresses of Q and D1



(a) (b) (c)

Figure 4.16: (a) Inductor currents during start-up, (b) Voltages across C1, C2, and C4 during start-up, (c) Voltages across C3 and Co during stat-up.

The results given in Figure 4.15(h) and Figure 4.15(i) show evidently that the proposed converter has an acceptable dynamic performance under wide changes in its input voltage.

In order to build the initial voltages across the capacitors of the proposed converter without having high inrush currents that may damage the semiconductor devices, a soft-starting algorithm is adopted. This soft-starting algorithm gradually increases the value of duty cycle from zero to the desired value during the starting instant. Figure 4.16 shows the currents of the three inductors and the voltages of the five capacitors during the soft start and during steady state. Based on these results, the converter appears to not have high inrush inductor currents during the start instant, and the capacitor voltages increase gradually without having high voltage overshoots during the start instant. The calculated loss distributions for the investigated case study of the experiment is presented in Figure 4.17. The total losses of this case study$P_{Loss} = 73.88\text{W}$, and it is distributed as following: The conduction losses of D_1, D_2, and D_3 are 14.4W and they account for 19% of the total losses of the converter, the conduction loss of Q is 21.28W and it accounts for 29% of the total converter losses, the switching loss of Q is 13.11W and it accounts for 18% of the total converter losses, the conduction losses of L_1, L_2, and L_3 are 16.88W and they account for 23% of the total converter

losses, and finally, the conduction losses of C_1, C_2, C_3, C_4, and C_o are 8.21W and they account for 11% of the total converter losses.

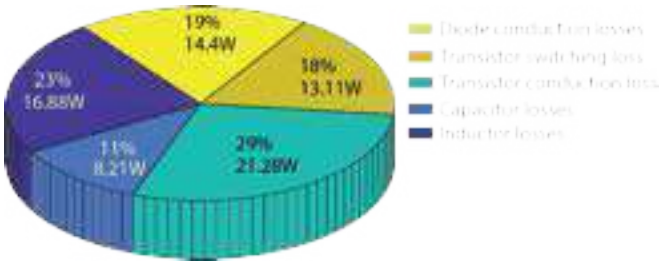


Figure 4.17: Calculated power loss distributions for the experiment (Vin = 50V, Vo = 400V, and R = 100Ω).

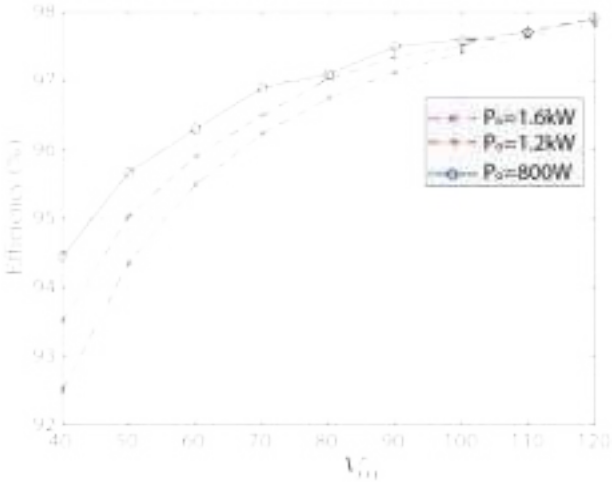


Figure 4.18: Efficiency curves of the proposed converter (Vo=400V, Vin=40→120V, output power=800W, 1200W, and 1600W).

The conduction and switching losses of Q are low due to the utilization of low voltage power MOSFET with low R_{DS} and low C_{OSS}. The efficiency curves of the laboratory prototype at different values of V_{in} (V_{in} = 40 → 120), and different output powers (P_o = 800W, 1200W, and 1600W), while keeping V_o fixed at 400V, are shown in Figure 4.18. The measured efficiency curves are obtained using a power analyzer (Tektronix PA3000). The maximum recorded efficiency is 97.8%, when P_o = 800W and V_{in} = 120V, while the minimum recorded efficiency is 92.5%, when P_o = 1600W and V_{in} = 40V.

4.7 Conclusion

In this chapter, a new single-switch dc-dc converter with an integrated $L^2C^3D^2$ network is presented. The proposed converter has many merits such as: high voltage gain without magnetic coupling, low voltage stress on the semiconductor devices, common ground, and universal input voltage. These features make it an excellent candidate for fuel cell vehicles. Steady-state analyses in CCM and DCM operations of the proposed converter were discussed. The proposed converter is compared with other step-up converters in literature regarding the voltage gain, the voltage stress on the semiconductor devices, the number of components, and other specifications, and the privilege of the proposed topology is justified. Finally, a 1.6 kW 400V prototype for the proposed topology was built, and the theoretical analysis was verified by the experimental results.

Chapter 5 A New Single-Switch Structure of a DC-DC Converter with Wide Conversion Ratio for Fuel Cell Vehicles: Analysis and Development

5.1 Introduction

In this chapter a new single-switch transformerless boost dc-dc converter is proposed for fuel cell vehicles. The developed topology utilizes a switched-capacitor multiplier and an integrated LC^2D output network in order to enhance the voltage gain of the converter and reduce the voltage stress on the power switch. In addition, the proposed converter has a wide voltage gain range to suit the wide voltage swings of the fuel cell. The operating principles and the steady-state analyses of the proposed converter when it operates in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are illustrated in this paper. Additionally, the dynamic modeling and the compensator design for the developed converter are discussed. A scaled-down 800 V, 1.3 kW experimental prototype was built using a Gallium Nitride (GaN) transistor and Silicon Carbide (SiC) diodes to validate the theoretical analyses of the proposed converter.

5.2 Structure and Steady-State Analysis of the Proposed Converter

5.2.1 The Proposed Topology

The schematic of the proposed converter is shown in Figure 5.1, where it is composed of one switch (Q), four diodes (D_1, D_2, D_3, and D_4), two inductors (L_1, and L_2), five capacitors (C_1, C_2, C_3, C_4, and C_5), and the load is represented by a resistance (R). The proposed topology is based on a two-level boost switching network, an integrated switched capacitor multiplier, and an integrated LC^2D output network. The integrated switched capacitor multiplier and the LC^2D output network enhance the voltage gain of the converter and reduce the voltage stress on the switch, hence, a

switch with lower rated voltage (= lower on resistance, lower total charge, and higher efficiency) can be used.

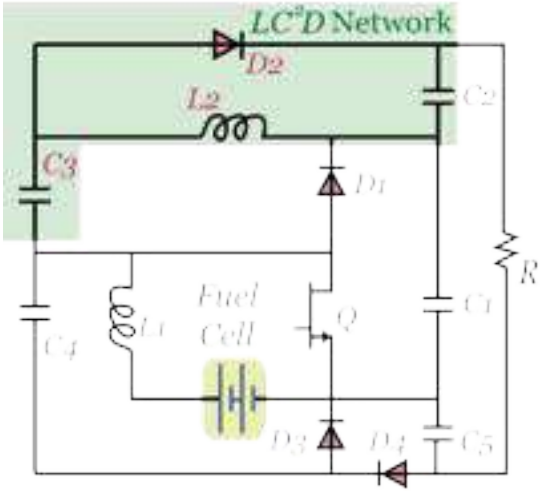


Figure 5.1: The proposed step-up converter.

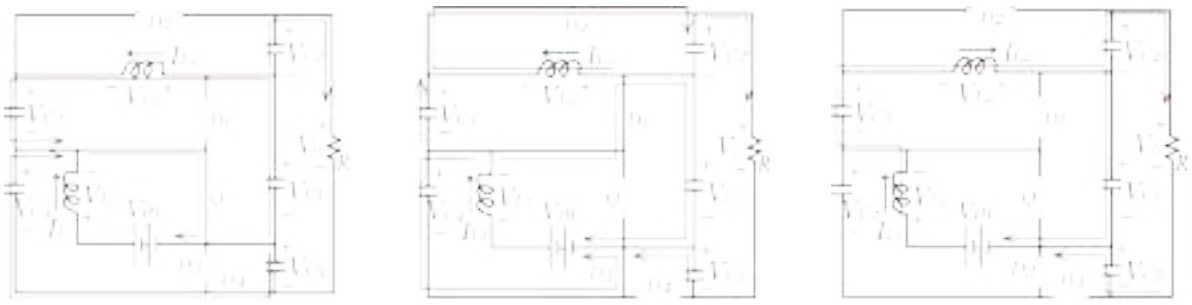
5.2.2 Operating States Analysis

Based on the conduction state of the switch and the four diodes, the operation of the proposed converter can be classified into three operating states, presented in Table 5.1. The analyses of the converter during the three switching states refer to the currents of the five capacitors ($C_1 \rightarrow C_5$) during charging as: i_{C1_ch}, i_{C2_ch}, i_{C3_ch}, i_{C4_ch}, and i_{C5_ch}, and during discharging as: i_{C1_dis}, i_{C2_dis}, i_{C3_dis}, i_{C4_dis}, and i_{C5_dis}. Also, in these analyses the currents of inductors (L_1 and L_2) are referred to as I_{L1} and I_{L2}, the voltages of the five capacitors are referred to as V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5}, and the input and output voltages and the output current are referred to as V_{in}, V_o, and I_o, respectively.

In order to simplify the analysis, the following assumptions were made: 1) The ripple currents of inductors (L_1 and L_2) equal zero. 2) The ripple voltages of the five capacitors ($C_1 \rightarrow C_5$) equal zero. 3) The inductors and capacitors are ideal with no equivalent series resistances. 4) The switch and diodes are ideal.

Table 5.1: OPERATING STATES OF THE SEMICONDUCTOR DEVICES

Operating State	Q	D_1	D_2	D_3
I (CCM & DCM)	ON	OFF	OFF	OFF
II (CCM & DCM)	OFF	ON	ON	ON
III (DCM)	OFF	OFF	OFF	OFF



(a) (b) (c)

Figure 5.2: Current flow paths during the three operating states. (a) Operating state I. (b) Operating state II. (c) Operating state III.

9) **Operating State I:**

In this mode, the switch is on, $D_1 \rightarrow D_3$ are reverse biased, and D_4 is forward biased. This operating state is for the converter when it operates in CCM and DCM, and the period of this state is dT, where d is the duty cycle and T is the periodic switching time. Figure 5.3 shows the important waveforms of the proposed converter when it operates in CCM and DCM, and the converter is in operating state *I* when $t_0 < t < t_1$.

During this state, both inductors charge, capacitors (C_3 and C_5) charge, and capacitors (C_1, C_2, and C_4) discharge. The current flow paths during this operating state are shown in Figure 5.2(a). By means of Kirchhof's Current Law (KCL), and Kirchhof's Voltage Law (KVL) on the equivalent circuit shown in Figure 5.2(a), we can deduce (1) and (2):

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C1} - V_{C3} \end{cases} \quad (1)$$

$$\begin{cases} I_{C1\_dis} = 2I_{L2} \\ I_{C2\_dis} = \dfrac{V_o}{R} \\ I_{C3\_ch} = I_{L2} \\ I_{C5\_ch} = I_{C4\_dis} - \dfrac{V_o}{R} \end{cases} \quad (2)$$

10) **Operating State II:**

In this mode, the switch is off, $D_1 \rightarrow D_3$ are forward biased, and D_4 is reverse biased. This operating state is for the converter when it operates in CCM and DCM, and the period of this state is (1-*d)T* (in CCM) or d_eT (in DCM). These time internals are shown in Figure 5.3, and the converter is in operating state *II* when $t_1 < t < t_2$.

During this state, both inductors discharge, capacitors (C_3 and C_5) discharge, and capacitors (C_1, C_2, and C_4) charge. The current flow paths during this operating state are shown in Figure 5.2(b). By means KCL and KVL laws on the equivalent circuit shown in Figure 5.2(b), we can deduce (3) and (4):

$$\begin{cases} V_{L1} = V_{in} - V_{C4} = V_{in} - V_{C1} \\ V_{L2} = -V_{C3} = -V_{C2} \end{cases} \quad (3)$$

$$\begin{cases} I_{L1} = I_{C4\_ch} + I_{C3\_ch} + I_{L2} + I_{C1\_ch} - I_{C2\_ch} \\ I_{C5\_dis} = \dfrac{V_o}{R} \end{cases} \quad (4)$$

11) **Operating State III:**

In this mode the switch is off, and $D_1 \rightarrow D_4$ are reverse biased. This operating state is for the converter when it operates only in DCM, and the period of this state is $(1 - d - d_e)T$. The converter is in operating state *III* when $t_2 < t < t_3$. In this operating state, the voltages across L_1 and

L_2 equal zero, a positive constant current I_{L1_III} flows through L_1, and a negative constant current I_{L2_III} flows through L_2. The relationship between I_{L1_III} and I_{L2_III} is presented in (6) where their summation equals null.

$$\begin{cases} V_{L1} = 0 \\ V_{L2} = 0 \end{cases} \tag{5}$$

$$I_{L1\_III} + I_{L2\_III} = 0 \tag{6}$$

5.3 Steady-State Analysis for CCM Operation

In CCM operation, the converter has two states of operation, namely: operating state *I* and operating state *II*, and the important waveforms of this operation is presented in Figure 5.3(a). The voltage gain, the voltage and current stresses on the semiconductor devices, and the efficiency analysis of the proposed converter are deduced in this subsection.

5.3.1 Voltage Gain

By using the voltage second balance on L_1 and L_2 we can extract the output voltage, and the voltages of the five capacitors, as following:

$$\frac{1}{T}\left(\int_0^{dT} V_{in}dt + \int_{dT}^{T} (V_{in} - V_{C1})dt\right) = 0 \tag{7}$$

$$\frac{1}{T}\left(\int_0^{dT} V_{in}dt + \int_{dT}^{T} (V_{in} - V_{C4})dt\right) = 0 \tag{8}$$

$$\frac{1}{T}\left(\int_0^{dT} (V_{C1} - V_{C3})dt - \int_{dT}^{T} V_{C2}dt\right) = 0 \tag{9}$$

$$\frac{1}{T}\left(\int_{0}^{dT}(V_{C1}-V_{C3})dt-\int_{dT}^{T}V_{C3}dt\right)=0 \tag{10}$$

By solving equations (7)-(10), we can deduce the following relationships:

$$\begin{cases} V_{C1}=V_{C4}=V_{C5}=\frac{V_{in}}{(1-d)} \\ V_{C2}=V_{C3}=\frac{d\,V_{in}}{(1-d)} \\ V_o=\frac{2+d}{1-d}\,V_{in} \end{cases} \tag{11}$$

Hence, the voltage gain *M* can be calculated as following:

$$M=\frac{2+d}{1-d} \tag{12}$$

5.3.2 Voltage Stresses on Semiconductor Devices

The voltage stresses on the switch (V_Q) and all the diodes (V_{D1}, V_{D2}, V_{D3}, and V_{D4}) equal V_{C1} and are depicted by (13):

$$V_Q=V_{D1}=V_{D2}=V_{D3}=V_{D4}=V_{C1}=\frac{V_{in}}{(1-d)} \tag{13}$$

By using (12) and (13), these voltage stresses can be presented in a normalized form as a function of V_O and *M* as shown in (14):

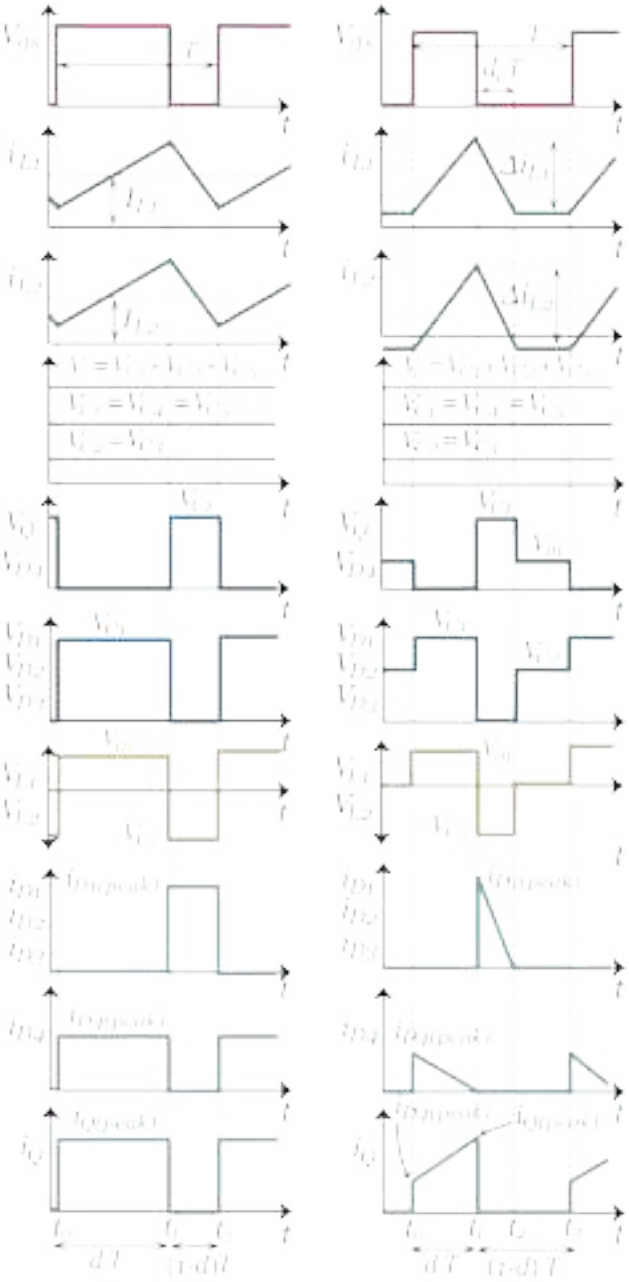
$$V_Q=V_{D1}=V_{D2}=V_{D3}=V_{D4}=V_{C1}=\frac{1+M}{3M}\,V_o \tag{14}$$

5.3.3 Current Stresses on Semiconductor Devices

Assuming a lossless operation where the input power equals the output power (i.e. $V_{in} \times I_{L1} = V_o \times I_o$), hence, I_{L1} and I_{L2} can be calculated as in (15) and (16):

$$I_{L2}=I_o=\frac{V_o}{R} \tag{15}$$

$$I_{L1}=MI_{L2}=\frac{(2+d)V_o}{(1-d)R}=\left(\frac{2+d}{1-d}\right)^2\frac{V_{in}}{R} \tag{16}$$



(a) (b)

Figure 5.3: Key waveforms of the proposed converter. (a) CCM operation. (b) DCM operation.

By using the charge-second balance rule on $C_1 \rightarrow C_5$ to extract their charging and discharging currents, as shown in (17)-(22):

$$\begin{cases} i_{C1\_dis} \times dT = i_{C1\_ch} \times (1-d)T \\ i_{C2\_dis} \times dT = i_{C2\_ch} \times (1-d)T \\ i_{C3\_ch} \times dT = i_{C3\_dis} \times (1-d)T \\ i_{C4\_dis} \times dT = i_{C4\_ch} \times (1-d)T \\ i_{C5\_ch} \times dT = i_{C5\_dis} \times (1-d)T \end{cases} \quad (17)$$

$$\begin{cases} i_{C1\_ch} = 2I_o \dfrac{d}{(1-d)} \\ i_{C1\_dis} = 2I_o \end{cases} \quad (18)$$

$$\begin{cases} i_{C2\_ch} = I_o \dfrac{d}{(1-d)} \\ i_{C2\_dis} = I_o \end{cases} \quad (19)$$

$$\begin{cases} i_{C3\_ch} = I_o \\ i_{C3\_dis} = I_o \dfrac{d}{(1-d)} \end{cases} \quad (20)$$

$$\begin{cases} i_{C4\_ch} = \dfrac{I_o}{(1-d)} \\ i_{C4\_dis} = \dfrac{I_o}{d} \end{cases} \quad (21)$$

$$\begin{cases} i_{C5\_ch} = I_o \dfrac{(1-d)}{d} \\ i_{C5\_dis} = I_o \end{cases} \quad (22)$$

By using equations (15)-(22) and the current flow paths shown in Figure 5.2, the current stress on the switch i_Q and the current stresses on the four diodes ($i_{D1} \rightarrow i_{D4}$) can be extracted as shown in (23)-(27):

$$i_Q = I_{L1} + I_{L2} + i_{C4\_dis} = \frac{1+2d}{d(1-d)} I_o \quad (23)$$

$$i_{D1} = I_{L1} - i_{C4\_ch} - i_{C3\_dis} = \frac{I_o}{(1-d)} \quad (24)$$

$$i_{D2} = I_{L2} + i_{C3\_dis} = \frac{I_o}{(1-d)} \quad (25)$$

$$i_{D3} = i_{C4\_ch} = \frac{I_o}{(1-d)} \quad (26)$$

$$i_{D4} = i_{C4\_dis} = \frac{I_o}{d} \quad (27)$$

By means of (23)-(27), and the current flow paths shown in Figure 5.2, the root-mean-square (rms) values of the currents of the switch and diodes can be calculated as following:

$$i_{Q\_rms} = \frac{1+2d}{\sqrt{d}(1-d)} I_o \tag{28}$$

$$i_{D1\_rms} = i_{D2\_rms} = i_{D3\_rms} = \frac{I_o}{\sqrt{1-d}} \tag{29}$$

$$i_{D4\_rms} = \frac{I_o}{\sqrt{d}} \tag{30}$$

Similarly, the rms values of the five capacitors' currents can be extracted using (18)-(22), as following:

$$i_{C1\_rms} = 2I_o \sqrt{\frac{d}{1-d}} \tag{31}$$

$$i_{C2\_rms} = i_{C3\_rms} = I_o \sqrt{\frac{d}{1-d}} \tag{32}$$

$$i_{C4\_rms} = I_o \sqrt{\frac{1}{d(1-d)}} \tag{33}$$

$$i_{C5\_rms} = I_o \sqrt{\frac{1-d}{d}} \tag{34}$$

5.3.4 Efficiency Analysis

In order to properly select the components and design an adequate cooling system, the power dissipated from the various components should be calculated. Equation (35) calculates the total power loss P_{Loss} of the proposed converter, where P_{L_cond}, P_{L_core}, P_C, P_D, P_{Q_sw}, and P_{Q_cond} are the inductors' conduction losses, the inductors' core losses, the capacitors' conduction losses, the diodes' conduction losses, the switching losses of the switch, and the conduction loss of the switch, respectively.

$$P_{Loss} = P_{L\_cond} + P_{L\_core} + P_C + P_D + P_{Q\_sw} + P_{Q\_cond} \tag{35}$$

The core losses and conduction losses of L_1 and L_2 can be calculated using (36) and (37), respectively, where R_{L1}, R_{L2}, f_s, l_{c1}, l_{c2}, A_{c1}, A_{c2}, ΔB_1, and ΔB_2 are the equivalent series resistances

of L_1 and L_2, the switching frequency, the magnetic flux path lengths of the two inductors' cores, the cross sectional areas of the two inductors' cores, and ac magnetic flux density of L_1 and L_2.

$$P_{L\_core} = l_{c1}\, A_{c1}\left(a\, \Delta B_1^b\, f_s^C\right) + l_{c2}\, A_{c2}\, (a\, \Delta B_2^b\, f_s^C) \tag{36}$$

$$P_{L\_cond} = I_{L1}^2 R_{L1} + I_{L2}^2 R_{L2} \tag{37}$$

Equation (36) is the Steinmetz equation and it is an empirical formula to calculate the core loss of an inductor where a, b, and c are fitting parameters and can be found in the datasheet of the core.

The conduction losses of the five capacitors can be calculated using (38), where $ESR1 \rightarrow ESR5$ are the equivalent series resistances of the five capacitors $C_1 \rightarrow C_5$.

$$\begin{aligned} P_C = {} & I_{C1\_rms}^2 ESR1 + I_{C2\_rms}^2 ESR2 + I_{C3\_rms}^2 ESR3 + I_{C4\_rms}^2 ESR4 \\ & + I_{C5\_rms}^2 ESR5 \end{aligned} \tag{38}$$

The conduction and switching losses of the four diodes can be calculated by (39), where $V_{f1} \rightarrow V_{f4}$ and $Q_{C1} \rightarrow Q_{C4}$ are the forward voltages and capacitive charges of the Schottky diodes $D_1 \rightarrow D_4$, respectively.

$$\begin{aligned} P_D = {} & \left[(1-d)(i_{D1}V_{f1} + i_{D2}V_{f2} + i_{D3}V_{f3}) + d\, i_{D4}V_{f4}\right] \\ & + f_s\left(\frac{V_{in}}{1-d}\right)[Q_{C1} + Q_{C2} + Q_{C3} + Q_{C4}] \end{aligned} \tag{39}$$

The conduction and the switching losses of Q can be calculated using (40) and (41), respectively, where R_{on}, C_{OSS}, t_r, and t_f, are the on resistance, the parasitic output capacitance, the rise and fall times of the switch.

$$P_{Q\_cond} = I_{Q\_rms}^2 R_{on} \tag{40}$$

$$P_{Q\_sw} = 0.5 f_s\left(V_Q i_Q\left(t_r + t_f\right) + C_{OSS} V_Q^2\right) \tag{41}$$

The efficiency η can be calculated as following

$$\eta = \frac{V_o I_{L2}}{V_o I_{L2} + P_{Loss}} \tag{42}$$

5.4 Steady-State Analysis of DCM

When the proposed converter operates in DCM, it has three operating states, namely: operating state *I*, operating state *II*, and operating state *III*. Figure 5.3(b) shows the important waveforms of the proposed converter during DCM operation, where the period of the operating state *I* is dT, the period of the operating state *II* is d_eT, and the period of operating state *III* is $\left(1-(d+d_e)\right)T$. The first two operating states are the same as in CCM, while the additional third operating state is only for DCM operation. The voltage gain of the proposed converter, the boundary operating condition between DCM and CCM, the voltage and current stresses on the semiconductor devices are deduced in this subsection.

5.4.1 Voltage Gain

During DCM, the ripple currents of the two inductors (Δi_{L1} and Δi_{L2}) can be calculated as following:

$$\begin{cases} \Delta i_{L1} = \dfrac{d\,V_{in}}{f_s L_1} \\ \Delta i_{L2} = \dfrac{d\,V_{in}}{f_s L_2} \end{cases} \tag{43}$$

Based on (15), (16), (24)-(26), and (43), the peak current of D_1, D_2, or D_3 can be calculated as following:

$$i_{D1(peak)} = i_{D2(peak)} = i_{D3(peak)} = \frac{\Delta i_{L1} + \Delta i_{L2}}{3} = \frac{d\,V_{in}}{3 f_s\, L_{eq}} \tag{44}$$

$$L_{eq} = \left[\frac{1}{L_1} + \frac{1}{L_2}\right]^{-1} \tag{45}$$

The fraction of the periodic switching time associated with operating state *II* (d_e) can be deduced by equating the average current of D_1, D_2, or D_3 to the output current, as following:

$$\langle i_{D1} \rangle = \frac{1}{T}\left(\frac{d_e\,T}{2}\frac{d\,V_{in}}{3 f_s\, L_{eq}}\right) = \frac{V_o}{R}$$

Hence, d_e can be extracted as shown in (46):

$$d_e = \frac{6\, f_s\, L_{eq}\, V_o}{d\, V_{in}\, R} = \frac{6\, V_o}{d\, V_{in}} K \tag{46}$$

Where *K* is a dimensionless parameter and is defined by (47).

$$K = \frac{f_s\, L_{eq}}{R} \tag{47}$$

By means of equation (11), the five capacitors' voltages can be formulated as following:

$$\begin{cases} V_{C1} = V_{C4} = V_{C5} = \frac{V_{in} + V_o}{3} \\ V_{C2} = V_{C3} = \frac{V_o - 2V_{in}}{3} \end{cases} \tag{48}$$

Based on Figure 5.3, the average inductor voltage can be calculated and equated to zero to calculate the voltage gain of the proposed converter during DCM (M_{DCM}) operation, as following:

$$\frac{1}{T}\left(\int_0^{dT} V_{in} dt - \int_0^{d_e T} V_{C2} dt \right) = 0 \tag{49}$$

$$V_{in} d + \left(\frac{2V_{in} - V_o}{3} \right) d_e = 0 \tag{50}$$

By solving (50), the voltage gain during DCM (M_{DCM}) can be calculated as shown in (51):

$$M_{DCM} = 1 + \sqrt{1 + \left(\frac{d^2}{2K} \right)} \tag{51}$$

5.4.2 Boundary Operating Condition

During the boundary conduction mode (BCM) the voltage gain of the proposed converter during the CCM and DCM operations is the same, thus, the critical value of *K* ($K_{critical}$) can be deduced by equating (12) and (51) as following:

$$K_{critical} = \frac{d(1-d)^2}{6(d+2)} \tag{52}$$

Figure 5.4 shows a plot of $K_{critical}$ versus *d*. When $K < K_{critical}$ the converter operates in DCM, otherwise, in CCM.

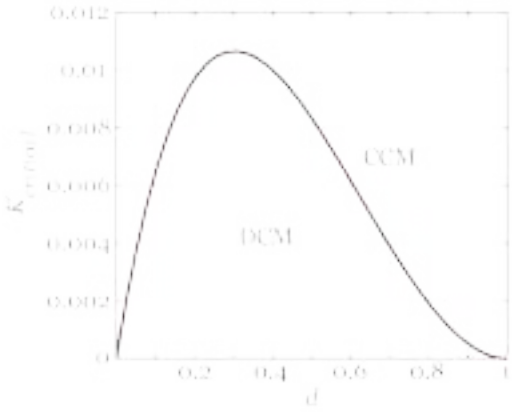


Figure 5.4: Boundary condition between DCM and CCM operations for the proposed converter.

5.4.3 Voltage Stresses on the Semiconductor Devices

During operating state *I*, the voltage stresses across *Q* and D_4 equal zero, while the voltage stresses across $D_1 \rightarrow D_3$ equal V_{C1}. During operating state *II*, the voltage stresses across *Q* and D_4 equal V_{C1}, while the voltage stresses across $D_1 \rightarrow D_3$ equal zero. During operating state *III*, the voltage stresses across *Q* and D_4 equal V_{in}, while the voltage stresses across $D_1 \rightarrow D_3$ equal V_{C2}. Accordingly and by means of (48), the voltage stresses on the switch and diodes during the three operating states can be formulated as in (53):

$$\begin{aligned} &V_Q(I) = V_{D4}(I) = V_{D1}(II) = V_{D2}(II) = V_{D3}(II) = 0 \\ &V_Q(II) = V_{D4}(II) = V_{D1}(I) = V_{D2}(I) = V_{D3}(I) = V_{C1} = V_{in}\left(\frac{M_{DCM}+1}{3}\right) \\ &V_Q(III) = V_{D4}(III) = V_{in} \\ &V_{D1}(III) = V_{D2}(III) = V_{D3}(III) = V_{C2} = V_{in}\left(\frac{M_{DCM}-2}{3}\right) \end{aligned} \quad (53)$$

5.4.4 Current Stresses on the Semiconductor Devices

As shown in Figure 5.3(b), the currents of the four diodes have a triangular shape, the peak values for i_{D1}, i_{D2}, i_{D3}, and i_{D4} are calculated by (44) and (54).

$$i_{D4(peak)} = \frac{2I_o}{d} = \frac{2V_o}{d\,R} = \frac{2\,M_{DCM}\,V_{in}}{d\,R} \quad (54)$$

The current of Q has a trapezoidal shape, the two heights of it are $i_{D4(peak)}$ and $i_{Q(peak)}$ as shown in Figure 5.3(b), and the value of $i_{Q(peak)}$ can be calculated by (55).

$$i_{Q(peak)} = \Delta i_{L1} + \Delta i_{L2} = \frac{d\, V_{in}}{f_s\, L_{eq}} \tag{55}$$

The rms values of the diode currents and the switch currents can be obtained by (56).

$$\begin{aligned} i_{D1(rms)} &= i_{D2(rms)} = i_{D3(rms)} = \frac{d\, V_{in}}{3 f_s\, L_{eq}} \sqrt{\frac{d_e}{3}} \\ i_{D4(rms)} &= \frac{2 M_{DCM}\, V_{in}}{R\, \sqrt{3d}} \\ i_{Q(rms)} &= \sqrt{\frac{d}{3}\left(i_{Q(peak)}^2 + i_{D4(peak)}^2 + i_{Q(peak)}\, i_{D4(peak)}\right)} \end{aligned} \tag{56}$$

5.5 Comparative Study with other Step-Up Solutions

This subsection compares the proposed converter with twelve other step-up converters that do not utilize any magnetic coupling components. The converters are compared based on the voltage gain, the number of active and passive components, the normalized voltage stresses on the power switches and diodes, the amount of input current ripple, the potential difference between the grounds of the input and output terminals ($V_{Grounds}$), and the voltage gain range. Table 5.2 summarizes the components and the features for each of the compared converters. The plots of the voltage gain versus the duty cycle for the compared converters are shown in Figure 5.5. The maximum normalized voltage stresses on the power switches and diodes versus the voltage gain are shown in Figure 5.6 and Figure 5.7, respectively.

Comparing the conventional three-level boost (TLB) converter with the proposed converter, on one hand, the proposed converter has one inductor, three capacitors, and two diodes more, and one power switch less compared to the conventional TLB converter. On the other hand, the proposed converter has higher voltage gain, lower voltage stresses on the semiconductor devices, and wider voltage gain range compared to the conventional TLB converter.

Additionally, $V_{Grounds}$ for the 117

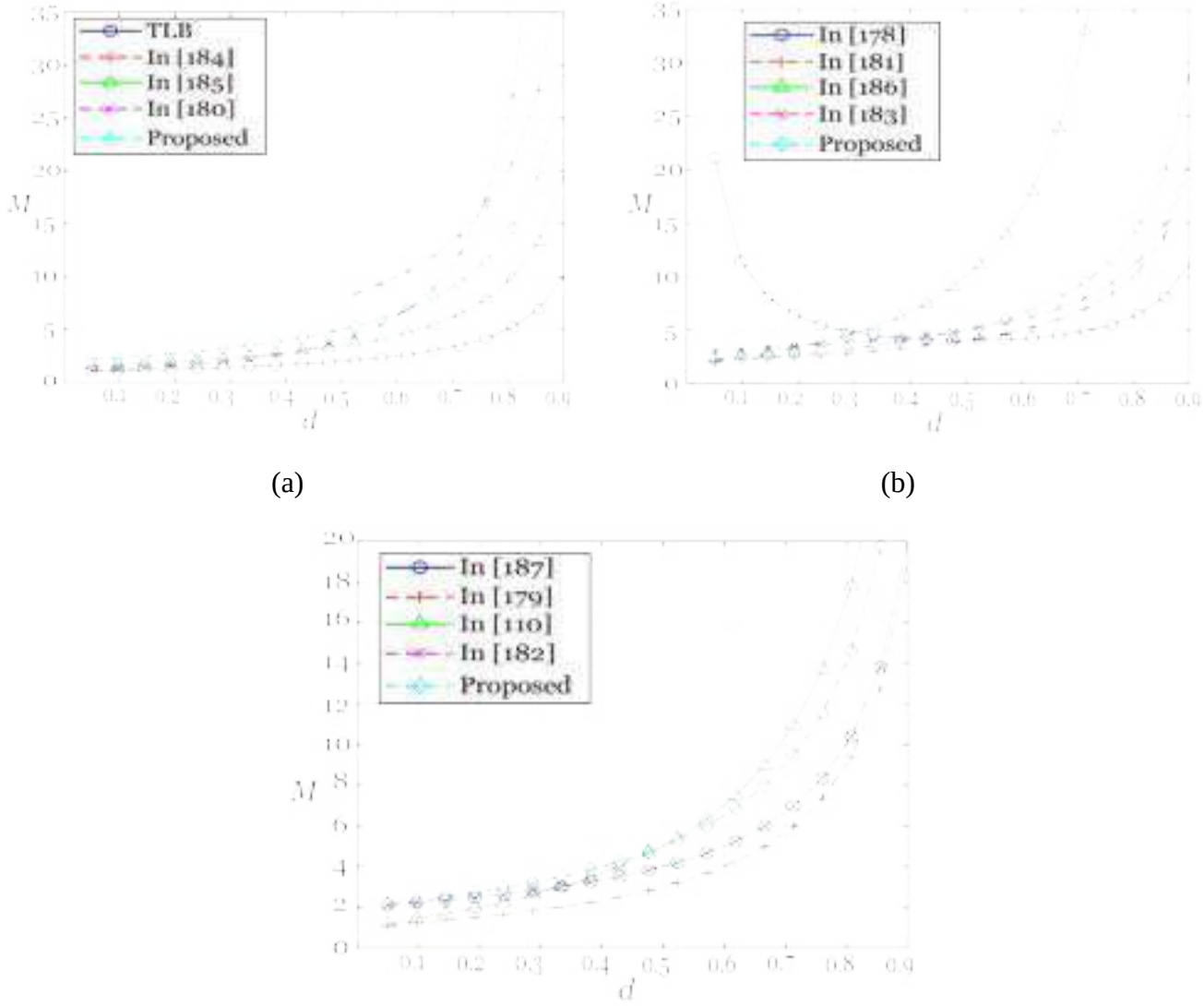
conventional TLB converter is HF PWM voltage, which causes more EMI noise and increases the periodic maintenance costs, on the contrary with the proposed converter which has $V_{Grounds}$ equals a constant voltage. The voltage quadrupler boost converter in [184] has higher voltage gain and lower voltage stress on its switches compared to the proposed converter.

Table 5.2: COMPARISON BETWEEN THE PROPOSED AND OTHER STEP-UP DC-DC CONVERTERS

Reference	Voltage gain (M)	Active components counts	Passive components counts	Voltage stress on transistors (V_Q / V_o)	Voltage stress on diodes (V_D / V_o)	Continuous input current	$V_{Grounds}$	Voltage gain range (d=0 →0.9)
TLB	$\frac{1}{1-d}$	2 Switches 2 Diodes	1 Inductor 2 Capacitors	$\frac{1}{2}$	$\frac{1}{2}$	*Yes*	HF PWM voltage	1→10
In [184]	$\frac{4}{1-d}$	2 Switches 4 Diodes	2 Inductors 4 Capacitors	$\frac{1}{4}$	$\frac{1}{2}, \frac{1}{4}$	*Yes*	HF PWM voltage	8→40 (minimum d = 0.5)
In [185]	$\frac{3+d}{2(1-d)}$	1 Switches 4 Diodes	2 Inductors 4 Capacitors	$\frac{1}{2}+\frac{1}{4M}$	$\frac{1}{2}+\frac{1}{4M}$	*Yes*	0 V	1.5→19.5
In [180]	$\frac{1}{(1-d)^2}$	1 Switch 3 Diodes	2 Inductors 2 Capacitors	1	$1, \sqrt{1-\frac{M-1}{M}}$, $1-\sqrt{1-\frac{M-1}{M}}$	*No*	0 V	1→100
In [178]	$\frac{1}{d(1-d)}$	2 Switches 3 Diodes	2 Inductors 2 Capacitors	$\frac{1}{2}+\sqrt{\frac{1}{4}-\frac{1}{M}}, 1$	$\frac{1}{2}+\sqrt{\frac{1}{4}-\frac{1}{M}}$, $\frac{3}{2}+\sqrt{\frac{1}{4}-\frac{1}{M}}$	*Yes*	HF PWM voltage	-- →11
In [181]	$\frac{2}{1-d}$	2 Switches 2 Diodes	2 Inductors 2 Capacitors	$\frac{1}{2}$	$\frac{1}{2}, 1$	*Yes*	HF PWM	2→20
In [186]	$\frac{2+d}{(1-d)^2}$	2 Switches 5 Diodes	3 Inductors 6 Capacitors	$\frac{\sqrt{1+12M}-1}{1+6M-\sqrt{1+12M}}, \frac{2M}{1+6M-\sqrt{1+12M}}$	$\frac{\sqrt{1+12M}-1}{1+6M-\sqrt{1+12M}}, \frac{2M}{1+6M-\sqrt{1+12M}}$	*No*	HF PWM	2→290
In [183]	$\frac{3-d}{1-d}$	1 Switch 4 Diodes	1 Inductor 4 Capacitors	$\frac{M-1}{2M}$	$\frac{M-1}{2M}$	*No*	Constant voltage	3→21
In [187]	$\frac{2}{1-d}$	1 Switch 3 Diodes	2 Inductors 4 Capacitors	$\frac{1}{2}$	$\frac{1}{2}$	*Yes*	Constant voltage	2→20
In [179]	$\frac{1+d}{1-d}$	1 Switch 3 Diodes	2 Inductors 3 Capacitors	$\frac{1+M}{2M}$	$\frac{1+M}{2M}$	*No*	0 V	1→19
In [110]	$\frac{1+3d}{1-d}$	2 Switches 2 Diodes	3 Inductors 3 Capacitors	$\frac{3+M}{4M}$	$\frac{3+M}{2M}$	*Yes*	HF PWM voltage	1→37
In [182]	$\frac{2}{1-d}$	1 Switch 3 Diodes	1 Inductor 3 Capacitors	$\frac{1}{2}$	$\frac{1}{2}$	*Yes*	0 V	2→20
Proposed	$\frac{2+d}{1-d}$	1 Switch 4 Diodes	2 Inductors 5 Capacitors	$\frac{1+M}{3M}$	$\frac{1+M}{3M}$	*Yes*	Constant voltage	2→29

It also has one capacitor less and one power switch more compared to the proposed converter. This converter has two main drawbacks, first, its $V_{Grounds}$ is HF PWM voltage, on the contrary with

the proposed converter where its $V_{Grounds}$ is a constant voltage, second, the maximum normalized voltage stress on its diodes is higher compared to that of the proposed converter. The recently proposed single-switch converter in [185] has one less capacitor and the same number of switches, diodes and inductors compared to the proposed converter. The voltage gain of the proposed



(a) (b)

(c)

Figure 5.5: Comparison of voltage gain M versus duty cycle d. (a) Between the proposed converter, the TLB converter, converters in [184], [185], and [180]. (b) Between the proposed converter, converters in [178], [181], [186], and [183]. (c) Between the proposed converter and the converters in [187], [179], [110], and [182]

converter is higher and the voltage stresses on the switch and diodes of the proposed converter are lower compared to the converter in [185]. Comparing the proposed converter with the quadratic boost converter in [180], on one hand, the converter in [180] has one diode and three capacitors less than the proposed converter, on the other hand, this converter has lower voltage gain (for $d < 0.6$) and higher voltage stresses on its switch and diodes compared to the proposed converter. Additionally, the input current ripple of the converter in [180] is high, which can reduce the lifetime of the fuel cell. The extendable step-up dc-dc converter in [178] has one diode and three capacitors less than the proposed converter, while the proposed converter has one power switch less. The proposed converter has higher voltage gain (for $d > 0.4$) and lower voltage stresses on the power switches and diodes compared to the converter in [178]. Comparing the proposed converter with converter *II* in [181], on one hand, it has two diodes and three capacitors less than the proposed converter, while the proposed converter has one power switch less. The voltage gain of the proposed converter is higher and the voltage stress on its semiconductor devices is less than that in converter *II* in [181]. In addition, the $V_{Grounds}$ of the converter in [181] is HF PWM voltage which may add a lot of EMI noise. The converter in [186] has one power switch, one diode, one inductor, and one capacitor more than the proposed converter. The proposed converter has lower voltage gain compared to the converter in [186], nevertheless, the maximum normalized voltage stresses on the semiconductor devices of the

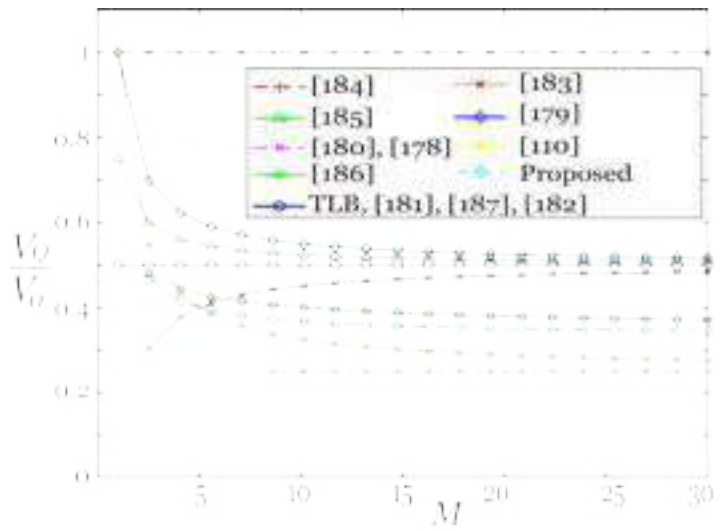


Figure 5.6: Maximum normalized voltage stress on the power switches in the compared converters.

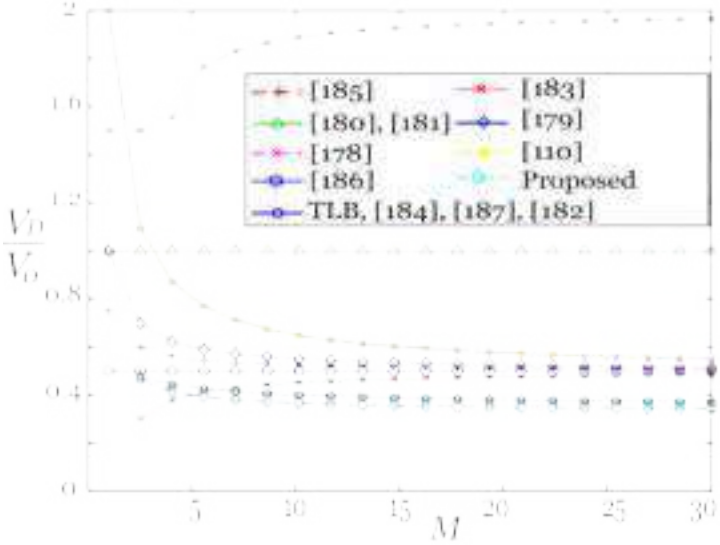


Figure 5.7: Maximum normalized voltage stress on the diodes in the compared converters.

proposed converter are less. The converter in [186] also suffers from high input current ripple and its $V_{Grounds}$ is HF PWM voltage, which render this converter not suitable for fuel cell EV application. The hybrid converter presented in [183] has one less inductor, one less capacitor and the same number of semiconductor devices compared to the proposed converter. The converter in [183] has lower voltage gain (when $d > 0.5$), and higher voltage stresses on the semiconductor devices (when $M > 5$) compared to the proposed converter. Added to that, the converter in [183]

has a high input current ripple. Comparing the proposed converter with the single-switch hybrid boost converter in [187], on one hand, this converter has one diode and one capacitor less compared to the proposed converter. On the other hand, the proposed converter has higher voltage gain, less voltage stresses on the semiconductor devices, and wider voltage gain compared to the converter in [187]. The voltage-lift based boost converter in [179] has one less diode and two less capacitors compared to the proposed converter. The proposed converter has a wider voltage gain, less voltage stresses on the power switch and diodes, and higher voltage gain compared to the converter in [179]. In addition, the input current ripple of the converter in [179] is high. The converter in [110] integrates active switched-inductor and passive switched-capacitor networks to enhance the voltage gain and reduce the voltage stress on the semiconductor devices. The converter in [110] has lower voltage gain (when $d < 0.5$), higher voltage stress on its power switches (when $M < 5$), and higher voltage stress on its diodes compared to the proposed converter. Regarding the number of components, the converter in [110] has two less diodes, two less capacitors, one more power switch and one more inductor compared to the proposed converter. The converter in [110] also suffers from additional EMI noise because its $V_{Grounds}$ is HF PWM voltage. The multilevel boost converter in [182], on one hand, has one less diode, one less inductor, and two less capacitors compared to the proposed converter. This converter has low input current ripple and a common ground between its input and out terminals. Nevertheless, the proposed converter has higher voltage gain, lower voltage stress on its semiconductor devices, and a wider voltage gain range compared to the converter in [182].

Based on the comparisons above, it is clear that the proposed converter combines many merits such as: low number of power switches, high step-up voltage conversion ratio, wide voltage gain range, low input current ripple, and low voltage stresses on its semiconductor devices. All these

features make the proposed converter a good choice as a power electronic interface between the fuel cell and the high voltage dc-link bus of the EV.

5.6 Design of Components

5.6.1 Selection of Semiconductor Devices

Equation (14) calculates the voltage stress on the power switch and diodes, hence, by knowing the maximum values of V_o and M, the maximum voltage stress on the semiconductor devices can be calculated. Similarly, equations (23)-(27) calculate the current stresses on the power switch and diodes in CCM operation, while (44), (54) and (55) calculate the current stresses on the semiconductor devices in DCM operation. Accordingly, by knowing the maximum voltage stress and current stress on each semiconductor device, the ratings of the power switch and diodes can be determined such that the maximum voltage and current stresses should be within the safe operating area (SOA) of the selected diodes and power switch.

5.6.2 Design of Inductors

By means of (15) and (16), the inductor currents can be calculated, hence, the saturation currents of L_1 and L_2 should be higher than the maximum currents flowing through L_1 and L_2, respectively. When the maximum ripple currents Δi_{L1}, and Δi_{L2} are known, the minimum values of inductances can be obtained by (57).

$$\begin{cases} L_1 \geq \dfrac{d\, V_{in}}{f_s\, \Delta i_{L1}} \\ L_2 \geq \dfrac{d\, V_{in}}{f_s\, \Delta i_{L2}} \end{cases} \tag{57}$$

5.6.3 Design of Capacitors

Equation (11) calculates the voltages across the five capacitors, accordingly the selected capacitors should be able to withstand these voltage levels.

When the maximum ripple voltages ΔV_{C1}, ΔV_{C2}, ΔV_{C3}, ΔV_{C4} and ΔV_{C5} are known, the minimum values of capacitances can be obtained by (58).

$$\begin{cases} C_1 \geq \dfrac{2I_o d}{f_s\, \Delta V_{C1}} \\ C_2 \geq \dfrac{I_o d}{f_s\, \Delta V_{C2}} \\ C_3 \geq \dfrac{I_o d}{f_s\, \Delta V_{C3}} \\ C_4 \geq \dfrac{I_o}{f_s\, \Delta V_{C4}} \\ C_5 \geq \dfrac{I_o(1-d)}{f_s\, \Delta V_{C5}} \end{cases} \tag{58}$$

5.7 Dynamic Modeling and Voltage Loop Controller Design

5.7.1 Small-Signal Modeling

In this analysis, the equivalent series resistances of the inductors and capacitors are omitted, the power switch and diodes are assumed to be ideal. Fig. 3(b) shows that there is mutual coupling between the capacitors ($C_1 \rightarrow C_5$) of the proposed converter, accordingly, to remove this coupling, small resistances ($r_{C2} = 0.1\Omega$ and $r_{C4} = 0.1\Omega$) are considered in series with C_2 and C_4, respectively. In this subsection, the state-space average and small-signal models of the proposed converter are derived for the converter when it operates in CCM, thus, the converter has only two operating states (*I* and *II*). By applying the averaging method on the inductors' voltages and

capacitors' currents during operating states *I* and *II*, calculated by (1)-(4), the state-space average model of the proposed converter can be obtained as shown in (59).

In order to derive the small-signal model of the proposed converter, all the state variables, output variable, input variable, and control variable should be replaced by their dc quiescent values and ac perturbation signals, as in (60).

$$\begin{aligned}
v_{in}(t) &= V_{in} + \hat{v}_{in} \\
v_{C1}(t) &= V_{C1} + \hat{v}_{C1} \\
v_{C2}(t) &= V_{C2} + \hat{v}_{C2} \\
v_{C3}(t) &= V_{C3} + \hat{v}_{C3} \\
v_{C4}(t) &= V_{C4} + \hat{v}_{C4} \\
v_{C5}(t) &= V_{C5} + \hat{v}_{C5} \\
i_{L1}(t) &= I_{L1} + \hat{\imath}_{L1} \\
i_{L2}(t) &= I_{L2} + \hat{\imath}_{L2} \\
v_o(t) &= V_o + \hat{V}_o \\
d(t) &= d + \hat{d}
\end{aligned}
\quad \text{with} \quad
\begin{aligned}
|\hat{v}_{in}| &\ll |V_{in}| \\
|\hat{v}_{C1}| &\ll |V_{C1}| \\
|\hat{v}_{C2}| &\ll |V_{C2}| \\
|\hat{v}_{C3}| &\ll |V_{C3}| \\
|\hat{v}_{C4}| &\ll |V_{C4}| \\
|\hat{v}_{C5}| &\ll |V_{C5}| \\
|\hat{\imath}_{L1}| &\ll |I_{L1}| \\
|\hat{\imath}_{L2}| &\ll |I_{L2}| \\
|\hat{v}_o| &\ll |V_o| \\
|\hat{d}| &\ll |d|
\end{aligned}
\qquad (60)$$

Where V_{in}, V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{C5}, V_o, I_{L1}, I_{L2}, d are the dc quiescent values of the input variable, state variables, output variable, and the control variable, and $\hat{v}_{in}$, $\hat{v}_{C1}$, $\hat{v}_{C2}$, $\hat{v}_{C3}$, $\hat{v}_{C4}$, $\hat{v}_{C5}$, $\hat{\imath}_{L1}$, $\hat{\imath}_{L2}$, $\hat{v}_o$, and $\hat{d}$ are the corresponding small ac perturbation signals. The small-signal model of the proposed converter is given in (61).

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{C1}(t)}{dt} \\ \frac{dv_{C2}(t)}{dt} \\ \frac{dv_{C3}(t)}{dt} \\ \frac{dv_{C4}(t)}{dt} \\ \frac{dv_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d(t)-1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{d(t)}{L_2} & 0 & \frac{-1}{L_2} & 0 & 0 \\ \frac{1-d(t)}{C_1} & \frac{-d(t)}{C_1} & \frac{-1}{RC_1}+\frac{d(t)-1}{C_1 r_{C4}} & \frac{-1}{RC_1} & 0 & \frac{1-d(t)}{C_1 r_{C4}} & \frac{-1}{RC_1} \\ 0 & 0 & \frac{-d(t)}{RC_2} & \frac{-d(t)}{RC_2}+\frac{d(t)-1}{C_2 r_{C2}} & \frac{1-d(t)}{C_2 r_{C2}} & 0 & -\frac{d(t)}{RC_2} \\ 0 & \frac{1}{C_3} & \frac{d(t)-1}{RC_3} & \left(\frac{1}{r_{C2}}-\frac{1}{R}\right)\left(\frac{1-d(t)}{C_3}\right) & \frac{d(t)-1}{C_3 r_{C2}} & 0 & \frac{d(t)-1}{RC_3} \\ 0 & 0 & \frac{1-d(t)}{C_4 r_{C4}} & 0 & 0 & \frac{-1}{C_4 r_{C4}} & \frac{d(t)}{C_4 r_{C4}} \\ 0 & 0 & \frac{-1}{RC_5} & \frac{-1}{RC_5} & 0 & \frac{d(t)}{C_5 r_{C4}} & \frac{-d(t)}{r_{C4} C_5}-\frac{1}{RC_5} \end{bmatrix} \times \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ v_{C3}(t) \\ v_{C4}(t) \\ v_{C5}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T v_{in}(t) \tag{59}$$

$$v_o(t) = [0 \quad 0 \quad 1 \quad 1 \quad 0 \quad 0 \quad 1]\,[i_{L1}(t) \quad i_{L2}(t) \quad v_{C1}(t) \quad v_{C2}(t) \quad v_{C3}(t) \quad v_{C4}(t) \quad v_{C5}(t)]^T$$

$$\begin{aligned} v_{in}(t) &= V_{in} + \hat{v}_{in} & |\hat{v}_{in}| &\ll |V_{in}| \\ v_{C1}(t) &= V_{C1} + \hat{v}_{C1} & |\hat{v}_{C1}| &\ll |V_{C1}| \\ v_{C2}(t) &= V_{C2} + \hat{v}_{C2} & |\hat{v}_{C2}| &\ll |V_{C2}| \\ v_{C3}(t) &= V_{C3} + \hat{v}_{C3} & |\hat{v}_{C3}| &\ll |V_{C3}| \\ v_{C4}(t) &= V_{C4} + \hat{v}_{C4} & |\hat{v}_{C4}| &\ll |V_{C4}| \\ v_{C5}(t) &= V_{C5} + \hat{v}_{C5} & |\hat{v}_{C5}| &\ll |V_{C5}| \\ i_{L1}(t) &= I_{L1} + \hat{\imath}_{L1} & |\hat{\imath}_{L1}| &\ll |I_{L1}| \\ i_{L2}(t) &= I_{L2} + \hat{\imath}_{L2} & |\hat{\imath}_{L2}| &\ll |I_{L2}| \\ v_o(t) &= V_o + \hat{V}_o & |\hat{v}_o| &\ll |V_o| \\ d(t) &= d + \hat{d} & |\hat{d}| &\ll |d| \end{aligned} \quad \text{with} \tag{60}$$

$$
\begin{bmatrix} \frac{d\hat{\imath}_{L1}(t)}{dt} \\ \frac{d\hat{\imath}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{C1}(t)}{dt} \\ \frac{d\hat{v}_{C2}(t)}{dt} \\ \frac{d\hat{v}_{C3}(t)}{dt} \\ \frac{d\hat{v}_{C4}(t)}{dt} \\ \frac{d\hat{v}_{C5}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{d}{L_2} & 0 & \frac{-1}{L_2} & 0 & 0 \\ \frac{1-d}{C_1} & \frac{-d}{C_1} & -\left(\frac{1}{RC_1}+\frac{1-d}{C_1 r_{C4}}\right) & \frac{-1}{RC_1} & 0 & \frac{1-d}{C_1 r_{C4}} & \frac{-1}{RC_1} \\ 0 & 0 & \frac{-d}{RC_2} & -\left(\frac{d}{RC_2}+\frac{1-d}{C_2 r_{C2}}\right) & \frac{1-d}{C_2 r_{C2}} & 0 & -\frac{d}{RC_2} \\ 0 & \frac{1}{C_3} & \frac{d-1}{RC_3} & \left(\frac{1}{r_{C2}}-\frac{1}{R}\right)\left(\frac{1-d}{C_3}\right) & \frac{d-1}{C_3 r_{C2}} & 0 & \frac{d-1}{RC_3} \\ 0 & 0 & \frac{1-d}{C_4 r_{C4}} & 0 & 0 & \frac{-1}{C_4 r_{C4}} & \frac{d}{C_4 r_{C4}} \\ 0 & 0 & \frac{-1}{RC_5} & \frac{-1}{RC_5} & 0 & \frac{d}{C_5 r_{C4}} & -\left(\frac{d}{r_{C4}C_5}+\frac{1}{RC_5}\right) \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1}(t) \\ \hat{\imath}_{L2}(t) \\ \hat{v}_{C1}(t) \\ \hat{v}_{C2}(t) \\ \hat{v}_{C3}(t) \\ \hat{v}_{C4}(t) \\ \hat{v}_{C5}(t) \end{bmatrix}
$$

$$
+ \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 \\ \frac{1}{L_1} & \frac{-1}{C_1} & \frac{-1}{C_1} & \frac{1}{C_1 r_{C4}} & 0 & 0 & \frac{-1}{C_1 r_{C4}} & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_2} & \frac{-1}{RC_2}+\frac{1}{C_2 r_{C2}} & \frac{-1}{C_2 r_{C2}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{RC_3} & \frac{1}{RC_3}-\frac{1}{C_3 r_{C2}} & \frac{1}{C_3 r_{C2}} & 0 & \frac{1}{RC_3} \\ 0 & 0 & 0 & \frac{-1}{C_4 r_{C4}} & 0 & 0 & 0 & \frac{-1}{C_4 r_{C4}} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_4 r_{C4}} & \frac{-1}{C_4 r_{C4}} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \end{bmatrix} \hat{d}(t) \qquad (61)
$$

$$
\hat{v}_o(t) = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1}(t) & \hat{\imath}_{L2}(t) & \hat{v}_{C1}(t) & \hat{v}_{C2}(t) & \hat{v}_{C3}(t) & \hat{v}_{C4}(t) & \hat{v}_{C5}(t) \end{bmatrix}^T
$$

$$
\frac{G_{v_o d}(\mathrm{S})}{(\hat{v}_{in}=0)} = \frac{\hat{v}_o}{\hat{d}} = \frac{S^6 + a_5 S^5 + a_4 S^4 + a_3 S^3 + a_2 S^2 + a_1 S + a_0}{b_7 S^7 + b_6 S^6 + b_5 S^5 + b_4 S^4 + b_3 S^3 + b_2 S^2 + b_1 S + b_0} \qquad (62)
$$

Where a_6 = -5.299e22, a_5 = -1.276e32, a_4 = -6.333e37, a_3 = -7.675e42, a_2 = -1.157e45, a_1 = -9.863e49, a_0 = -2.191e50, b_7 = 8.503e17, b_6 = 1.094e24, b_5 = 3.775e29, b_4 = 3.839e34, b_3 = 8.207e36, b_2 = 5.137e41, b_1 = 1.192e43, b_0 = 2.192e47.

$$
G_C = \left(K_P + \frac{K_I}{S}\right) \times G_{v_o d}(\mathrm{S}) = \frac{e_7 S^7 + e_6 S^6 + e_5 S^5 + e_4 S^4 + e_3 S^3 + e_2 S^2 + e_1 S + e_0}{f_8 S^8 + f_7 S^7 + f_6 S^6 + f_5 S^5 + f_4 S^4 + f_3 S^3 + f_2 S^2 + f_1 S} \qquad (63)
$$

Where e_7 = -1.59e19, e_6 = - 3.828e28, e_5 = - 1.9e34, e_4 = - 2.303e39, e_3 = - 3.495e41, e_2 = - 2.959e46, e_1 = - 9.829e46, e_0 = - 7.232e46, f_8 = 8.5e17, f_7 = 1.094e24, f_6 = 3.775e29, f_5 = 3.839e34, f_4 = 8.207e36, f_3 = 5.137e41, f_2 = 1.192e43, f_1 = 2.192e47.

By means of Laplace transform on (61), and the parameters of the experimental setup in Table III, the control-to-output transfer function $G_{v_o d}(\mathrm{S})$ can be obtained in the frequency domain from the time domain as in (62).

5.8 Closed-Loop Voltage Controller

In the developed experiment, a proportional integral (PI) controller is utilized to regulate the output voltage of the proposed converter. The structure of the closed-loop voltage controller is shown in Figure.5.8 and the parameters of the adopted PI controller are K_P =0. .0003 and K_I = 0.00033. The compensated transfer function of the proposed converter is given in (63). The Bode plots of the compensated transfer function of the proposed converter are shown in Figure 5.9. These bode plots show that the proposed converter with the adopted PI voltage controller has positive gain and phase margins, which indicates a stable operation.

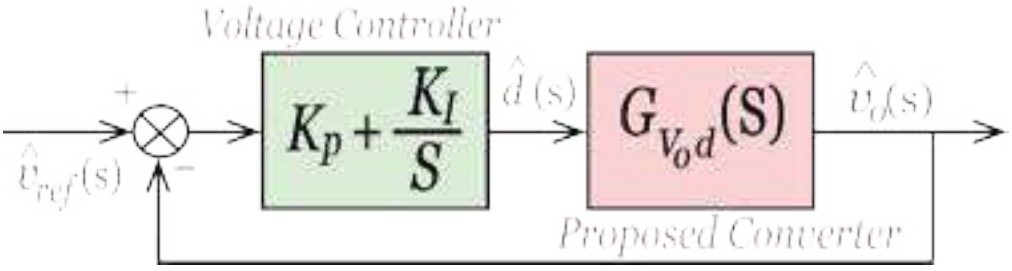


Figure 5.8: Closed-loop PI voltage controller of the proposed converter.

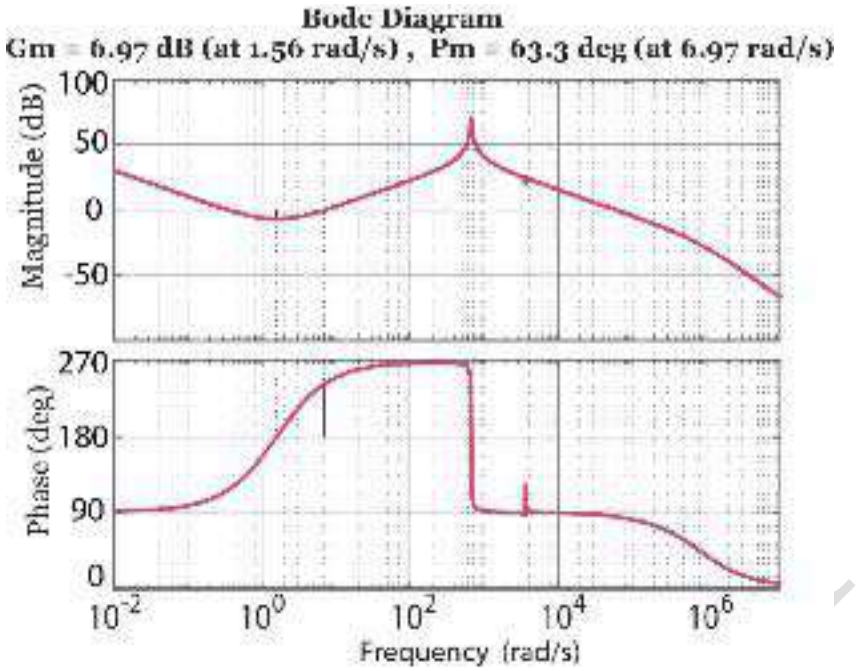


Figure 5.9: Bode plot of the compensated transfer function of the proposed converter.

5.9 Experimental Results and Analysis

To verify the theoretical analyses of the proposed converter, a scaled-down experimental prototype was built, as shown in Figure 5.10. The developed prototype has a rated output power of 1.3kW, and its power circuit is built with (GS66516T) GaN HEMT and (IDH20G65C6) SiC diodes. The currents and voltages are measured via sense resistors, and the converter operation is controlled by a (TMS320f28377s) microcontroller. The values of the used inductors and capacitors used in the developed prototype are enlisted in Table 5.3. The voltage profile of "CH40020F-S" fuel cell from "Zahn Electronics INC." is depicted by a programmable power supply.

Figure 5.10: Experimental setup.

Table 5.3: EXPERIMENT PARAMETERS

Parameters and Components	Values
Rated power P_o	1.3 kW
Output voltage V_o	800V
Power switch Q	GS66516T
Power Diodes D_1, D_2, D_3, D_4	IDH20G65C6
Inductors L_1, L_2	250 µH
Capacitors C_1, C_2, C_3, C_4, C_5	220 µF
Switching frequency f_s	100 KHz
Load R (Case study I)	650 Ω
Load R (Case study II)	2000 Ω
Microcontroller	TMS320f28377s

Two case studies are investigated in this section, namely: 1) Case study I: aims to verify the theoretical analysis of the proposed converter when it operates in CCM. 2) Case study II: aims to validate the important relationships in the theoretical analysis of the proposed converter when it operates in DCM.

The values of inductors and capacitors are enlisted in Table 5.3. In case study I, the input voltage V_{in} is 90V, the load resistor R is 650 Ω, and d = 0.7. In case study II, V_{in} is 150V, the load resistor R is 2000 Ω, and d = 0.4.

Case study I investigates the operation of the proposed converter during CCM. The values of inductors, capacitors, load resistance, input voltage, and duty cycle are as following: $L_1 = L_2 = 250$ µH, $C_1 \rightarrow C_5 = 220$ µF, $R = 650\ \Omega$, and $d = 0.7$. The experimental results for this case study are shown in Figure 5.11. The dimensionless parameter K is defined by (47), thus, it can be calculated for case study I as following:

$$K = \frac{f_s\, L_{eq}}{R} = \frac{10^5 \times 125 \times 10^{-6}}{650} = 0.019 \tag{64}$$

The critical value of K can be calculated by (52), as shown in (65):

$$K_{critical} = \frac{d(1-d)^2}{6(d+2)} = \frac{0.7 \times (0.3)^2}{6 \times (2.7)} = 3.89 \times 10^{-3} \tag{65}$$

Since K is greater than $K_{critical}$, the converter operates in CCM during case study I. The voltage on the five capacitors and the output voltage can be calculated using (11) as following:

$$\begin{aligned} V_{C1} = V_{C4} = V_{C5} &= \frac{V_{in}}{(1-d)} = \frac{90}{0.3} = 300\ \text{V} \\ V_{C2} = V_{C3} &= \frac{d\, V_{in}}{(1-d)} = \frac{0.7 \times 90}{0.3} = 210\ V \\ V_o &= \frac{2+d}{1-d}\, V_{in} = \frac{2.7}{0.3} \times 90 = 810\ \text{V} \end{aligned} \tag{66}$$

Which closely agree with the experimental results in Figure 5.11(b), (c), and (d). Also, the inductor currents and the load current can be calculated by (15) and (16), additionally, the ripple currents can be calculated using (57).

$$\begin{cases} I_{L2} = I_o = \frac{V_o}{R} = \frac{(2+d)\, V_{in}}{R(1-d)} = \frac{2.7 \times 90}{650 \times 0.3} \approx 1.25\ \text{A} \\ I_{L1} = M I_{L2} = \frac{(2+d) V_o}{(1-d) R} = \left(\frac{2+d}{1-d}\right)^2 \frac{V_{in}}{R} = \left(\frac{2.7}{0.3}\right)^2 \frac{90}{650} = 11.2\ A \end{cases} \tag{67}$$

$$\begin{aligned} \Delta i_{L1} &= \frac{d\, V_{in}}{f_s\, L_1} = \frac{0.7 \times 90}{10^5 \times 250 \times 10^{-6}} = 2.5\ \text{A} \\ \Delta i_{L2} &= \frac{d\, V_{in}}{f_s\, L_2} = \frac{0.7 \times 90}{10^5 \times 250 \times 10^{-6}} = 2.5\ \text{A} \end{aligned} \tag{68}$$

Which closely agree with the experimental results in Figure 5.11(a). The voltage stresses on the power switch and diodes can be obtained by (13), as following:

$$V_Q = V_{D1} = V_{D2} = V_{D3} = V_{D4} = \frac{V_{in}}{(1-d)} = \frac{90}{0.3} = 300\ \text{V} \qquad (69)$$

These voltage stresses calculated by (69) are close to the experimental results in Figure 5.11(e) and (f). The current stresses on the power switch and diodes can be calculated using (23)-(27).

$$\begin{cases} i_Q = \frac{1+2d}{d(1-d)} I_o = \frac{(1+1.4)}{0.7\times 0.3} \times 1.26 = 14.4\ \text{A} \\ i_{D1} = i_{D2} = i_{D3} = \frac{I_o}{(1-d)} = \frac{1.26}{0.3} = 4.2\ \text{A} \\ i_{D4} = \frac{I_o}{d} = \frac{1.26}{0.7} = 1.8\ \text{A} \end{cases} \qquad (70)$$

The current stresses calculated in (70) are verified by the experimental results in Figure 5.11(h) and (g).

In order to evaluate the dynamic performance of the proposed converter and the adopted PI voltage controller, the input voltage is changed gradually from 320 V to 80 V while keeping the reference output voltage fixed at 800 V. Figure 5.11(i) shows the output voltage and the current of L_1 when the input voltage gradually goes down from 320 V to 80 V, and it is clear that the proposed converter with the adopted PI controller is capable of holding the output voltage fixed during the wide fluctuation in the input voltage. Based on equation (12), I_{L1} can be calculated when V_{in} = 320 V and when V_{in} = 80 V, as $I_{L1} \approx 3$ A and $I_{L1} \approx 12.3$ A, respectively, which closely agree with the measured current of L_1 shown in Figure 5.11(i).

Figure 5.13 shows the calculated power loss distributions for the experiment in case study I. The capacitors' conduction losses are dominant with 20.14 W which account for 31% of the total power loss in this case study. The reason for the high capacitors' losses is the utilization of electrolytic capacitors in the experimental prototype, if film capacitors were used, the capacitors' conduction losses would have been lower. The switching loss of the power switch comes next with

15.8 W which accounts for 25% of the total power loss. The losses of the diodes equal 13.5 W which account for 21% of the total power loss. The conduction losses of the two inductors equal 8.6W and account for 13% of the total power loss, and the conduction loss of the power switch equal 6 W which accounts for 9% of the total power loss. The low switching and conduction losses of the power switch is due to the utilization of a GaN HEMT as a power switch, which has lower on resistance, lower total charge, and lower output capacitance compared to its silicon (Si) and SiC power counterparts.

The plots between the measured efficiency and the input voltage of the proposed converter are shown in Figure 5.14 (a), as they were measured using a power analyzer (Tektronix PA3000). Two measured efficiency curves are given in Figure 5.14 to depict the efficiency of the proposed converter when the output power equals 1 kW and 1.3 kW, the output voltage is fixed at 800 V, and the input voltage varies from 90 V up to 300 V. When P_o equals 1.3 kW, the minimum efficiency is 94.6% when the input voltage is 90 V, and the maximum efficiency is 97.3% when the input voltage is 220 V. When P_o is 1 kW, the minimum efficiency is 95.5% when the input voltage is 90 V, and the maximum efficiency is 97.6% when the input voltage is 220 V. For the efficiency curves in Figure 5.14(a), the efficiency is low when input voltage is low and this is because of the high conduction losses in the input inductor, capacitors, diodes, and switch (since the converter is operating at relatively high values of duty cycle), and the efficiency keeps improving as the input voltage increases. After a certain input voltage value, the efficiency starts dropping due to the increased switching loss of the power switch. The calculated efficiency curves of the proposed converter when the output power equals 1 kW and 1.3 kW, the output voltage is fixed at 800 V, and the input voltage varies from 90 V up to 300 V are presented in Figure 5.14(a). The small deviations between the measured and calculated efficiency curves is due to the

assumptions used in loss calculation. The measured efficiency curves when the output voltage is fixed at 800 V and the output power is changed from 500 W to 1.3 kW when the input voltage is 100 V and 200 V are shown in Figure 5.14(b). Based on Figure 5.14(b), the maximum efficiency is 97.8% when the input voltage is 200 V and the output power is 500 W, while the maximum efficiency is 97% when the input voltage is 100 V and the output power is 500 W.

Case study II investigates the operation of the proposed converter in DCM. The load is represented by a 2000Ω resistance, and the input voltage is set at 150 V. In this case study, the closed-loop voltage controller is deactivated, and the converter operates with duty cycle of 0.4. The dimensionless parameter *K* is defined by (47), hence, it can be calculated for case study II as following:

$$K = \frac{f_s\, L_{eq}}{R} = \frac{10^5 \times 125 \times 10^{-6}}{2000} = 6.25 \times 10^{-3} \tag{71}$$

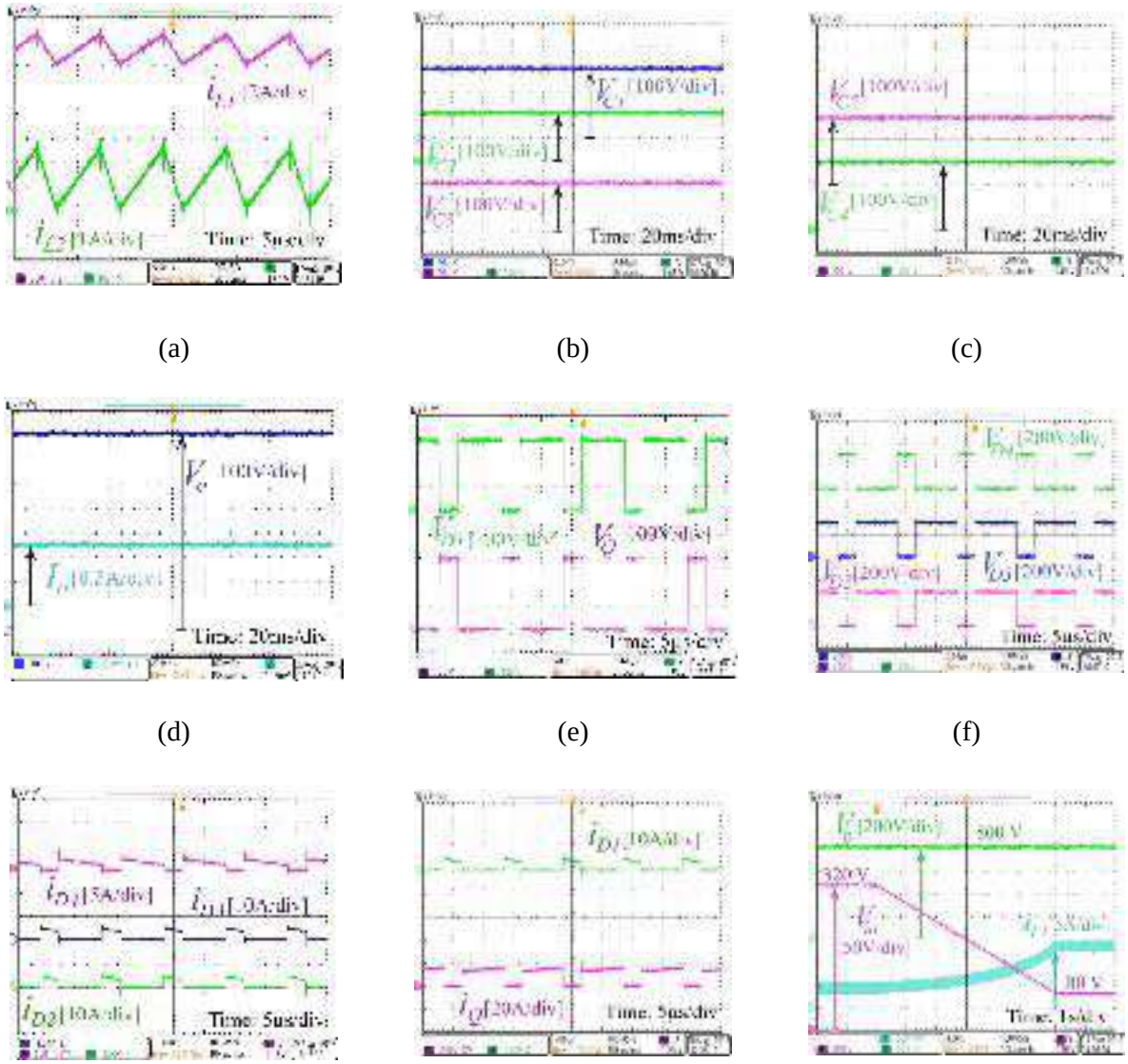
The critical value of *K* can be calculated by (52), as shown in (72):

$$K_{critical} = \frac{d(1-d)^2}{6(d+2)} = \frac{0.4 \times (0.6)^2}{6 \times (2.4)} = 0.01 \tag{72}$$

Since $K_{critical}$ is greater than *K*, the converter operates in DCM during case study II.

The current ripples of the two inductors can be obtained by means of (43), as following:

$$\begin{cases} \Delta i_{L1} = \dfrac{d\, V_{in}}{f_s L_1} = \dfrac{0.4 \times 150}{10^5 \times 250 \times 10^{-6}} = 2.4 \text{ A} \\ \Delta i_{L2} = \dfrac{d\, V_{in}}{f_s L_2} = \dfrac{0.4 \times 150}{10^5 \times 250 \times 10^{-6}} = 2.4 \text{ A} \end{cases} \tag{73}$$



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 5.11: Experimental results of case study I

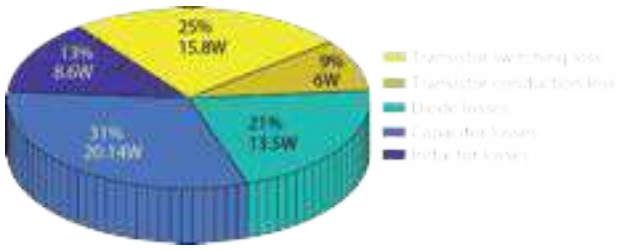
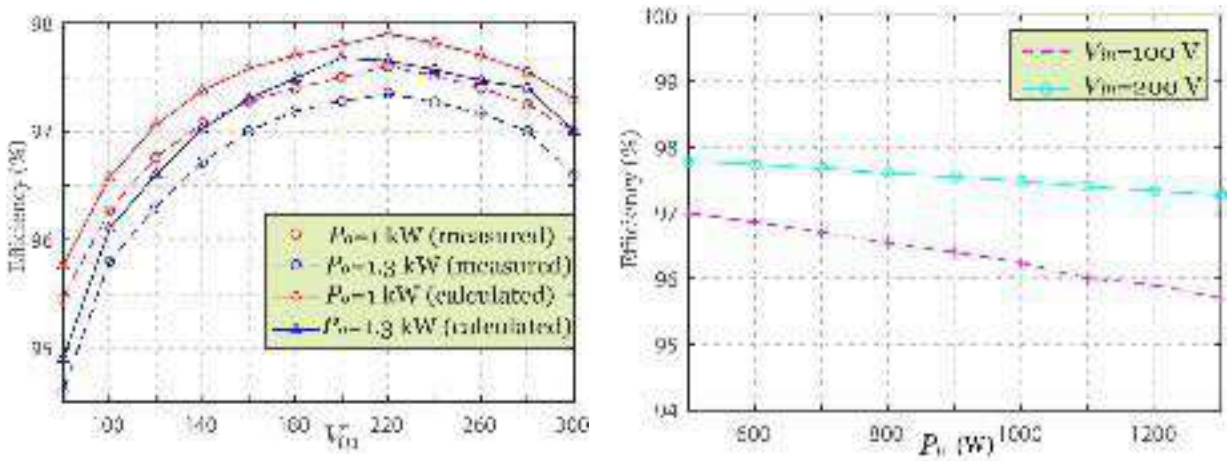


Figure 5.12: Breakdown of losses in Case I



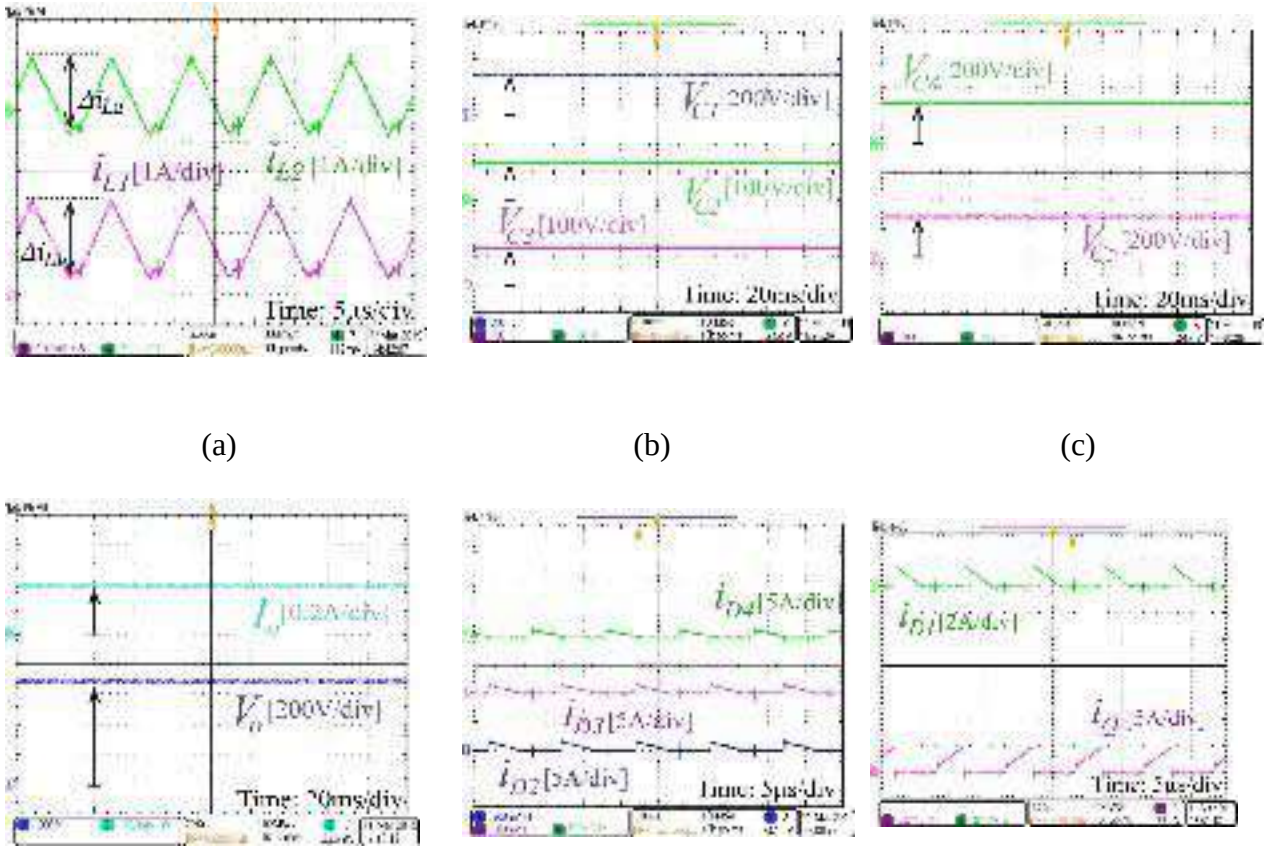
(a) (b)

Figure 5.13: Measured efficiency curves.

Which closely agree with the experimental results in Figure 5.15(a). The voltages on the five capacitors and the output voltage can be calculated using (48) and (51).

$$V_o = M_{DCM} \times V_{in} = \left(1 + \sqrt{1 + \left(\frac{d^2}{2K}\right)}\right) \times V_{in} = \left(1 + \sqrt{1 + \left(\frac{0.4^2}{2 \times 6.25 \times 10^{-3}}\right)}\right) \times 150 \approx 707 \text{ V} \quad (74)$$

$$\begin{cases} V_{C1} = V_{C4} = V_{C5} = \frac{V_{in} + V_o}{3} = \frac{150+707}{3} = 285.7 \text{ V} \\ V_{C2} = V_{C3} = \frac{V_o - 2V_{in}}{3} = \frac{707 - 2 \times 150}{3} = 135.7 \text{ V} \end{cases} \quad (75)$$



(a) (b) (c)

(d) (e) (f)

Figure 5.14: Experimental results for case study II.

The experimental results in Figure 5.15(b) and (c) closely agree with the calculated values in (74) and (75). The peak switch and diodes currents can be obtained by means of (44), (54), and (55), as shown in (76).

The experimental results in Figure 5.15(e) and (f) are close to the values calculated by (76). The spikes in the switch and diode currents are mainly caused by the capacitive charges of the SiC Schottky diodes.

$$\begin{cases} i_{D1(peak)} = i_{D2(peak)} = i_{D3(peak)} = \dfrac{d\,V_{in}}{3f_s\,L_{eq}} = \dfrac{0.4\times150}{3\times10^5\times125\times10^{-6}} = 1.6\text{ A} \\ i_{d4(peak)} = \dfrac{2V_o}{d\,R} = \dfrac{2\times707}{0.4\times2000} \approx 1.8\text{ A} \\ i_{Q(peak)} = \dfrac{d\,V_{in}}{f_s\,L_{eq}} = \dfrac{0.4\times150}{10^5\times125\times10^{-6}} = 4.8\text{ A} \end{cases} \quad (76)$$

5.10 Conclusion

A new single-switch step-up dc-dc converter that utilizes a switched-capacitor multiplier and an integrated LC^2D output network was proposed for fuel cell vehicles in this chapter. The proposed converter has a wide voltage gain range to suit the wide voltage swings of the fuel cell. The voltage stress on the semiconductor devices of the proposed converter is less than half of the output voltage, which enables the utilization of a power switch with lower rated voltage. In addition, the input current ripple is low and the potential difference between the grounds of its input and output terminals is a constant voltage, which prolongs the lifetime of the fuel cell and reduces the radiated EMI. A 1.3 kW 800 V prototype was built using a GaN transistor and SiC diodes, and the experimental measurements verified the theoretical analysis.

Chapter 6 A New SEPIC-Based Step-Up DC-DC Converter with Wide Conversion Ratio for Fuel Cell Vehicles: Analysis and Design

6.1 Introduction

In this chapter, a new SEPIC-based step-up dc-dc converter which integrates discontinuous-current quasi-Z-source (qZS) and switched-capacitor networks is proposed. The proposed converter has a low input current ripple, wide voltage gain range, low voltage stress on the semiconductor devices, and a constant potential difference between the grounds of its input and output ports. These features make the proposed converter an excellent interface between the fuel cell and the dc-link bus inside the electric vehicle. The analysis of the proposed converter for steady-state operations in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are given. Finally, a 3-kW/800-V scaled-down prototype was built using a Gallium Nitride (GaN) power switch and Silicon Carbide (SiC) diodes to validate the feasibility of the proposed converter and its theoretical analysis.

6.2 Structure and Operating Principles of the Proposed Converter

6.2.1 Configuration of the Proposed Converter

The proposed step-up dc-dc converter topology is shown in Figure 6.1, and it is composed of one power switch (Q), five diodes ($D_1 \rightarrow D_5$), seven capacitors ($C_1 \rightarrow C_7$), and three inductors ($L_1 \rightarrow L_3$). The fuel cell is represented by a voltage source (V_{in}), and the load is represented by a resistance (R). The proposed converter is based on the conventional SEPIC converter, as Q is the main switch, L_1 is the input inductor, D_1 is the output diode, and C_6 is the energy transfer capacitor of the conventional SEPIC. The second inductor of the conventional SEPIC is replaced by a discontinuous-current qZS network (L_2, L_3, D_2, C_2, C_7). In addition, a switched-capacitor network ($D_3 \rightarrow D_5$, $C_3 \rightarrow C_5$) is utilized. The capacitors of the qZS and the switched-capacitor networks

are stacked in-series with the output capacitor of the conventional SEPIC to enhance the voltage gain of the proposed converter, and reduce the voltage stresses on the semiconductor devices and capacitors.

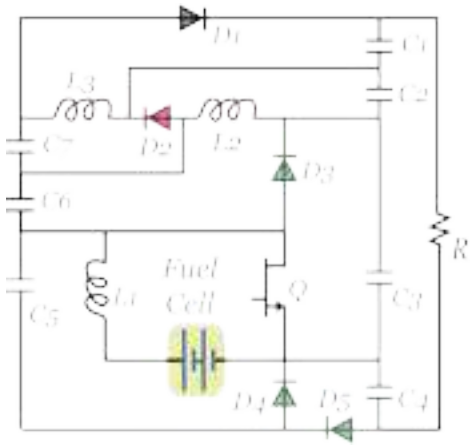


Figure 6.1: The schematic of the proposed converter.

6.2.2 Switching States Analysis

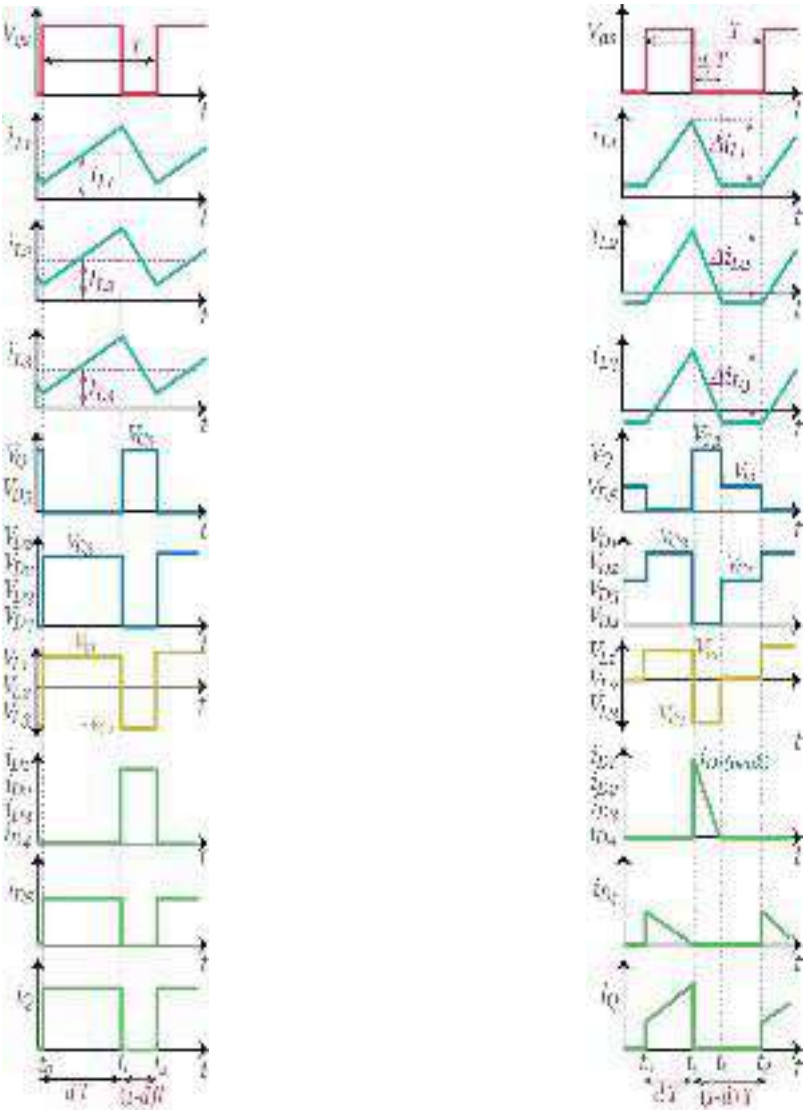
The proposed converter has two switching states, namely: State 0, and State 1. In State 1, *Q* is on, $D_1 \rightarrow D_4$ are off, and D_5 is on. In this switching state, C_1, C_2, C_3, and C_5 discharge, while C_4, C_6, and C_7 charge. Figure 6.3(a) shows the current flow paths during switching state 1. By means of *Kirchhof's Voltage Law* (KVL), and the equivalent circuit shown in Figure 6.3(a), we can deduce the following relationships:

$$\begin{cases} V_{L1} = V_{in} \\ V_{L2} = V_{C3} - V_{C6} \\ V_{L3} = V_{C2} + V_{C3} - V_{C6} - V_{C7} \\ V_{C4} = V_{C5} \end{cases} \quad (1)$$

In State 0, *Q* is off, $D_1 \rightarrow D_4$ are on, and D_5 is off. In this switching state, C_1, C_2, C_3, and C_5 charge, while C_4, C_6, and C_7 discharge. Figure 6.3(b) shows the current flow paths during switching

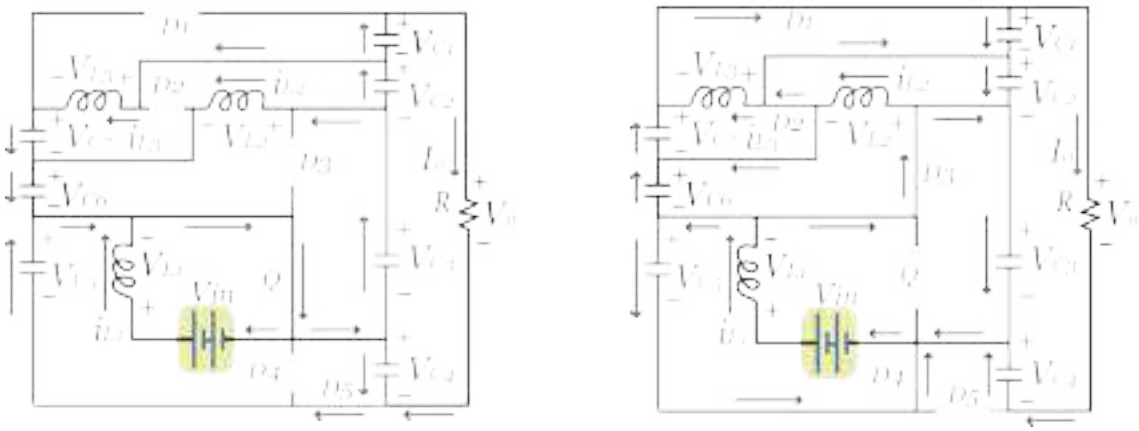
state 0. By applying the KVL rule on the equivalent circuit shown in Figure 6.3(b), we get the following relationships:

$$\begin{cases} V_{L1} = V_{in} - V_{C3} = V_{in} - V_{C5} \\ V_{L2} = -V_{C2} = -V_{C6} \\ V_{L3} = -V_{C1} = -V_{C7} \end{cases} \quad (2)$$



(a) (b)

Figure 6.2: Figure 6.2: Key waveforms of the proposed converter. (a) CCM operation. (b) DCM operation.



(a) (b)

Figure 6.3: Equivalent circuits of the proposed converter (a) During State 1. (b) During State 0.

6.2.3 Analysis of Voltage Gain and Voltage Stress

By means of equations (1) and (2), and by applying the voltage second balance rule on the three inductors, where the period of State 1 is dT and the period of State 0 is $(1\text{-}d)T$, as shown in Figure 6.2(a), where T is the switching periodic time, and d is the duty cycle, we get the following relationships:

$$\begin{aligned} &V_{C1} = V_{C2} = V_{C6} = V_{C7} = \frac{dV_{in}}{1-d} \\ &V_{C3} = V_{C4} = V_{C5} = \frac{V_{in}}{1-d} \\ &V_o = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \left(\frac{2+2d}{1-d}\right) V_{in} \\ &M = \frac{V_o}{V_{in}} = \frac{2+2d}{1-d} \end{aligned} \tag{3}$$

Where M is the voltage gain of the converter, V_{in} and V_o are the input and output voltages, $V_{C1} \rightarrow V_{C7}$ are the voltages across the capacitors $C_1 \rightarrow C_7$. By means of Figure 6.3, the voltage stress across the semiconductor devices can be deduced, as following:

$$V_Q = V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = \frac{V_{in}}{1-d} \tag{4}$$

Using (3) and (4), the voltage stress on the semiconductor devices can be expressed as a function on V_o and M, as follows:

$$V_Q = V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = \left(\frac{2+M}{4M}\right) V_o \tag{5}$$

6.2.4 Analysis of Current Stress

Assuming a lossless operation of the converter (i.e. $V_{in} \times I_{L1} = V_o \times I_o$), thus, the currents I_{L2}, I_{L3}, and I_{L1} can be calculated as in (6) and (7), where I_o is the output current:

$$I_{L2} = I_{L3} = I_o = \frac{V_o}{R} \tag{6}$$

$$I_{L1} = \left(\frac{2+2d}{1-d}\right) I_o = \left(\frac{2+2d}{1-d}\right) \frac{V_o}{R} \tag{7}$$

By applying the *Kirchhof's Current Law* (KCL) on the equivalent circuits of the proposed converter, shown in Figure 6.3, the current stresses on the power switch and diodes can be deduced as follows:

$$i_Q = \left(\frac{1+3d}{d(1-d)}\right) I_o = \left(\frac{(M-1)(M+2)}{M-2}\right) I_o \tag{8}$$

$$i_{D1} = i_{D2} = i_{D3} = i_{D4} = \frac{I_o}{1-d} = \left(\frac{M+2}{4}\right) I_o \tag{9}$$

$$i_{D5} = \frac{I_o}{d} = \left(\frac{M+2}{M-2}\right) I_o \tag{10}$$

6.2.5 Influence of the Parasitic Elements on Voltage Gain

In order to investigate the effect of the parasitic elements of the passive and active components on the voltage gain of the proposed converter, some of these elements were taken into account in the model of the converter. The circuit of the proposed converter with the included parasitic elements is shown in Figure 6.4. In this non-ideal converter model, the following parasitic elements were included: the series resistances of the inductors ($r_{L1} = r_{L2} = r_{L3} \approx r_L$), the equivalent series resistances of the capacitors ($r_{C1} = r_{C2} = r_{C3} = r_{C4} = r_{C5} = r_{C6} = r_{C7} \approx r_C$), the on resistance of

the power switch(r_S), the forward resistances of the diodes ($r_{D1} = r_{D2} = r_{D3} = r_{D4} = r_{D5} \approx r_D$), and their respective forward voltages ($V_{F1} = V_{F2} = V_{F3} = V_{F4} = V_{F5} \approx V_F$). The values for the operating and assumed parasitic parameters are as follows: $V_{in} = 100$, $r_L = 35\ \text{m}\Omega, r_C = 200\ \text{m}\Omega$, $r_D = 80\ \text{m}\Omega$, $r_S = 25\ \text{m}\Omega$, $V_F = 1.3\ \text{V}, R = 300\ \Omega$. When these parasitic elements are taken into account, a new equation can be deduced to describe the static voltage gain of the proposed converter $(M^{`})$, as shown in (11).

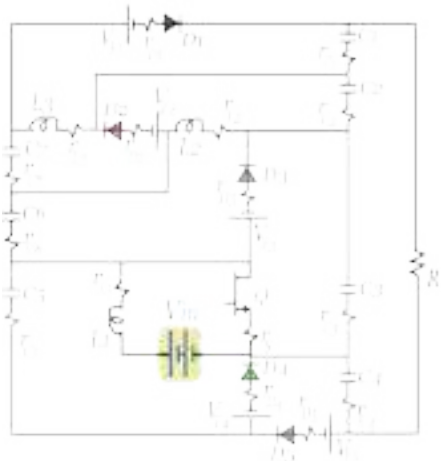


Figure 6.4: The proposed converter with the parasitic elements.

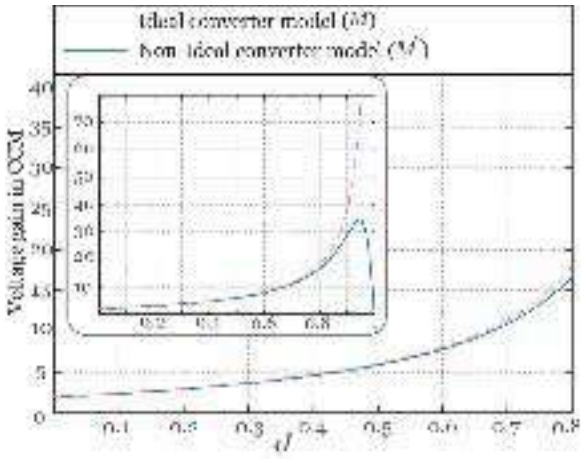


Figure 6.5: Static voltage gain curves for the ideal/non-ideal models of the proposed converter.

Figure 6.5 shows the voltage gain curves of the proposed converter described by the ideal and non-ideal models of the converter. It is noticed that the ideal and non-ideal models of the proposed converter are close to each other for $d = 0 \rightarrow 0.75$, as $M` \approx 13$ at $d = 0.75$, which shows the capability of the proposed converter to achieve high step-up voltage gains.

$$M` = \frac{R(1-d)(V_{in} - 3V_F + 3d\,V_F + 2d\,V_{in})}{V_{in}[R + 4r_D(1-d) + 4r_S + 6r_L + 2d(6r_C + 2r_L + 6r_S - R) + d^2(R + 6r_L - 2r_C - 10r_C d)]} \quad (11)$$

6.2.6 Efficiency Analysis

Calculating the different power losses in the components of the converter is essential to properly select the cooling system. The total power loss P_{Loss} of the proposed converter can be calculated by (12), where P_{Q_sw}, P_{Q_cond}, P_D, P_{L_cond}, P_{L_core}, and P_C are the switching and conduction losses of the power switch, the conduction loss of the diodes, the conduction and core losses of the inductors, and the conduction loss of the capacitors.

$$P_{loss} = P_{Q\_sw,} + P_{Q\_cond} + P_D + P_{L\_cond} + P_{L\_core} + P_C \quad (12)$$

The losses of the power switch Q can be calculated as follows:

$$P_{Q\_sw} = f_s(0.5V_Q i_Q(t_r + t_f) + 0.5{V_s}^2 C_{OSS}) \quad (13)$$

$$P_{Q\_cond} = \left(\left(\frac{1+3d}{\sqrt{d}(1-d)}\right) I_o\right)^2 R_{DS} \quad (14)$$

Where f_s, R_{DS}, t_r, t_f, and C_{OSS}, are the switching frequency, on resistance, rise time, fall time, and the parasitic output capacitance of Q, respectively.

The losses of the inductors can be derived using (15), and (16), where R_{L1}, R_{L2}, R_{L3}, l_{c1}, l_{c2}, l_{c3}, A_{c1}, A_{c2}, A_{c3}, ΔB_1, ΔB_2, and ΔB_3 are the equivalent series resistances of the three inductors, the magnetic flux path lengths of the cores of the three inductors, the cross sectional areas of the cores of the three inductors, and the three inductor's ac magnetic flux density.

$$P_{L\_cond} = \sum_{n=1}^{n=3} I_{Ln}^2 \, R_{Ln} \tag{15}$$

$$P_{L\_core} = \sum_{n=1}^{n=3} l_{cn} \, A_{cn} \, (a \, \Delta B_n^b \, f_n^c) \tag{16}$$

Equation (16), is the Steinmetz equation and it is an empirical formula, where *a*, *b*, and *c* are fitting parameters and can be gotten from the core manufacturer datasheet.

The conduction losses of the five diodes can be calculated by means of (17), as follows:

$$P_D = 5 \, V_{fd} \, I_o \tag{17}$$

Where V_{fd} is the forward voltage of each diode. The conduction loss of the capacitors can be extracted as following:

$$P_C = \sum_{n=1}^{n=7} I_{Cn\_rms}^2 \, ESR_{Cn} \tag{18}$$

Where $ESR_{C1} \rightarrow ESR_{C7}$ and $i_{C1\_rms} \rightarrow i_{C7\_rms}$, are the equivalent series resistances and the rms currents of the seven capacitors, respectively. The rms currents of the seven capacitors can be calculated by (19)-(23).

$$\boldsymbol{i_{C1\_rms} = i_{C7\_rms} = I_o\sqrt{\frac{d}{1-d}}} \tag{19}$$

$$\boldsymbol{i_{C2\_rms} = i_{C6\_rms} = 2I_o\sqrt{\frac{d}{1-d}}} \tag{20}$$

$$\boldsymbol{i_{C3\_rms} = 3I_o\sqrt{\frac{d}{1-d}}} \tag{21}$$

$$\boldsymbol{i_{C4\_rms} = I_o\sqrt{\frac{1-d}{d}}} \tag{22}$$

$$\boldsymbol{i_{C5\_rms} = I_o\sqrt{\frac{1}{d(1-d)}}} \tag{23}$$

Finally, the converter's efficiency η can be calculated using (24):

$$\eta = \frac{MV_{in}\, I_o}{MV_{in}\, I_o + P_{Loss}} \tag{24}$$

6.2.7 DCM Operation Steady-State Analysis

In DCM operation, the off state of the transistor is split into two states, the first state has a time period of d_zT, where d_z is a fraction of the periodic switching time T, and this state is similar to State 0 in CCM operation where $D_1 \rightarrow D_4$ conduct when Q is off. The second state during the off state of Q takes place when the voltages across the inductors drop to zero and all the diodes are reverse-biased, as shown in Figure 6.6. During this state, positive constant current flows in L_1 while negative constant currents flow in L_2 and L_3. All the important theoretical waveforms of the proposed converter during the DCM operation are shown in Figure 6.2(b).

Since the average current of each of the five diodes equals the output current, thus, d_z can be derived as following:

$$\frac{1}{2T} d_z T i_{D(peak)} = \frac{V_o}{R} \tag{25}$$

Where $i_{D(peak)}$ is the peak current of any diode of D_1, D_2, D_3, and D_4, and it can be calculated by (26).

$$i_{D(peak)} = \frac{dV_{in}}{4 f_s L_{eq}} \tag{26}$$

As L_{eq} is defined by (27).

$$L_{eq} = \left[\frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}\right]^{-1} \tag{27}$$

Accordingly, d_z can be deduced as given in (28).

$$d_z = \frac{8V_o}{dV_{in}} \frac{f_s L_{eq}}{R} = \frac{8V_o}{dV_{in}} K \tag{28}$$

Where K is a dimensionless parameter and it is defined by (29).

$$K = \frac{f_s L_{eq}}{R} \tag{29}$$

By means of Figure 6.2(b), and applying the voltage second rule on any of the three inductors we get (30)-(31), where M_{DCM} is the voltage gain of the proposed converter in DCM operation.

$$\frac{1}{T}\left[\int_0^{dT} V_{in}\, dt - \int_0^{d_z T} V_{C1}\, dt\right] = 0 \tag{30}$$

$$V_{in} d + \left(\frac{2V_{in} - V_o}{4}\right) d_z \tag{31}$$

$$M_{DCM}^2 - 2M_{DCM} - \frac{d^2}{2K} = 0 \tag{32}$$

By solving the quadratic equation (32), M_{DCM} can be extracted.

$$M_{DCM} = \frac{V_o}{V_{in}} = 1 + \sqrt{1 + \frac{d^2}{2K}} \tag{33}$$

In order to get the boundary condion between the DCM and CCM operations, M_{CCM} equals M_{DCM}. Hence, the critical value of K ($K_{critical}$) is defined by (34), and plotted versus d in Figure 6.7, as the converter operates in DCM when $K < K_{critical}$, and in *CCM* otherwise.

$$K_{critical} = \frac{d(1-d)^2}{8(d+2)} \tag{34}$$

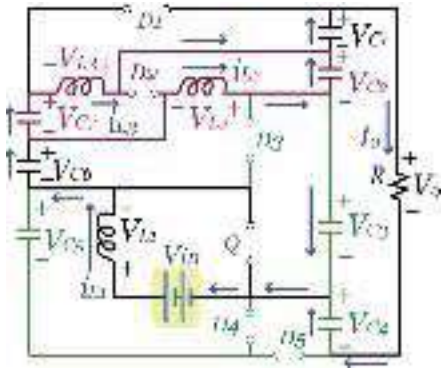


Figure 6.6: Current flow paths during the third switching state (in DCM).

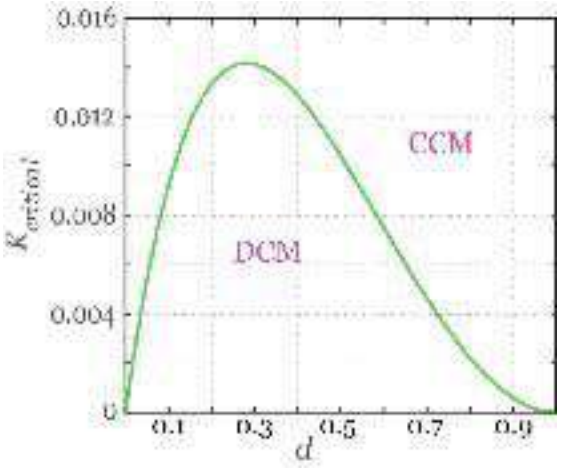


Figure 6.7: Boundary condition between CCM and DCM operations for the proposed topology.

6.3 Component Parameters Design

6.3.1 Design of the Semiconductor Devices

The selected power switch should tolerate the maximum voltage and current stresses applied to it. Equations (5) and (8) describe the current and voltage stresses on the switch, hence, by knowing the output voltage and current and the maximum voltage gain, the maximum current and voltage stresses can be determined. These maximum stress values should be within the safe operating area (SOA) of the selected power switch. Similarly, the maximum voltage and current stresses on the diodes can be calculated via (5) and (9), and accordingly the ratings of the selected diodes can be determined.

6.3.2 Design of Inductors

Using equations (6) and (7), the three inductors' currents can be deduced. By knowing the maximum ripple currents Δi_{L1}, Δi_{L2}, and Δi_{L3}, the minimum required inductances can be determined using (35), where *d* is the duty cycle, and f_s is the switching frequency.

$$\begin{cases} L_1 \geq \dfrac{dV_{in}}{f_s \Delta i_{L1}} \\ L_2 \geq \dfrac{dV_{in}}{f_s \Delta i_{L2}} \\ L_3 \geq \dfrac{dV_{in}}{f_s \Delta i_{L3}} \end{cases} \tag{35}$$

6.3.3 Design of Capacitors

Using equation (3), the voltages of the seven capacitors can be determined. By knowing the maximum ripple voltages ΔV_{C1}, ΔV_{C2}, ΔV_{C3}, ΔV_{C4}, ΔV_{C5}, ΔV_{C6} and ΔV_{C7}, the minimum required capacitances can be determined using (36).

$$\begin{cases} C_1 \geq \dfrac{I_o d}{f_s \Delta V_{C1}} \\ C_2 \geq \dfrac{2 I_o d}{f_s \Delta V_{C2}} \\ C_3 \geq \dfrac{3 I_o d}{f_s \Delta V_{C3}} \\ C_4 \geq \dfrac{I_o (1-d)}{f_s \Delta V_{C4}} \end{cases} , \quad \begin{cases} C_5 \geq \dfrac{I_o}{f_s \Delta V_{C5}} \\ C_6 \geq \dfrac{2 I_o d}{f_s \Delta V_{C6}} \\ C_7 \geq \dfrac{I_o d}{f_s \Delta V_{C7}} \end{cases} \tag{36}$$

6.4 Comparative Study

In this section, the proposed converter is compared with seven other step-up dc-dc converter architectures. These other dc-dc topologies are: the 3LB converter, and the converters in [110], [177], [178], [180], [188], and [189]. Table 6.1 summarizes the number of passive and active components, the voltage gain, and the maximum normalized voltage stresses across the switches and diodes of each converter. Also, it shows whether the converter has low input current ripple or not, and the potential difference between the grounds of the input and output ports of each converter. The voltage gain of the compared converters is plotted versus the duty cycle in Figure 6.8, while the maximum normalized voltage stress on the switches and diodes of the compared converters are graphed in Figure 6.9 and Figure 6.10, respectively.

The 3LB converter, the converters in [110], [178], and [189] have HF PWM potential difference between the input and output grounds, which may increase the radiated EMI noise and the leakage currents of the converters, and accordingly an extra periodic maintenance may be required. The converters in [110], [180], and [189] have a pulsating input current which can affect the lifetime of the fuel cell.

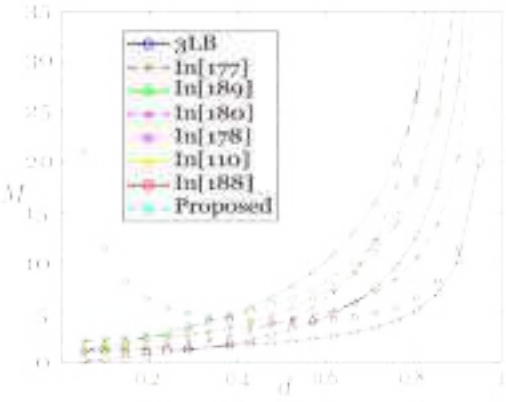


Figure 6.8: Voltage gain curves of the compared converters.

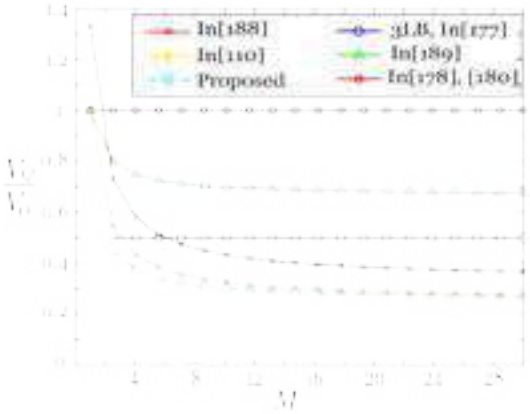


Figure 6.9: Maximum normalized voltage stress on the switches of the compared converters.

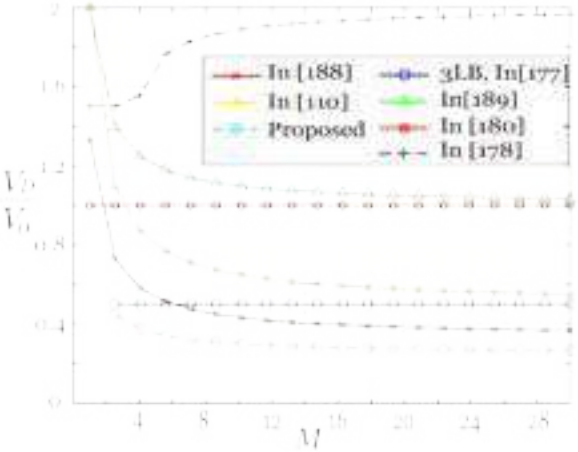


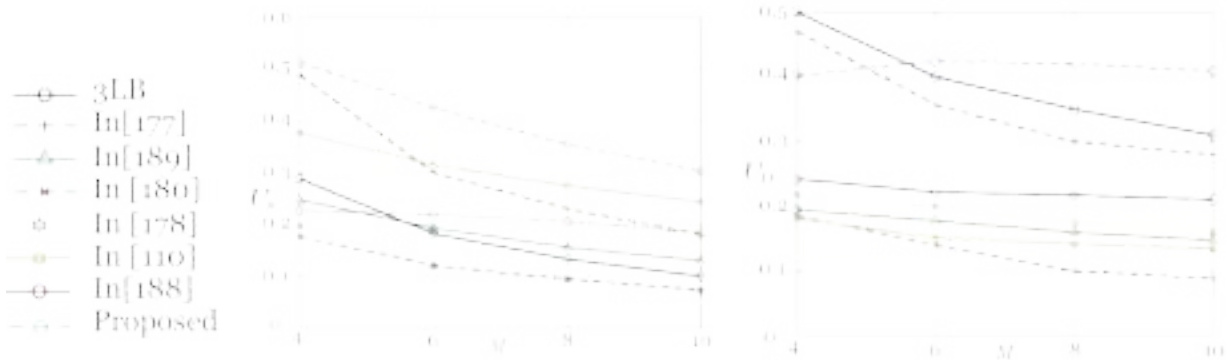
Figure 6.10: Maximum normalized voltage stress on the diodes of the compared converters.

Figure 6.8 shows that the proposed converter has a higher voltage gain compared to the 3LB converter and the converters in [110], [188], [177], [178] (for d >0.35), [189] (for d <0.35), and [180] (for d <0.7). Regarding the voltage stress on the power switches and diodes of the compared

converters, Figure 6.9 and Figure 6.10 show that the proposed converter has the least maximum voltage stress on its switch and diodes compared to the converters in Table 6.1. In order to properly compare the estimated cost of the power switches and diodes of each converter, the utilization factor of the switches (U_S) and the utilization factor of the diodes are calculated by (37) and (38), respectively.

$$U_S = \frac{P_o}{\sum V_{Qi}\, i_{Qi\,(rms)}} \tag{37}$$

$$U_D = \frac{P_o}{\sum V_{Dj}\, i_{Dj\,(rms)}} \tag{38}$$



(a) (b)

Figure 6.10: (a) Utilization factor of power switches. (b) Utilization factor of diodes.

Where P_o is the output power of the converter, $V_{Qi,}\, i_{Qi(rms)}$ are the voltage and the root-mean-square (rms) current stresses on switch i, $V_{Di,}\, i_{Di(rms)}$ are the voltage and the rms current stresses on diode j. The utilization factors for the power switches and diodes of the converters in Table 6.1 are graphically presented versus the voltage gain in Figure 6.11 when P_o is 3kW and V_o is 800V. It is clear from Figure 6.11(a) that the proposed converter has the highest switch utilization factor. Figure 6.11(b) shows that the proposed converter has higher diode utilization factor compared to the converters in [110], [188], [178], [180], and [189], while it has higher diode utilization factor compared to the 3LB converter and the converter in [177] for $M > 5$.

The comparisons above show that the proposed converter integrates a number of features such as: high voltage conversion ratio, wide input voltage range, low voltage stress on the semiconductor devices, low input current ripple, constant voltage difference between its input and output ports' grounds, and high utilization of the semiconductor devices. These features make the proposed topology an excellent interface between the fuel cell and the dc-link bus of the inverter of the EV.

Table 6.1: COMPARISON BETWEEN THE PROPOSED AND OTHER STEP-UP DC-DC SOLUTIONS

Topology	Voltage gain (M)	Maximum voltage stress across switches	Maximum voltage stress across diodes	Number of semiconductor devices	Number of inductors & capacitors	Input current ripple	Grounds' potential difference	Voltage gain range d : 0 →0.9
3LB	$\frac{1}{1-d}$	$\frac{1}{2}$	$\frac{1}{2}$	2 Switches 2 Diodes	1 Inductor 2 Capacitors	Low	HF PWM voltage	1→10
In [110]	$\frac{1+3d}{1-d}$	$\frac{3+M}{4M}$	$\frac{3+M}{2M}$	2 Switches 2 Diodes	3 Inductors 3 Capacitors	High	HF PWM voltage	1→37
In [188]	$\frac{3d}{1-d}$	$\frac{3+M}{3M}$	$\frac{3+M}{3M}$	1 Switch 3 Diodes	4 Inductor 6 Capacitors	Low	0 V	0→27
In [178]	$\frac{1}{d(1-d)}$	1	$\frac{3}{2}+\sqrt{\frac{1}{4}-\frac{1}{M}}$	2 Switches 3 Diodes	2 Inductors 2 Capacitors	Low	HF PWM voltage	-- →11
In [180]	$\frac{1}{(1-d)^2}$	1	1	1 Switch 3 Diodes	2 Inductors 2 Capacitors	High	0 V	1→100
In [189] (n=1)	$\frac{1+5d}{1-d}$	$\frac{1+2M}{3M}$	$\frac{1+M}{M}$	3 Switches 12 Diodes	6 Inductor 1 Capacitors	High	HF PWM voltage	1→55
In [177]	$\frac{2}{1-d}$	$\frac{1}{2}$	$\frac{1}{2}$	2 Switches 3 Diodes	2 Inductors 3 Capacitors	Low	Constant voltage	2→20
Proposed	$\frac{2+2d}{1-d}$	$\frac{2+M}{4M}$	$\frac{2+M}{4M}$	1 Switch 5 Diodes	3 Inductors 7 Capacitors	Low	Constant voltage	2→38

6.5 Experimental Results and Analysis

A scaled-down 3-kW/800-V experimental prototype was built to verify the feasibility of the proposed topology and the correctness of its theoretical analysis, as shown in Figure 6.12. The

power circuit of the prototype was built using a GaN power switch (GS66516T-E02-MR) and SiC Schottky diodes (IDDD10G65C6XTMA1), and controlled by a TMS320f28335 microcontroller. The currents of the inductors, diodes, and power switch are measured via current sense resistors. The operating frequency is 100 kHz, and the selected values of the three inductors and seven capacitors are enlisted in Table 6.2.

Table 6.2: MAIN EXPERIMENTAL PARAMETERS OF THE PROPOSED CONVERTER

Parameters and Components	Values
Rated power P_o	3-kW
Output voltage V_o	800-V
Power switch Q	GS66516T-E02-MR (2-in-parallel)
Diodes $D_1 \rightarrow D_5$	IDDD10G65C6XTMA1
Inductor L_1	250 µH
Inductors L_2, L_3	330 µH
Capacitors C_1, C_2, C_6, C_7	180 µF
Capacitors C_3, C_4, C_5	150 µF
Load resistor	215 Ω
Switching frequency f_s	100 KHz
Microcontroller	TMS320f28335

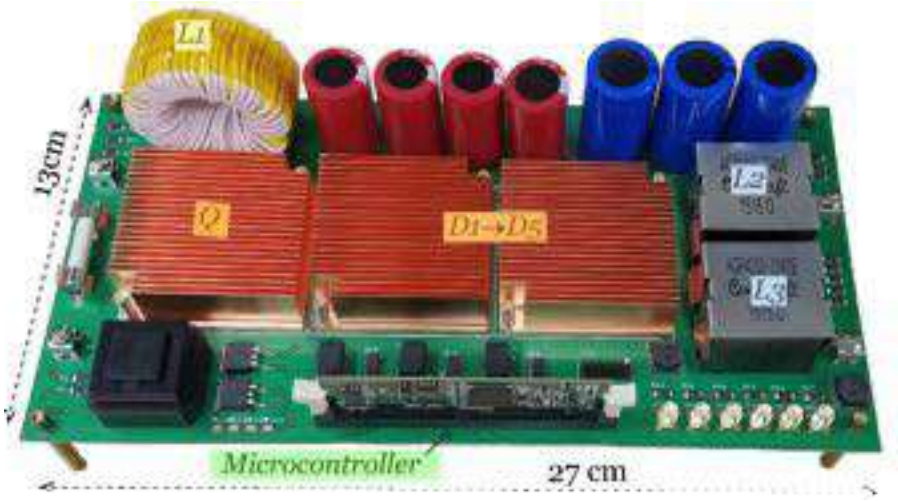
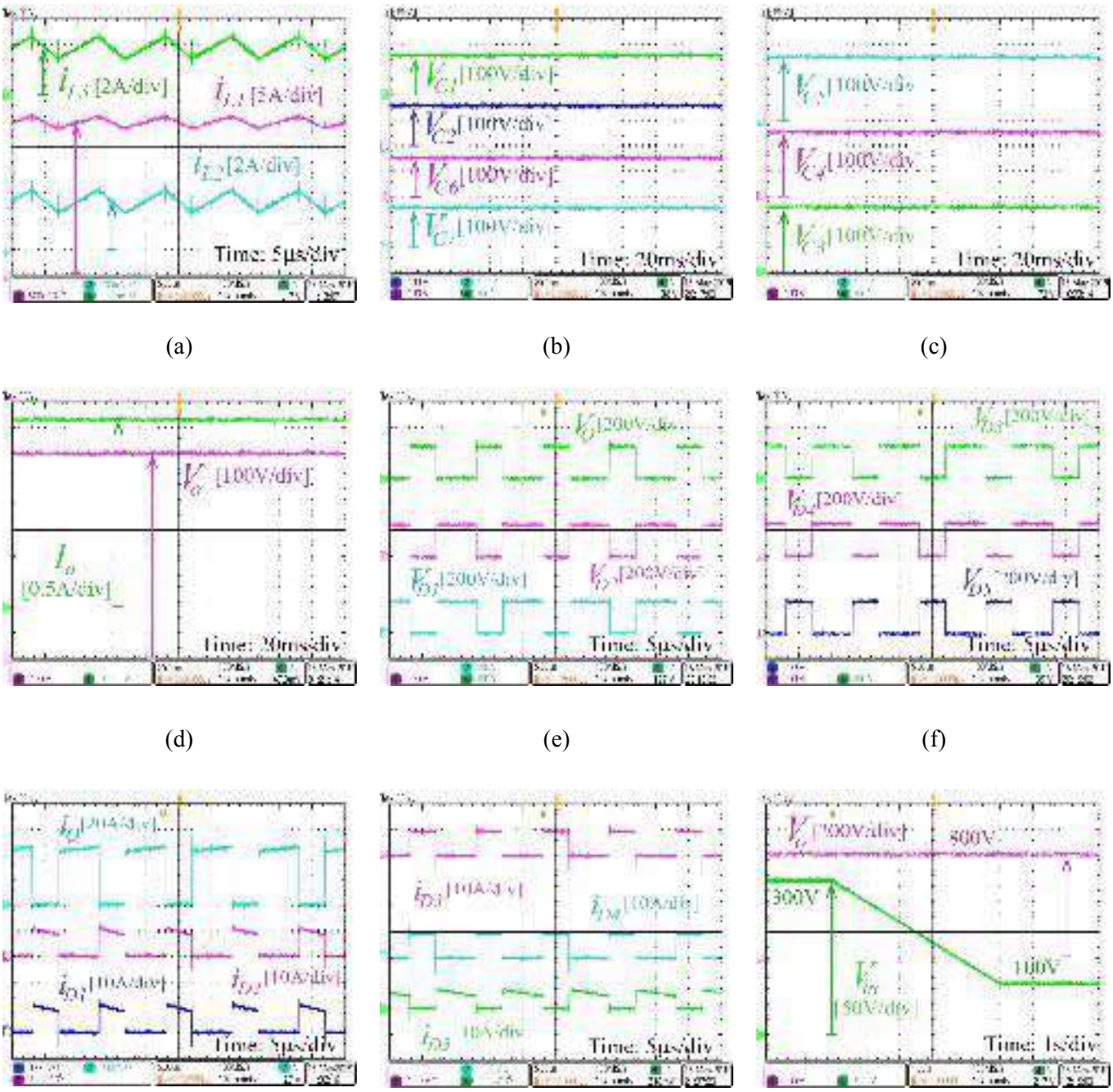


Figure 6.11: Experimental prototype.

The operating parameters are as following: V_{in} = 100V, R = 215Ω, d = 0.6. The experimental test results are presented in Figure 6.13.

The voltage gain and the output voltage of the developed converter can be calculated using equation (3), as following: M = 8, V_o = 800V, which closely agrees with the experimental results in Figure 6.13(d). Similarly, the voltages across the seven capacitors can be calculated by (3) as: $V_{C1} = V_{C2} = V_{C6} = V_{C7}$ = 150V, and $V_{C3} = V_{C4} = V_{C5}$ = 250V, which closely agree with the results shown in Figure 6.13(b) and Figure 6.13(c).

The inductor currents and their respective ripple currents can be calculated by (6), (7), and (35), as follows: $I_{L1} \approx 29.77$A, $I_{L2} = I_{L3} \approx 3.72$A, Δi_{L1}= 2.4A, $\Delta i_{L2} \approx 1.8$A, $\Delta i_{L3} \approx 1.8$A, which is close to the experimental results shown in Figure 6.13(a). The voltage stress across the power switch and the five diodes can be calculated by equation (4), as follows: $V_Q = V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5}$ = 250V, which comply with the experimental results shown in Figure 6.13(e) and Figure 6.13(f).



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 6.12: Experimental results.

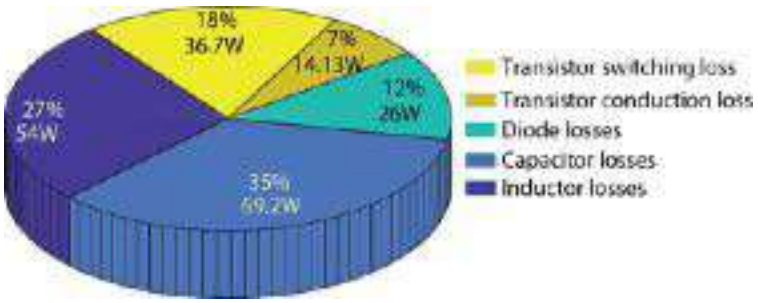


Figure 6.13: Distributions of the calculated power loss for the experiment

The current stress of the power switch *Q* can be calculated via equation (8), as: $i_Q \approx 43.4\text{A}$, which closely agrees with the experimental results presented in Figure 6.13(g). Similarly, the current stresses of the five diodes can be calculated by equations (9) and (10), as: $i_{D1} = i_{D2} = i_{D3} = i_{D4} \approx 9.3\text{A}$, and $i_{D5} \approx 6.2\text{A}$, which comply with the experimental results in Figure 6.13(g) and Figure 6.13(h).

To evaluate the wide input voltage capability of the proposed converter, the input voltage of the converter is changed gradually from 300V to 100V, while a closed-loop Type III voltage controller is utilized to set the output voltage of the converter at 800V. Figure 6.13(i) shows the result of this test where the output voltage is fixed at 800V while the input voltage changed from 300V to 100V. This result shows that proposed converter has an acceptable dynamic performance with wide changes in the input voltage.

The calculated losses of the active and passive components of the proposed converter for the case study investigated in this section (V_{in} = 100V, V_o = 800V, d = 0.6, f_s = 100kHz, R = 215Ω), is shown in Figure 6.14. The total calculated losses P_{loss} equal 197.37W. The conduction losses of the capacitors account for 35% of the total converter losses (replacing the electrolytic capacitors used in the experimental prototype with film or ceramic capacitors can reduce this loss segment).

The switching and conduction losses of the power switch account for 18% and 7%, respectively, of the total losses. The conduction losses of the diodes account for 12% of the converter losses.

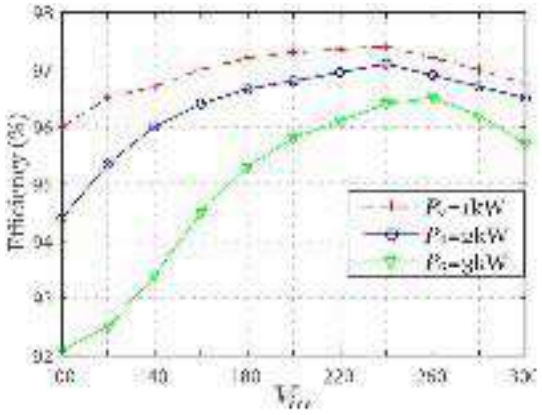


Figure 6.14: Measured efficiency curves of the proposed converter versus V_{in}

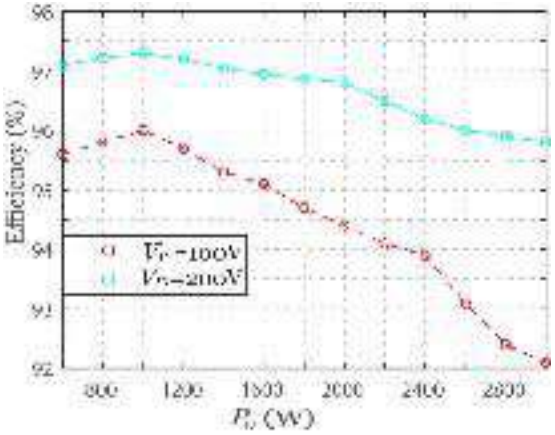


Figure 6.15: Measured efficiency curves of the proposed converter versus P_o

Finally, the conduction losses of the three inductors account for 27% of the total losses of the converter. Figure 6.15 shows the measured efficiency curves of the proposed converter versus the input voltage (V_{in} = 100 →300V), for P_o equals 1kW, 2kW, and 3kW. For P_o = 1kW curve, the minimum efficiency is 96% at V_{in} = 100V, and the maximum efficiency is 97.4% at V_{in} = 240V. For P_o = 2kW curve, the minimum efficiency is 94.4% at V_{in} = 100V, and the maximum efficiency is 97.1% at V_{in} = 240V. For P_o = 3kW curve, the minimum efficiency is 92.1% at V_{in} = 100V, and

the maximum efficiency is 96.5% at V_{in} = 260V. Figure 6.16 shows the measured efficiency curve of the developed prototype versus the output power. In this efficiency test, V_{in} = 100V and 200V, V_o = 800V, P_o = 600W → 3kW. In this test, when V_{in} = 100V, the maximum efficiency is 96% at P_o = 1kW, and the minimum efficiency is 92.1% at P_o = 3kW, while when V_{in} = 200V, the maximum efficiency is 97.3% at P_o = 1kW, and the minimum efficiency is 95.8% at P_o = 3kW.

6.6 Conclusion

A new SEPIC-based step-up dc-dc converter with embedded discontinuous-current quasi-Z-source and switched capacitor networks was proposed in this paper. The proposed topology has the advantages of continuous input current, high step-up voltage gain, wide-input-voltage range, constant potential difference between the grounds of the input and output ports, and low voltage stress on the semiconductor devices. These features make the proposed converter a suitable power electronic interface between the fuel cell and the dc-link of the inverter in the EV. Finally, a 3-kW/800-V prototype for the proposed topology was developed, and the theoretical analysis was validated by the experimental results.

Chapter 7 Design and Implementation of a New Transformerless Bidirectional DC-DC Converter with Wide Conversion Ratios

7.1 Introduction

A new transformerless bidirectional buck-boost converter is proposed in this chapter. The proposed converter has a simple circuit structure, low component count, low voltage stress on the power transistors, and a wide voltage gain range. This makes it applicable in the energy storage charge/discharge systems, such as the electric vehicles (EV), microgrids and nanogrids with energy storage units, and uninterruptible power supplies. In addition, synchronous rectification between the complementary transistors is employed to improve the converter efficiency. A comprehensive analysis of the steady-state operation, small-signal model, component parameters design, and efficiency analysis of the proposed converter operating in a continuous conduction mode (CCM) is given. Finally, a 1.6 kW scaled-down prototype was built using Silicon Carbide (SiC) MOSFETs to validate the effectiveness and feasibility of the proposed converter.

7.2 Structure and Operating Principle of the Proposed Converter

7.2.1 Configuration of the Proposed Converter

The configuration of the proposed BBB dc-dc converter is shown in Figure 7.1. It can be seen that the proposed converter is composed of three switches (Q_1, Q_2, and Q_3), two inductors (L_1, and L_2), four capacitors (C_1, C_2, C_3, and C_4), and two ports (port *A*, and port *B*). The converter can manage the power flow either from port *A* to port *B*, or from port *B* to port *A*. The signals G_1, G_2, and G_3 are the triggering signals of switches Q_1, Q_2, and Q_3, respectively. Synchronous rectification is employed, where G_2, and G_3 are identical and they are complementary to G_1. To simplify the analysis, the following assumptions are made: (a) All the components are ideal, thus, the on-resistance of the switches, and the equivalent series resistances of the inductors and

capacitors are ignored. (b) All the capacitors and inductors are large enough to apply the small ripple approximation.

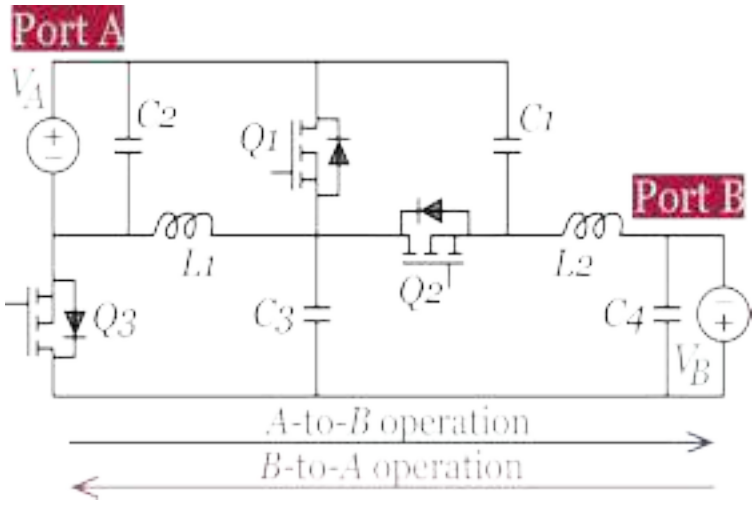


Figure 7.1: The schematic of the proposed converter.

7.2.2 A-to-B Operation of the Proposed Converter

In this operation, power flows from port *A* to port *B*. The equivalent circuit of this operation is shown in Figure 7.2, where a voltage source V_A is connected at port *A*, and a resistive load R_1 is connected at port *B*. The key waveforms for this operation are shown in Figure 7.4(a), as it has two switching states, namely: *State 0*, and *State 1*. In this operation, Q_1 is the main transistor and Q_2, and Q_3 are synchronous rectifiers.

There is a dead time between the rising edge of G_2, and G_3, and the falling edge of G_1. Another dead time is present between the falling edge of G_2, and G_3, and the rising edge of G_1. During these dead times, the current flows in the antiparallel diodes of Q_2, and Q_3, hence, the voltage across the drain and source of these transistors is close to zero. This provides zero-voltage-switching (ZVS) during turn-on and turn-off for Q_2, and Q_3, which enhances the converter efficiency.

1) State 0

In this switching state, Q_1 is turned on, and Q_2 and Q_3 are turned off. The period of this state is d_1T, where T is the periodic switching time, and d_1 is the duty cycle of Q_1. Figure 7.2(a) shows the current flow paths during this switching state, and according to it, the following equations can be derived:

$$\begin{cases} V_{L1} = V_A \\ V_{L2} = V_{C1} - V_B + V_{C3} \end{cases} \tag{1}$$

$$\begin{cases} i_{c1} = i_{c3} = -I_{L2} \\ i_{C4} = I_{L2} - \dfrac{V_B}{R_1} \end{cases} \tag{2}$$

2) State 1

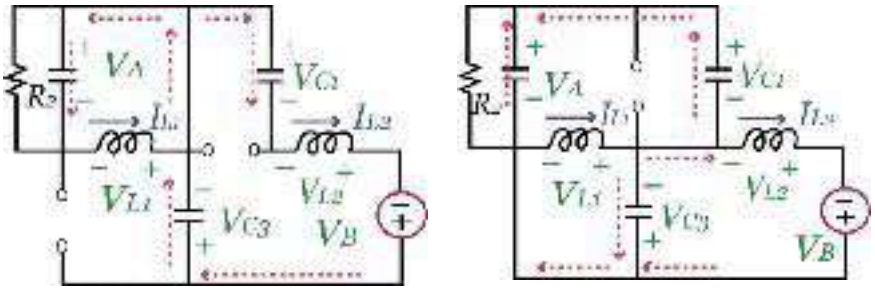
In this switching state, Q_1 is turned off, and Q_2 and Q_3 conduct current in the reverse direction. The period of this state is $d_2T = d_3T = (1-d_1)T$, where d_2 and d_3 are the duty cycle values of Q_2, and Q_3, respectively. Figure 7.2(b) shows the current flow paths during this switching state, and according to it, the following equations can be derived:

$$\begin{cases} V_{L1} = -V_{C3} = V_A - V_{C1} \\ V_{L2} = -V_B + V_{C3} \end{cases} \tag{3}$$

$$\begin{cases} i_{c1} = i_{C3} = \dfrac{I_{L1} - I_{L2}}{2} \\ i_{C4} = i_{L2} - \dfrac{V_B}{R_1} \end{cases} \tag{4}$$

(a) (b)

Figure 7.2: Current-flow paths of the proposed converter in the A-to-B operation. (a) State 0: G1 G2 G3 = 100. (b) State 1: G1 G2 G3 = 011.



(a) (b)

Figure 7.3: Current-flow paths of the proposed converter in the B-to-A operation. (a) State 0: G1 G2 G3 = 100. (b) State 1: G1 G2 G3 = 011.

3) Capacitor Voltages and Inductor Currents

From (1), and (3), and using the volt-second balance rule on inductors L_1, and L_2, the capacitor voltages, and the voltage gain for *A*-to-*B* operation M_{AB} can be derived as shown in (5), and (6), respectively:

$$\begin{cases} V_{c1} = \dfrac{V_A}{1-d_1} \\ V_{c3} = \dfrac{d_1}{1-d_1} V_A \\ V_B = \dfrac{2d_1}{1-d_1} V_A \end{cases} \tag{5}$$

$$M_{AB} = \frac{V_B}{V_A} = \frac{2d_1}{1-d_1} \tag{6}$$

From (2), and (4), and using the charge-second balance rule on capacitors C_1, C_3 and C_4, the inductor currents can be derived as shown in (7):

$$\begin{cases} I_{L1} = \dfrac{1+d_1}{1-d_1}\, I_{L2} \\ I_{L2} = \dfrac{V_B}{R_1} = \dfrac{2d_1}{(1-d_1)R_1} V_A \end{cases} \tag{7}$$

7.2.3 B-to-A Operation of the Proposed Converter

In this operation, power flows from port *B* to port *A*. The equivalent circuit of this operation is shown in Figure 7.3, where a voltage source V_B is connected at port *B*, and a resistive load R_2 is connected at port *A*. In this operation, Q_2, and Q_3 are the main power switches and Q_1 is a synchronous rectifier. Dead time is employed between the main switches and the synchronous rectifier, as shown in Figure 7.4(b), to provide ZVS during turn-on and turn-off for Q_1. The capacitor voltages, inductor current, and voltage gain M_{BA} for this operation can be derived from (5), (6), and (7), by replacing d_1 by (1-d_2), as following:

$$M_{BA} = \frac{V_A}{V_B} = \frac{d_2}{2(1-d_2)} \tag{8}$$

$$\begin{cases} V_{c1} = \dfrac{V_B}{2(1-d_2)} \\ V_{c3} = \dfrac{V_B}{2} \\ V_A = \dfrac{d_2}{2(1-d_2)} V_B \end{cases} \tag{9}$$

$$\begin{cases} I_{L1} = \dfrac{2-d_2}{d_2}\, I_{L2} \\ I_{L2} = \dfrac{V_A}{R_2} M_{BA} = \left(\dfrac{d_2}{2(1-d_2)}\right)^2 \dfrac{V_B}{R_2} \end{cases} \tag{10}$$

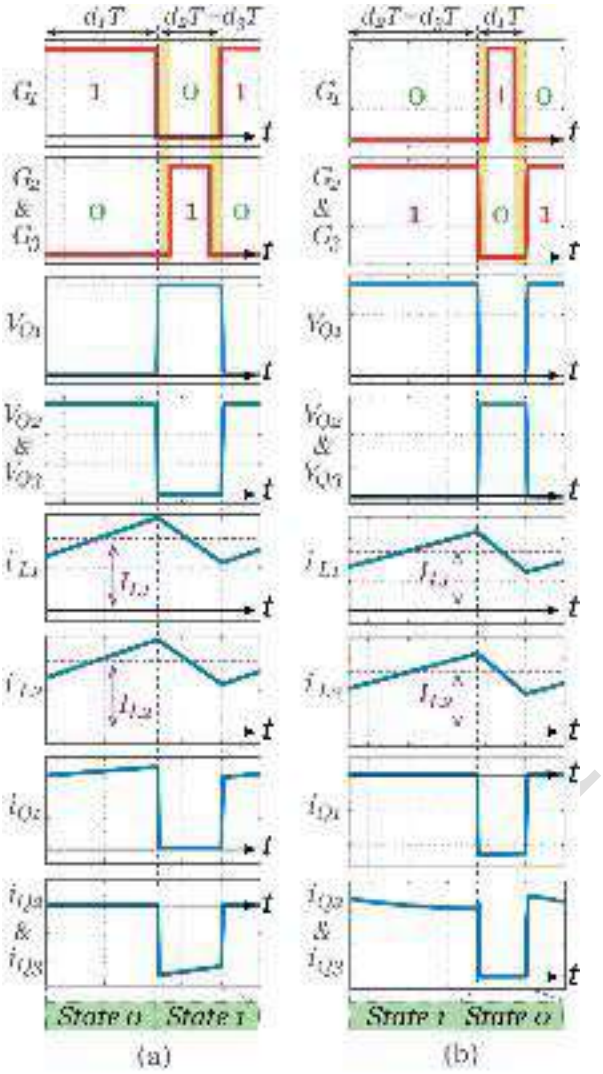


Figure 7.4: Typical waveforms of the proposed converter. (a) A-to-B operation. (b) B-to-A operation.

7.2.4 Switches, Capacitors, and Inductors design

1) Switches Selection:

Equations (11)-(13) describe the voltage and current stresses on Q_1, Q_2, and Q_3, respectively.

$$V_{Q1} = V_{Q2} = V_{Q3} = \frac{V_B}{2d_1} \tag{11}$$

$$I_{Q1} = I_{L1} + I_{L2} \tag{12}$$

$$I_{Q2} = I_{Q3} = \frac{I_{L1}+I_{L2}}{2} \tag{13}$$

The selected transistors should tolerate these voltage and current stresses.

12) Capacitors Selection:

Equations (5), and (9) describe the voltage stress across C_1, C_2, C_3, and C_4. The relationship between the capacitance of these capacitors and the associated ripple voltages is depicted in (14):

$$\begin{cases} C_1 = \dfrac{2{d_1}^2}{\Delta V_{C1} f_s (1-d_1) R_1} V_A = \dfrac{{d_2}^2}{4\Delta V_{C1} f_s (1-d_2) R_2} V_B \\ C_2 = \dfrac{{d_2}^3 V_B}{4 f_s R_2 \Delta V_{C4} (1-d_2)^2} \\ C_3 = \dfrac{2{d_1}^2}{\Delta V_{C3} f_s (1-d_1) R_1} V_A = \dfrac{{d_2}^2}{4\Delta V_{C3} f_s (1-d_2) R_2} V_B \\ C_4 = \dfrac{\Delta i_{L2}}{8 f_s \Delta V_{C4}} \end{cases} \quad (14)$$

By knowing the switching frequency, f_s, and the desired capacitor voltage ripples ΔV_{C1}, ΔV_{C2}, ΔV_{C3}, and ΔV_{C4}, the capacitance of C_1, C_2, C_3, and C_4 can be determined.

13) Inductors Selection:

Equations (7), and (10) calculate the currents the currents flowing in inductors L_1, and L_2. The relationship between the inductance of these inductors and the associated ripple currents is depicted in (15). These equations can be used to determine the inductance of L_1, and L_2, when the desired inductor current ripples Δi_{L1}, and Δi_{L2} are known.

$$\begin{cases} L_1 = \dfrac{V_A d_1}{f_s \Delta i_{L1}} = \dfrac{V_B d_2}{2 f_s \Delta i_{L1}} \\ L_2 = \dfrac{V_A d_1}{f_s \Delta i_{L2}} = \dfrac{V_B d_2}{2 f_s \Delta i_{L1}} \end{cases} \quad (15)$$

7.2.5 Comparison with Other Bidirectional Buck-Boost Converters

In this section, the proposed converter is compared with six other BBB converters. In this comparative study, the proposed converter is compared with the conventional BBB converter, the converter, the bidirectional version of the KY-based converter in [190], the CBB-IIM converter,

the CBB-CIM converter, and the bidirectional version of the quadratic buck-boost converter in [191]. The circuit diagrams of these converters are shown in Figure 7.5. Table 7.1 shows the static voltage gain for *A*-to-*B* and *B*-to-*A* operations, the normalized voltage stress of the power switches, and the number of components of the proposed converter and the other BBB converters in this comparative study.

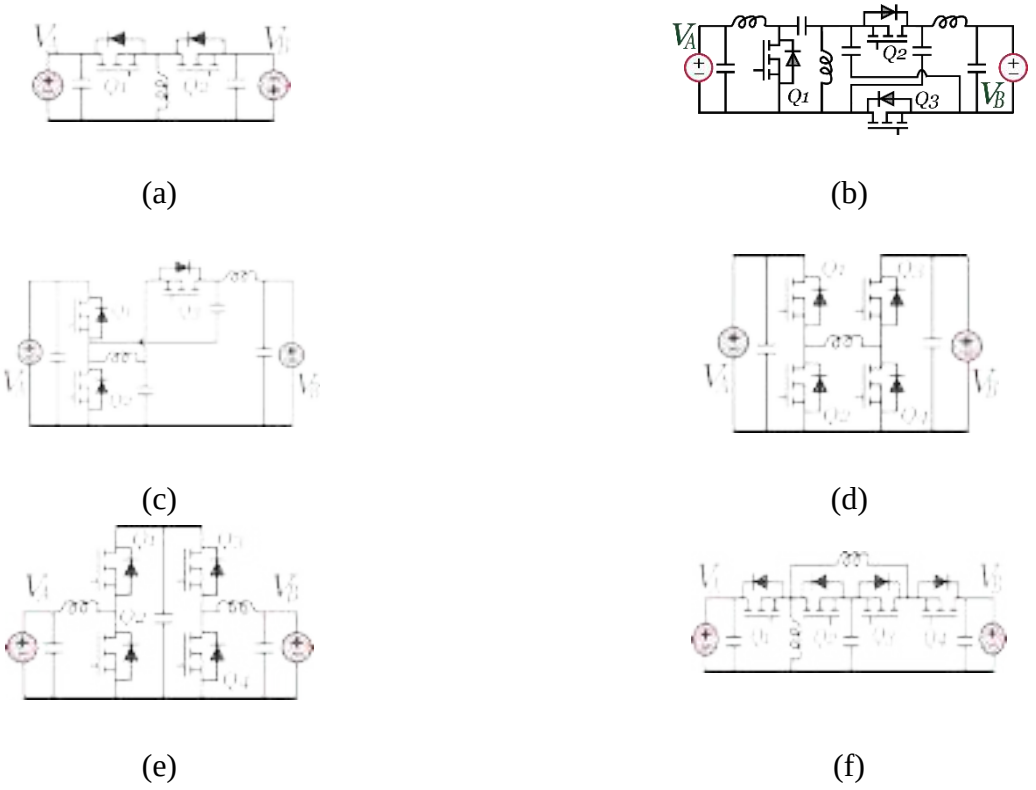
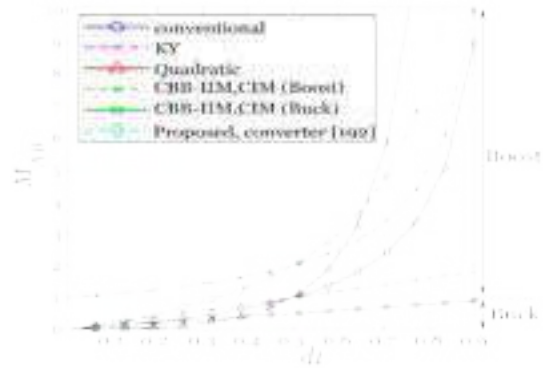
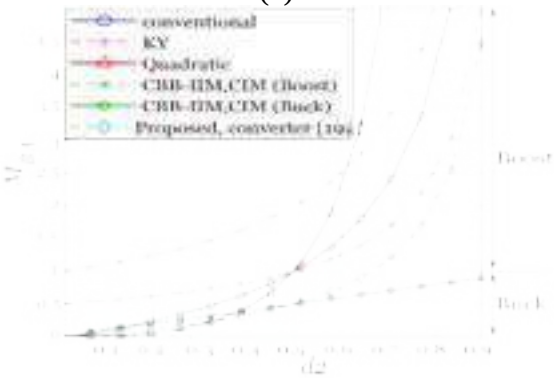


Figure 7.5: Other BBB converters. (a) Conventional BBB converter. (b) Converter in [192]. (c) Bidirectional version of the KY-based converter in [190]. (d) CBB-IIM. (e) CBB-CIM. (f) Bidirectional version of the quadratic converter in [191].

Figure 7.6(a) and Figure 7.6(b) show the voltage gain of the compared converters versus the duty cycle for *A*-to-*B* and *B*-to-*A* operations, respectively. In this comparison, the normalized voltage stress on the power switches is depicted as a function of V_B and M_{AB}.



(a)



(b)

Figure 7.6: Comparison of voltage gain between the proposed converter and other BBB converters. (a) A-to-B operation. (b) B-to-A operation.

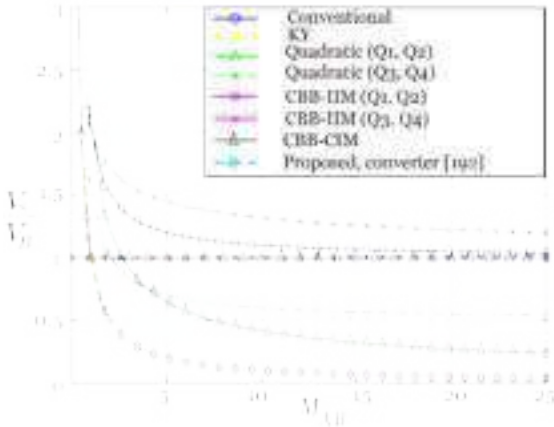


Figure 7.7: Normalized voltage stress on the switches of the compared converters.

The graphical representation of the normalized voltage stress on the power switches of the compared converters is shown in Figure 7.7.

Comparing the proposed converter with the conventional BBB converter, on one hand, the

conventional BBB converter has lower number of switches and passive components, on the other hand, the voltage gain of the proposed converter is higher in *A*-to-*B* operation and lower in *B*-to-*A* operation. This makes the proposed converter better for the applications that require buck and boost operations in both power flow directions, but with boost operation dominant in one power flow direction and buck operation dominant in the other power flow direction (i.e. energy storage systems with large voltage swings). Additionally, the voltage stress in the proposed converter is lower, which enables the utilization of power switches with lower rated voltage. The converter presented in [192] has the same voltage gain in the *A*-to-*B* and *B*-to-*A* operations, and the same voltage stress as in the proposed converter. Nevertheless, the proposed converter has one less inductor and one less capacitor.

Table 7.1: COMPARISON BETWEEN THE PROPOSED AND OTHER BBB CONVERTERS

Topology	Components	Voltage stress (V_S)		Voltage gain	
				A-to-*B* operation	*B*-to-*A* operation
Conventional BBB converter	2 Switches 1 Inductor 2 Capacitors	$Q_{1,2}$	$\left(\frac{M_{AB}+1}{M_{AB}}\right)V_B$	$M_{AB}=\frac{d_1}{1-d_1}$	$M_{BA}=\frac{d_2}{1-d_2}$
KY-based Converter [190]	3 Switches 2 Inductors 4 Capacitors	$Q_{1,2,3}$	$\frac{V_B}{M_{AB}}$	$M_{AB}=2d_1$	$M_{BA}=\frac{1}{2(1-d_2)}$
Quadratic Converter [191]	4 Switches 2 Inductors 3 Capacitors	$Q_{1,2}$	$\left(\frac{1+\sqrt{M_{AB}}}{M_{AB}}\right)V_B$	$M_{AB}=\frac{d_1^2}{(1-d_1)^2}$	$M_{BA}=\frac{d_2^2}{(1-d_2)^2}$
		$Q_{3,4}$	$\left(\frac{1+\sqrt{M_{AB}}}{\sqrt{M_{AB}}}\right)V_B$		
CBB-IIM converter	4 Switches 1 Inductor 2 Capacitors	$Q_{1,2}$	$\frac{V_B}{M_{AB}}$	$M_{AB}=\begin{cases}d_1 & \text{(Buck)}\\ \frac{1}{1-d_1} & \text{(Boost)}\end{cases}$	$M_{BA}=\begin{cases}d_2 & \text{(Buck)}\\ \frac{1}{1-d_2} & \text{(Boost)}\end{cases}$
		$Q_{3,4}$	V_B		
CBB-CIM converter	4 Switches 2 Inductor 3 Capacitors	$Q_{1,2,3,4}$	$\begin{cases}\frac{V_B}{M_{AB}} & M_{AB}\le 1\\ V_B & M_{AB}>1\end{cases}$	$M_{AB}=\begin{cases}d_1 & \text{(Buck)}\\ \frac{1}{1-d_1} & \text{(Boost)}\end{cases}$	$M_{BA}=\begin{cases}d_2 & \text{Buck)}\\ \frac{1}{1-d_2} & \text{(Boost)}\end{cases}$
Converter [192]	3 Switches 3 Inductors 5 Capacitors	$Q_{1,2,3}$	$\left(\frac{M_{AB}+2}{2M_{AB}}\right)V_B$	$M_{AB}=\frac{2d_1}{1-d_1}$	$M_{BA}=\frac{d_2}{2(1-d_2)}$
Proposed	3 Switches 2 Inductors 4 Capacitors	$Q_{1,2,3}$	$\left(\frac{M_{AB}+2}{2M_{AB}}\right)V_B$	$M_{AB}=\frac{2d_1}{1-d_1}$	$M_{BA}=\frac{d_2}{2(1-d_2)}$

The KY-based BBB converter has the least voltage stress on its power switches, however, its voltage gain range is limited, and hence, it is not suitable for applications that require wide voltage gain range operation. Comparing the proposed converter with the bidirectional version of the quadratic buck-boost converter in [191], the proposed converter has higher voltage gain in *A*-to-*B* operation for $d_1 < 0.66$, and lower voltage gain in *B*-to-*A* operation for $0.33 < d_2 < 0.66$. In the quadratic BBB converter, the voltage stress on two of its switches (Q_3 and Q_4) is higher compared to the voltage stress on any switch of the proposed converter.

Additionally, the proposed converter has one less power switch and continuous current at port *B*, on the contrary with the quadratic BBB converter which has discontinuous currents at both of its ports. The CBB-IIM converter, on one hand, has one less inductor and two less capacitors, but on the other hand, it has an extra power switch compared to the proposed converter. The currents at port *A* and port *B* of the CBB-IIM converter are discontinuous. Additionally, the voltage stress on two of switches (Q_3 and Q_4) of the CBB-IIM converter is higher compared to the voltage stress on any switch of the proposed converter. The CBB-CIM converter has one less capacitor and an extra power switch compared to the proposed converter. This converter has continuous currents at port *A* and port *B*. The voltage stress on the power switches of the CBB-CIM converter is higher compared to the proposed converter. The proposed converter has higher voltage gain in *A*-to-*B* operation for $d_1 > 0.5$ compared to the CBB-IIM and CBB-CIM converters (in boost mode), and lower voltage gain in *B*-to-*A* operation for $d_2 < 0.5$ compared to the CBB-IIM and CBB-CIM converters (in buck mode).

7.2.6 Efficiency Analysis

The power losses of the proposed converter are calculated by (16), where P_{loss}, $P_{Q\_cond,}$ P_{Q_sw}, P_L, and P_C are the total power loss, the conduction loss of the transistors, the switching loss of the transistors, the loss of inductors, and the loss of the capacitors. The switching loss of the transistors is for Q_1 (in *A*-to-*B* operation), and for Q_2 and Q_3 (in *B*-to-*A* operation).

$$P_{loss} = P_{Q\_cond,} + P_{Q\_sw} + P_L + P_C \tag{16}$$

The terms of (16) are calculated by (17)-(21), where R_{DS1}, R_{DS2}, R_{DS3}, R_{L1}, R_{L2}, ESR_1, ESR_2, ESR_3, and ESR_4 are the on resistances of Q_1, Q_2, and Q_3, the series resistances of L_1, and L_2, and the equivalent series resistances of C_1, C_2, C_3, and C_4, respectively.

The switching loss of any of the three transistors can be calculated by (19), where *i* can be 1, 2, or 3, referring to Q_1, Q_2, or Q_3, respectively. In (19), t_{ri}, t_{fi}, and C_{OSSi} are the rise time, fall time, and the parasitic output capacitance of Q_i, respectively.

$$P_{Q\_cond} = d_1 {I_{Q1}}^2 R_{DS1} + d_2({I_{Q2}}^2 R_{DS2} + {I_{Q3}}^2 R_{DS3}) \tag{17}$$

$$P_{Q\_sw} = \begin{cases} P_{Q1_{sw}} & (A\text{-to-}B \text{ operation}) \\ P_{Q2\_sw} + P_{Q3\_sw} & (B\text{-to-}A \text{ operation}) \end{cases} \tag{18}$$

$$P_{Qi\_sw} = f_s(0.5 V_{Qi} I_{Qi}(t_{ri} + t_{fi}) + 0.5 {V_{Qi}}^2 C_{OSSi}) \tag{19}$$

$$P_L = {I_{L1}}^2 R_{L1} + {I_{L2}}^2 R_{L2} \tag{20}$$

$$P_C = {I_{C1}}^2 \mathrm{ESR}_1 + {I_{C2}}^2 \mathrm{ESR}_2 + {I_{C3}}^2 \mathrm{ESR}_3 + {I_{C4}}^2 \mathrm{ESR}_4 \tag{21}$$

The inductor currents can be calculated by (7), and (10). The current and voltage stresses on the transistors can be calculated by (11)-(13). The root-mean-square (rms) values of the capacitor currents I_{C1}, I_{C2}, I_{C3}, and I_{C4}, can be calculated by (22).

$$I_{C1} = I_{C3} = \sqrt{d_1 {I_{L2}}^2 + (1-d_1)\left(\frac{I_{L1}-I_{L2}}{2}\right)^2}$$

$$I_{C2} = \sqrt{d_1(I_{L1} - M_{AB}I_{L2})^2 + (1-d_1)(I_{L1} - (1+M_{AB})I_{L2})^2} \qquad (22)$$

$$\left(I_{C4} = \frac{\Delta i_{L2}}{2\sqrt{3}} \right.$$

The efficiency η can be calculated by (23)

$$\eta = \begin{cases} \dfrac{V_A I_{L2} M_{AB} - P_{Loss}}{V_A I_{L2} M_{AB}} & (A\text{-to-}B \text{ operation}) \\ \left(\dfrac{V_B I_{L2} - P_{Loss}}{V_B I_{L2}} \right. & (B\text{-to-}A \text{ operation}) \end{cases} \qquad (23)$$

7.3 Dynamic Modeling and Controller Design

7.3.1 Small-Signal Modeling

The small-signal modeling is used to derive the open-loop transfer functions that can be used in designing the controller, and analyzing the dynamic behavior of the proposed converter. For both *A*-to-*B* and *B*-to-*A* operations, the small-signal modeling is done using (1)-(4), by replacing each state variable and input by its dc quiescent value plus a small ac perturbation.

In *A*-to-*B* operation, the small-signal model is presented in (24), where I_{L1}, I_{L2}, V_{C1}, and d_1 are the dc values of the inductor currents, the voltage across C_1, and the duty cycle of Q_1, and $\hat{\imath}_{L1}$, $\hat{\imath}_{L2}$, $\hat{v}_{c1}$, $\hat{v}_{C3}$, $\hat{d}_1$,and $\hat{v}_B$ are small perturbations in inductor currents, capacitor voltages, duty cycle, and port *B* voltage.

$$L_1 \frac{d\hat{\imath}_{L1}}{dt} = -d_1 \hat{v}_{C1} + V_{C1} \hat{d}_1$$

$$L_2 \frac{d\hat{\imath}_{L2}}{dt} = V_{C1} \hat{d}_1 + \left(d_1 + \frac{C_1}{C_3}\right) \hat{v}_{C1} - \hat{v}_B$$

$$2C_1 \frac{d\hat{v}_{C1}}{dt} = d_1 \hat{\imath}_{L1} - (I_{L1} + I_{L2}) \hat{d}_1 - (1 + d_1) \hat{\imath}_{L2} \quad (24)$$

$$C_4 \frac{d\hat{v}_B}{dt} = \hat{\imath}_{L2} - \frac{\hat{v}_B}{R_1}$$

$$\left\{ \hat{v}_{C3} = \frac{C_1}{C_3} \hat{v}_{C1} \right.$$

By using Laplace transform on (24), the control-to-output transfer function can be given, as shown in (25).

$$G_{V_B d_1}(\mathrm{s}) = \frac{\hat{v}_B(s)}{\hat{d}_1(s)} = \frac{a_0 s^2 + a_1 s + a_2}{b_0 s^4 + b_1 s^3 + b_2 s^2 + b_3 s + b_4} \quad (25)$$

Where

$$
\begin{aligned}
a_0 &= 2C_1V_{C1}L_1L_2 \\
a_1 &= -L_1L_2(I_{L1}+I_{L2})\left(d_1+\frac{C_1}{C_3}\right) \\
a_2 &= (L_1(1+d_1)+L_2d_1-(1+d_1)L_1)V_{C1}\left(d_1+\frac{C_1}{C_3}\right) \\
&\quad +L_2{d_1}^2V_{C1} \\
b_0 &= 2C_1C_4L_1{L_2}^2 \\
b_1 &= \frac{2C_1L_1{L_2}^2}{R_1} \\
b_2 &= (1+d_1)\left(d_1+\frac{C_1}{C_3}\right)C_4L_1L_2+{d_1}^2{L_2}^2C_4 \\
&\quad +2C_1L_1L_2 \\
b_3 &= \frac{1}{R_1}\left(L_1L_2(1+d_1)\left(d_1+\frac{C_1}{C_3}\right)+{d_1}^2{L_2}^2\right) \\
b_4 &= L_1(1+d_1)\left(\left(d_1+\frac{C_1}{C_3}\right)-1\right)+L_2{d_1}^2
\end{aligned}
$$

In *B*-to-*A* operation, the small-signal model is presented in (26), where d_2 (= d_3) is the duty cycle of Q_2, and Q_3. Also,$\hat{d}_2$ and $\hat{v}_A$ are small perturbations in duty cycle, and port *A* voltage, respectively. By using Laplace transform on (26), the control-to-output transfer function can be given, as shown in (27).

$$
\begin{aligned}
L_1\frac{d\hat{\imath}_{L1}}{dt} &= \hat{v}_A - V_{C1}\hat{d}_2 - d_2\hat{v}_{C1} \\
L_2\frac{d\hat{\imath}_{L2}}{dt} &= -V_{C1}\hat{d}_2+\left(\frac{C_1}{C_3}+(1-d_2)\right)\hat{v}_{C1} \\
2C_1\frac{d\hat{v}_{C1}}{dt} &= (2-d_2)\hat{\imath}_{L2}-(I_{L1}+I_{L2})\hat{d}_2-d_2\hat{\imath}_{L1} \\
C_2\frac{d\hat{v}_A}{dt} &= \left(1-\frac{d_2}{2}\right)\hat{\imath}_{L1}-\frac{d_2}{2}\hat{\imath}_{L2}-(I_{L1}+I_{L2})\hat{d}_2-\frac{\hat{V}_A}{R_1} \\
\hat{v}_{C3} &= \frac{C_1}{C_3}\hat{v}_{C1}
\end{aligned}
\qquad (26)
$$

$$
G_{V_Ad_2}(\mathrm{s}) = \frac{\hat{v}_A(s)}{\hat{d}_2(s)} = \frac{e_0s^3+e_1s^2+e_2s+e_3}{f_0s^4+f_1s^3+f_2s^2+f_3s+f_4} \qquad (27)
$$

Where

$$
\begin{aligned}
e_0 &= -2C_1{L_1}^2{L_2}^2 I_{L2} \\
e_1 &= 2C_1L_1L_2V_{C1}(-L_2 + d_1L_1) \\
e_2 &= \left(L_2{d_2}^2 + L_1(2-d_2)(1-d_2)\right)(L_1L_2I_{L2}) + \\
&\quad \left(L_2d_2 + L_1d_2\left(1 - d_2 + \frac{C_1}{C_3}\right)\right)(I_{L1} + I_{L2})L_1L_2 \\
e_3 &= \left(L_1{d_2}^2 + L_1(2-d_2)(1-d_2)\right)(L_2 - d_1L_1)V_{C1} \\
&\quad + \left(L_2d_2 + L_1d_2\left(1 - d_2 + \frac{C_1}{C_3}\right)\right)\begin{pmatrix}(2-d_2)L_1V_{C1} \\ -d_2V_{C1}L_2\end{pmatrix} \\
f_0 &= -2C_1C_2{L_2}^2{L_1}^2 \\
f_1 &= \frac{2}{R_2}C_1{L_1}^2{L_2}^2 \\
f_2 &= -2C_1L_1{L_2}^2 + \begin{pmatrix}L_2{d_2}^2 + \\ L_1(2-d_2)(1-d_2)\end{pmatrix}(L_1L_2C_2) \\
f_3 &= -\left(L_2{d_2}^2 + L_1(2-d_2)(1-d_2)\right)\left(\frac{L_1L_2}{R_2}\right) \\
f_4 &= {L_2}^2{d_2}^2 + L_1L_2(2-d_2)(1-d_2) \\
&\quad -d_2L_2\left(L_2d_2 + L_1d_2\left(1 - d_2 + \frac{C_1}{C_3}\right)\right)
\end{aligned}
$$

7.3.2 Controller Design

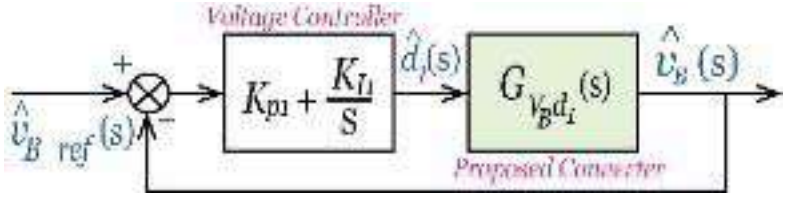
In the developed experiment, two proportional integral (PI) controllers are adopted to regulate the voltage of port *A* and port *B*, in the *B*-to-*A* and *A*-to-*B* operations, respectively. The parameters of the closed-loop PI voltage controller in the *A*-to-*B* operation are: K_{P1} = 0.000025, and K_{I1} = 0.00025. The parameters of the closed-loop PI voltage controller in the *B*-to-*A* operation are: K_{P2} = 0.001, and K_{I2} = .0001. The structure of the closed-loop voltage controllers in the *B*-to-*A* and *A*-to-*B* operations is shown in Figure 7.8. By means of (25), (27), and the parameters of the experiment in Table 7.2, compensated transfer functions ($G_{C\_AB}(\mathrm{s})$ and $G_{C\_BA}(\mathrm{s})$) of the proposed converter in *A*-to-*B* and *B*-to-*A* operations are given in (28) and (29), respectively.

$$G_{C\_AB}(\mathrm{s}) = \left(K_{P1} + \frac{K_{I1}}{s}\right).\ G_{V_B d_1}(\mathrm{s}) \ = \ \frac{x_0 s^3 + x_1 s^2 + x_2 s + x_3}{x_4 s^5 + x_5 s^4 + x_6 s^3 + x_7 s^2 + x_8 s} \qquad (28)$$

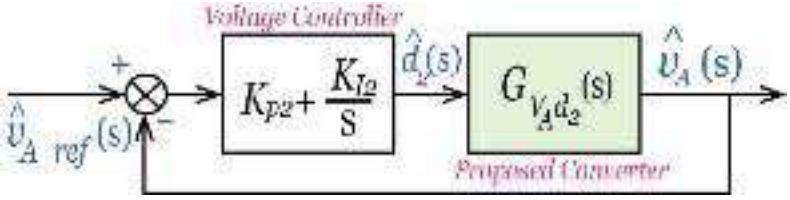
$$G_{C\_BA}(\mathrm{s}) = \left(K_{P2} + \frac{K_{I2}}{s}\right).\ G_{V_A d_2}(\mathrm{s}) \ = \ \frac{y_0 S^4 + y_1 s^3 + y_2 s^2 + y_3 s + y_4}{y_5 s^5 + y_6 s^4 + y_7 s^3 + y_8 s^2 + y_9 s} \qquad (29)$$

Where x_0 = 3.18e6, x_1 = - 3.16e9, x_2 = 1.12e13, x_3 = 1.1e12, x_4 = 27, x_5 = 1125, x_6 = 2e9, x_7 = 6.89e10, x_8 = 3.83e14, y_0 = -6.8, y_1 = -7.97e5, y_2 = -7.1e9, y_3 = 5.53e13, y_4 = 6.5e14, y_5 = 1, y_6 = 1.4e5, y_7 = 2.8e9, y_8 = 1.4e11, y_9 = 6.23e14.

Hence, the Bode plots of the compensated transfer functions of the converter with PI voltage controllers in *A*-to-*B* and *B*-to-*A* operations are given in Figure 7.9(a) and Figure 7.9(b), respectively. These Bode diagrams show that the compensated transfer functions of the proposed converter in both operations have positive gain and phase margins, which indicate a stable operation of the proposed converter with the adopted PI voltage controllers.

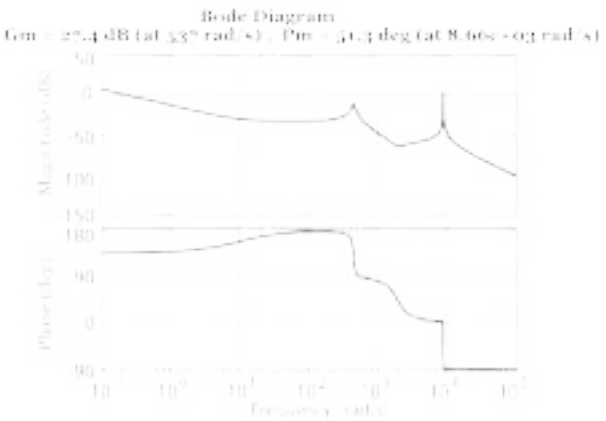


(a)

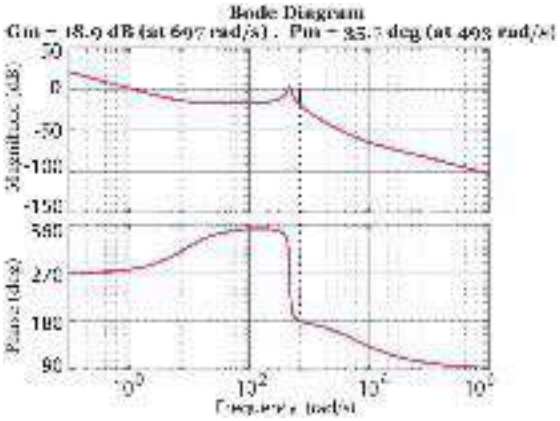


(b)

Figure 7.8: Closed-loop voltage controller. (a) A-to-B operation. (b) B-to-A operation.



(a)



(b)

Figure 7.9: Bode plots of the compensated transfer functions with PI controllers. (a) A-to-B operation. (b) B-to¬-A operation.

7.4 Experimental Results and Analysis

In order to validate the effectiveness of the proposed converter, a scaled-down prototype is developed, as shown in Figure 7.10. The parameters of the experimental setup are given in Table 7.2.

The laboratory setup is built using SiC MOSFETs, to have better efficiency at high frequency operation. In this section, two case studies are investigated, namely: case study I, and case study II. Case study I investigates the *A*-to-*B* operation, while case study II investigates the *B*-to-*A* operation.

Table 7.2: Experiment Parameters

Parameters and Components	Values
Rated power P_o	1.6 kW
Power MOSFET Q_1	C2M0025120D
Power MOSFETs Q_2, Q_3	SCT3030KL
Inductors L_1, L_2	300 µH
Capacitors C_2, C_4	2X120 µF
Capacitors C_1, C_3	2X20, 3X20 µF
Switching frequency f_s	100 KHz
Microcontroller	TMS32028f377s

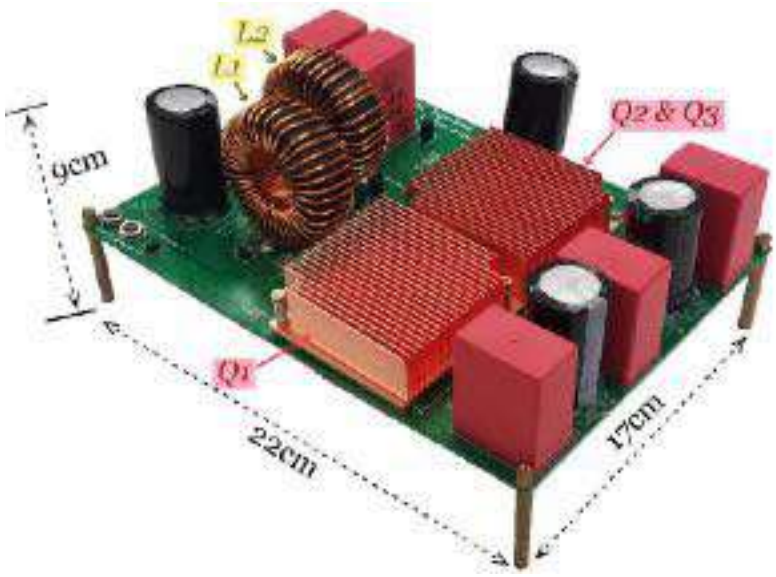


Figure 7.10: Experimental prototype.

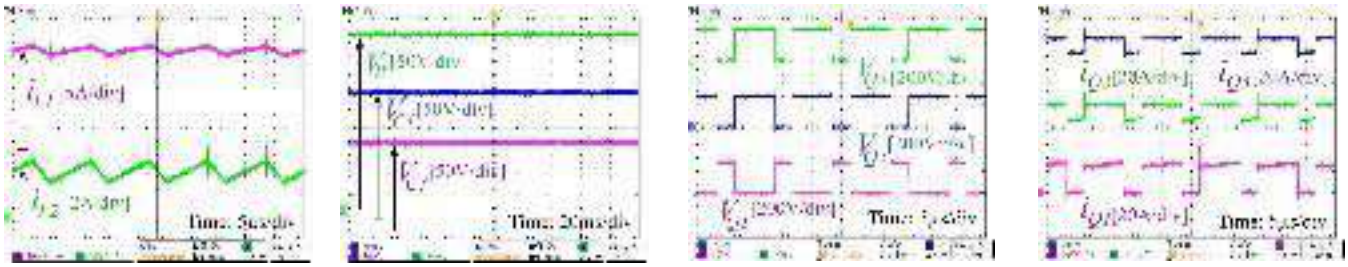
7.4.1 Experimental Results in Case Study I

This case study investigates the *A*-to-*B* operation of the proposed converter. In this case, port *A* is connected to a voltage source V_A=85V, port *B* is connected to a resistive load R_1=100Ω, and the duty cycle d_1=0.7.

The experimental results for case study I are shown in Figure 7.11. According to (7), and (15), the average current values of L_1, and L_2 and their ripple currents can be calculated as following:

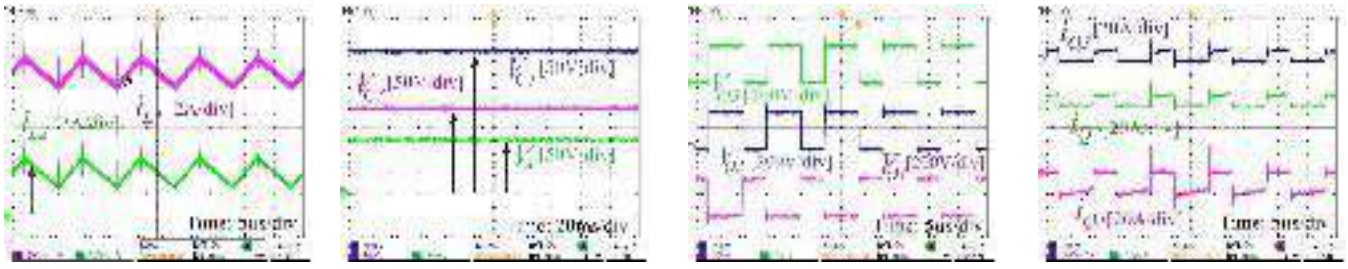
I_{L1}=22.48A, I_{L2}=3.97A, Δi_{L1}=Δi_{L2}=1.98A (both L_1 and L_2 have the same inductance in the experiment), which closely agree with the experimental results in Figure 7.11(a). According to (5) and (6), the average capacitor voltages can be calculated as following: V_{C1}=283.3V, V_{C3}=198.3V, and V_B=396V, which closely agree with the experimental results in Figure 7.11(b). According to (11), the voltage stress on the transistors can be calculated as following: V_{Q1}= V_{Q2}= V_{Q3}=283.3V, which closely agree with the experimental results in Figure 7.11(c). According to (12), and (13), the current stress on the transistors can be calculated as following: I_{Q1}=26.4A, I_{Q2}= I_{Q3}=13.2A, which closely agree with the experimental results in Figure 7.11(d).

The voltage waveforms of the synchronous rectifiers of the proposed converter in this case (*A*-to-*B* operation) are shown in Figure 7.13(a). It is clear, that both Q_2, and Q_3 realize ZVS during turn-on and turn-off transitions.



(a) (b) (c) (d)

Figure 7.11: Experimental results for case study I.



(a) (b) (c) (d)

Figure 7.12: Figure 7.11: Experimental results for case study II.

(a) (b)

Figure 7.13: Gate signals and the voltage stress across the synchronous rectification transistors. (a) Case study I. (b) Case study II.

(a) (b)

Figure 7.14: Dynamic behavior of the proposed converter due to step-change in load. (a) In A-to-B operation. (b) In B-to-A operation.

Figure 7.14(a) shows good dynamic behavior of V_B which is kept at 400V using the closed-loop voltage controller while the output power has step-changed from 800W to 1.6 kW, then from 1.6 kW to 800W.

7.4.2 Experimental Results in Case Study II

This case study investigates the *B*-to-*A* operation of the proposed converter. In this case, port *B* is connected to a voltage source V_B=400V, port *A* is connected to a resistive load R_2=12Ω, and the duty cycle d_2=0.4.

The experimental results for case study II are shown in Figure 7.12. According to (10), and (15), the average current values of L_1, and L_2 and their ripple currents can be calculated as following: I_{L1}=14.8A, I_{L2}=3.7A, $\Delta i_{L1}=\Delta i_{L2}$=2.7A, which closely agree with the experimental results in Figure 7.12(a). According to (8) and (9), the average capacitor voltages can be calculated as following: V_{C1}=333.3V, V_{C3}=200V, and V_A=133.3V, which closely agree with the experimental

results in Figure 7.12(b). According to (11), the voltage stress on the transistors can be calculated as following: V_{Q1}= V_{Q2}= V_{Q3}=333.3V, which closely agree with the experimental results in Figure 7.12(c). According to (12), and (13), the current stress on the transistors can be calculated as following: I_{Q1}=18.5A, I_{Q2}= I_{Q3}=9.3A, which closely agree with the experimental results in Figure 7.12(d).

The voltage waveforms of the synchronous rectifiers of the proposed converter in this case (*B*-to-*A* operation) are shown in Figure 7.13(b). It is clear, that Q_1 realizes ZVS during turn-on and turn-off transitions.

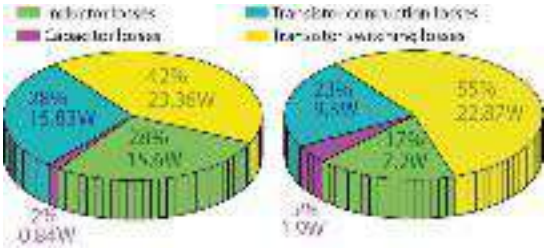
Figure 7.14(b) shows acceptable dynamic behavior of V_A which is kept at 133V using the closed-loop voltage controller while the output power has step-changed from 1.47 kW to 737W, then from 737W to 1.47 kW.

7.4.3 Efficiency Analysis of the Proposed Converter

The calculated loss distributions for the experiment in case study I and case study II are shown in Figure 7.15. In case study I, the total losses of the converter are 55.63W, and the loss distribution is shown in Figure 7.15(a). The switching loss in this case is caused by only Q_1 (Q_2 and Q_3 are soft-switched), and it accounts for 42% of the total losses. The conduction loss of Q_1, Q_2 and Q_3 account for 28% of the total losses. The losses of the capacitors and inductors in case I account for 2%, and 28% of the total losses, respectively. In case study II, the total losses of the converter are 41.27W, and the loss distribution is shown in Figure 7.15(b). The switching loss in this case is caused by only Q_2 and Q_3 (Q_1 is soft-switched), and it accounts for 55% of the total losses. The conduction loss of Q_1, Q_2 and Q_3 account for 23% of the total losses. The losses of the capacitors and inductors case II account for 5%, and 23% of the total losses, respectively. The measured efficiency curves for both *A*-to-*B* and *B*-to-*A* operations with output power equals 1kW and 1.5kW

are presented in Figure 7.16. The measured efficiency curves were obtained using a Power Analyzer (Tektronix PA3000).

In the *A*-to-*B* operation, the voltage at port *B* is kept constant at 400V, the output power (from port *B*) equals 1kW and 1.5kW, and the voltage at port *A*, V_A changes from 50V to 500V, the efficiency of the converter is tracked for each value of V_A. The converter operates in boost mode when V_A is less than 400V, and in buck mode otherwise. In the *B*-to-*A* operation, the voltage at port *B* is kept constant at 400V, the output power (from port *A*) equals 1kW and 1.5kW, and the voltage at port *A* changes from 50V to 500V, the efficiency of In the *A*-to-*B* operation, the voltage at port *B* is kept constant at 400V, the output power (from port *B*) equals 1kW and 1.5kW, and the voltage at port *A*, V_A changes from 50V to 500V, the efficiency of the converter is tracked for each value of V_A. The converter operates in boost mode when V_A is less than 400V, and in buck mode otherwise. In the *B*-to-*A* operation, the voltage at port *B* is kept constant at 400V, the output power (from port *A*) equals 1kW and 1.5kW, and the voltage at port *A* changes from 50V to 500V, the efficiency of V_A=300V) in *A*-to-*B* operation, and from 91% (at V_A=50) to 97.3% (at V_A=300V) in *B*-to-*A* operation.



(a) (b)

Figure 7.15: Calculated power loss distributions for the experiment. (a) In case study I. (b) In case study II.

It is noticed that the efficiency increases gradually as V_A increases for the same output power, this is due to the reduction in losses caused by the decreased input current. For high values of V_A, the switching losses become dominant, and the total efficiency drops, as shown in Figure 7.16.

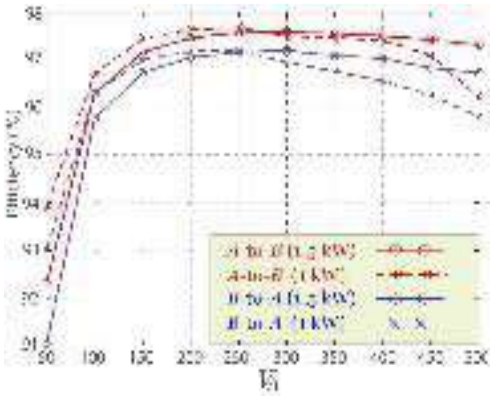


Figure 7.16: Measured efficiency curves of the proposed converter in A-to-B and B¬-to-A operations (VB=400V, VA=50→500V).

7.4.4 Bidirectional Transition Performance

In order to evaluate the bidirectional transient performance of the proposed converter, the circuit shown in Figure 7.17 was constructed. Two power supplies (i.e. *PS1*=100V and *PS2*=400V) are connected to port *A* and port *B* of the prototype. The power supplies are connected via dc solid-state relays (i.e. *SSR1* and *SSR2*) and two series diodes. Two local loads are connected to the two ports (i.e. R_A=15 Ω and R_B=100 Ω). To test the performance of the converter when it switches from *B*-to-*A* operation to *A*-to-*B* operation, the test starts by making *SSR1*: OFF and *SSR2*: ON, in this case the converter is working in B-to-*A* operation. When the states of the two solid-state relays are inverted *SSR1*: ON and *SSR2*: OFF, the converter works in *A*-to-*B* operation and the *A*-to-*B* voltage controller sets V_B at 400V. Figure 7.18(a) shows that the converter successfully holds the voltage at port *B* at 400V after the transition with an acceptable dynamic response. In Figure 7.18(a), V_B before the transition is the voltage of *PS2*, while after the transition, V_B is the processed voltage by the converter.

To test the performance of the converter when it switches from *A*-to-*B* operation to *B*-to-*A* operation, the test starts by making *SSR1*: ON and *SSR2*: OFF, in this case the converter is working in *A*-to-*B* operation. When the states of the two solid-state relays are inverted *SSR1*: OFF and *SSR2*:

ON, the converter works in *B*-to-*A* operation and the *B*-to-*A* voltage controller sets V_A at 100V. Figure 7.18(b) shows that the converter successfully holds the voltage at port *A* at 100V after the transition with an acceptable dynamic response. In Figure 7.18(b), V_A before the transition is the voltage of *PS1*, while after the transition, V_A is the processed voltage by the converter. In both tests, the polarity of i_{L1} and i_{L2} flips after the transitions, referred to the reference inductor currents direction shown in Figure 7.17.

The oscillations in current that are shown in Figure 7.18 when the converter changed its mode of operation is because the converter changed its mode of operation abruptly. In a realistic scenario, the switching between *A*-to-*B* and *B*-to-*A* operations should be done softly where the reference voltage ramps up to the desired level.

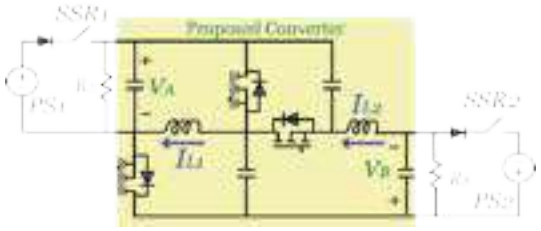


Figure 7.17: Bidirectional power flow transition test circuit.

(a) (b)

Figure 7.18: Dynamic behavior of the proposed converter due to step-change in load. (a) In A-to-B operation. (b) In B-to-A operation.

7.5 Conclusion

In this chapter, a new bidirectional dc-dc converter that can perform buck and boost operations in both power flow directions has been introduced. The proposed converter has a simple circuit

structure, low component counts, low voltage stress on the transistors, and wide voltage gain range. Synchronous rectification has been employed to improve the efficiency of the converter since the synchronous rectifiers turn on and turn off with ZVS. The proposed converter has good steady-state and dynamic performance. These features make it a good candidate for applications that require bidirectional power flow with wide conversion ratios, such as energy storage systems with large voltage swings.

Chapter 8 Analysis and Design of A New Bidirectional DC-DC Converter with Broad Voltage Gain Range for Energy Storage Applications

8.1 Introduction

A new bidirectional dc-dc converter for energy storage systems with large voltage fluctuations is presented in this chapter. The proposed topology has a wide range of voltage regulation, a common ground between its ports, continuous current at the low voltage port, high semiconductor utilization factor, and a low voltage stress on the power switches. The principles of operation, the current and voltage stresses on the power switches, and the design of components are discussed in this chapter. Finally, a 2-kW/800-V scaled-down prototype was developed using Silicon Carbide (SiC) MOSFETs to validate the feasibility of the proposed converter and the correctness of its theoretical analysis.

8.2 Structure and Operating Principles of the Proposed Converter

8.2.1 Circuit Structure of the Proposed Topology

The proposed converter is composed of four switches ($Q_1 \rightarrow Q_4$), three inductors ($L_1 \rightarrow L_3$), and six capacitors ($C_1 \rightarrow C_6$). The proposed topology is shown in Figure 8.1, as it has a low voltage side, where the ESS is connected, and a high voltage side, where the dc bus of the load is connected.

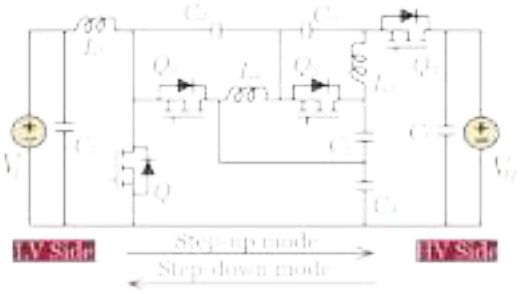
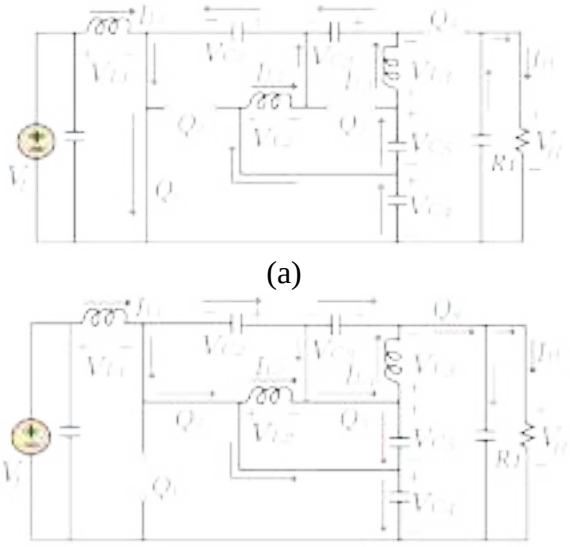


Figure 8.1: The structure of the proposed step-up dc-dc converter.

8.2.2 Operation in Step-Up Mode

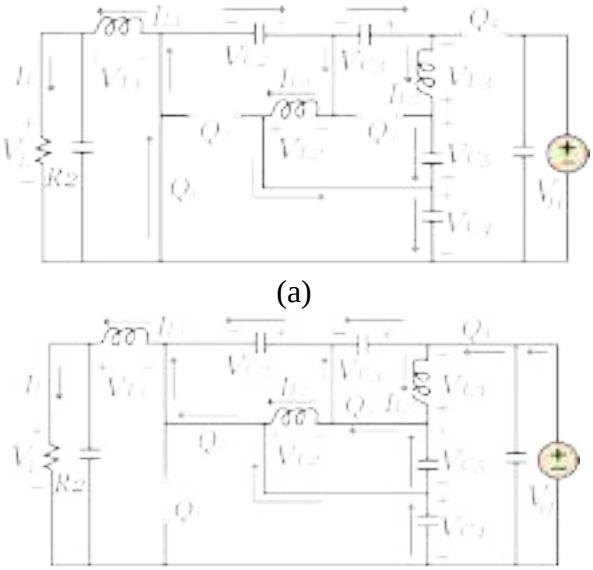
In this mode, the power flow is from the low voltage (LV) side to the high voltage (HV) side. The current flow paths and the key waveforms for this mode are shown in Figure 8.2 and Figure 8.4(a), respectively. In this mode, Q_1 acts as the main switch, while $Q_2 \rightarrow Q_4$ act as synchronous rectifiers. The triggering pulses of $Q_1 \rightarrow Q_4$ are $G_1 \rightarrow G_4$. The duty cycle of Q_1 is d_1 while the duty cycle of $Q_2 \rightarrow Q_4$ is d_2 (= 1-d_1). A delay is applied between the falling edge of $G_2 \rightarrow G_4$ and the rising edge of G_1, and another delay is applied between the falling edge of G_1 and the rising edge of $G_2 \rightarrow G_4$, as shown in Figure 8.4(a). During the delay time, currents flow through the body diodes of the synchronous rectifiers, thus, the drain-to-source voltages of the synchronous rectifiers drop to the forward voltage level of the body diodes, accordingly, ZVS can be realized by $Q_2 \rightarrow Q_4$ during the turn-on and turn-off transitions.



(a)

(b)

Figure 8.2: Current flow paths for step-up mode. (a) State 1. (b) State 0.



(a)

(b)

Figure 8.3: Current flow paths for step-down mode. (a) State 1. (b) State 0.

The proposed converter has two switching states, namely: State1 and State 0. In the following analysis: $i_{C1\_ch} \rightarrow i_{C6\_ch}$, and $i_{C1\_dis} \rightarrow i_{C6\_dis}$ are the charging and discharging currents of $C_1 \rightarrow C_6$. The inductor currents and the instantaneous voltages across the inductors are referred to as $I_{L1} \rightarrow I_{L3}$ and $V_{L1} \rightarrow V_{L3}$, respectively. V_H, V_L, I_H, I_L, and $V_{C2} \rightarrow V_{C5}$ are the voltages of the high

voltage and low voltage sides, the currents of the high voltage and low voltage sides, and the voltages across $C_2 \rightarrow C_5$.

In State 1, Q_1 is turned on, $Q_1 \rightarrow Q_4$ are turned off, C_2 and C_3 charge, and $C_4 \rightarrow C_6$ discharge, as shown in Figure 8.2(a). By applying *Kirchhoff's Voltage Law* (KVL) and *Kirchhoff's Current Law* (KCL) on the equivalent circuit in Figure 8.2(a), we can extract the following relationships:

$$\begin{cases} V_{L1} = V_L \\ V_{L2} = V_{C4} - V_{C2} \\ V_{L3} = V_{C4} + V_{C5} - V_{C3} - V_{C2} \end{cases} \quad (1)$$

$$\begin{cases} i_{C2\_ch} = I_{L2} + I_{L3} \\ i_{C3\_ch} = I_{L3} \\ i_{C4\_dis} = I_{L2} + I_{L3} \\ i_{C5\_dis} = I_{L3} \\ i_{C6\_dis} = I_H \end{cases} \quad (2)$$

In State 0, Q_1 is turned off, $Q_1 \rightarrow Q_4$ are turned on, C_2 and C_3 discharge, and $C_4 \rightarrow C_6$ charge, as shown in Figure 8.2(b). By applying the KVL and KCL rules on the equivalent circuit in Figure 8.2(b), we can extract the following relationships:

$$\begin{cases} V_{L1} = V_L - V_{C4} \\ V_{L2} = -V_{C2} = -V_{C5} \\ V_{L3} = -V_{C3} \end{cases} \quad (3)$$

$$\begin{cases} i_{C2\_dis} = i_{C3\_dis} + I_{L3} + i_{C5\_ch} - I_{L2} \\ i_{C4\_ch} = I_{L1} - i_{C2\_dis} - I_{L2} + i_{C5\_ch} \\ i_{C6\_ch} = i_{C3\_dis} + I_{L3} - I_H \end{cases} \quad (4)$$

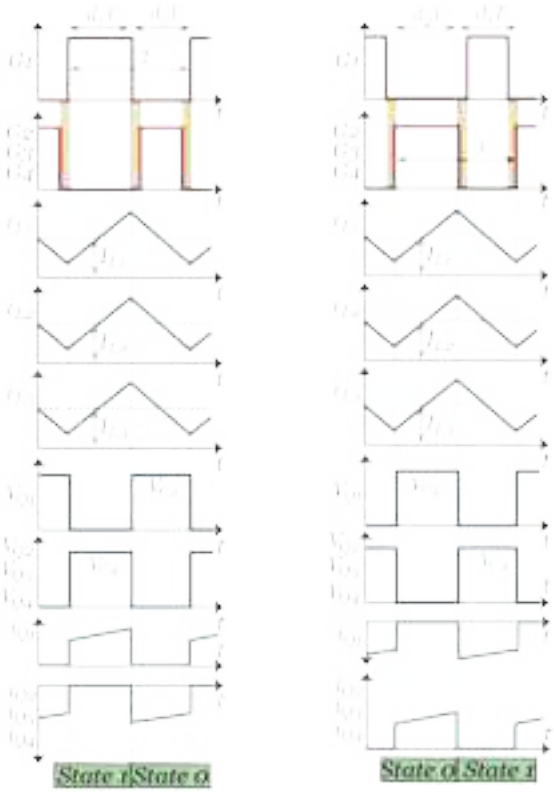
By applying the volt-second rule on (1) and (3), the capacitor voltages can be calculated, as follows:

$$\begin{cases} V_{C2} = V_{C3} = V_{C5} = \dfrac{d_1}{1-d_1} V_L \\ V_{C4} = \dfrac{1}{1-d_1} V_L \end{cases} \tag{5}$$

$$V_H = V_{C3} + V_{C4} + V_{C5} = \frac{1+2d_1}{1-d_1} V_L \tag{6}$$

Accordingly, the voltage gain in step-up mode M_{Boost} can be extracted, as follows:

$$M_{Boost} = \frac{V_H}{V_L} = \frac{1+2d_1}{1-d_1} \tag{7}$$



(a) (b)

Figure 8.4: Key waveforms of the proposed converter. (a) Step-up mode. (b) Step-down mode.

8.2.3 Operation in Step-Down Mode

In this mode, the power flow is from the HV side to the LV side. The current flow paths and the key waveforms for this mode are shown in Figure 8.3 and Figure 8.4(b), respectively. In this mode,

$Q_2 \rightarrow Q_4$ act as the main switches, while Q_1 acts as a synchronous rectifier. The duty cycle of $Q_2 \rightarrow Q_4$ is d_2 while the duty cycle of Q_1 is d_1 (= 1-d_2). A delay is applied between the falling edge of G_1 and the rising edge of $G_2 \rightarrow G_4$, and another delay is applied between the falling edge of $G_2 \rightarrow G_4$ and the rising edge of G_1, as shown in Figure 8.4(b). The delay between the triggering pulses allows Q_1 to realize ZVS during the turn-on and turn-off transitions.

Since Q_1 and $Q_2 \rightarrow Q_4$ work in a complementary fashion, the voltage of the capacitors and the voltage gain in the step-down mode M_{Buck} can be directly derived from (5), (6), and (7), by replacing d_1 by (1-d_2), as follows:

$$\begin{cases} V_{C2} = V_{C3} = V_{C5} = \dfrac{1-d_2}{3-2d_2}\, V_H \\ V_{C4} = \dfrac{1}{3-2d_2}\, V_H \end{cases} \tag{8}$$

$$V_L = \frac{d_2}{3-2d_2}\, V_H \tag{9}$$

$$M_{Buck} = \frac{V_L}{V_H} = \frac{d_2}{3-2d_2} \tag{10}$$

8.2.4 Voltage and Current Stresses on the Switches

By applying KVL rule on the equivalent circuits of the proposed converter, depicted in Figure 8.2 and Figure 8.3, the voltage stress on the switches of the proposed converter V_Q can be expressed as shown in (11):

$$V_Q = \frac{V_L}{1-d_1} = \frac{V_H}{3-2d_2} = \left(\frac{M_{Boost}+2}{3M_{Boost}}\right) V_H \tag{11}$$

Assuming a loss-free operation (i.e. $V_L I_L = V_H I_H$), the currents of the three inductors of the proposed converter can be derived, as follows:

$$I_{L2} = I_{L3} = I_H = M_{Buck}\, I_L = \frac{d_2}{3-2d_2}\, I_L \tag{12}$$

$$I_{L1} = I_L = M_{Boost}\, I_H = \frac{1}{1-d_1}\, I_H \tag{13}$$

By means of the current flow paths shown on the equivalent circuits of the proposed converter in Figure 8.2 and Figure 8.3, the current stresses on the switches can be expressed, as following:

$$i_{Q1} = \frac{3\, I_H}{1-d_1} = \frac{3\, I_L}{3-2d_2} = (M_{Boost} + 2) I_H \tag{14}$$

$$i_{Q2} = i_{Q3} = i_{Q4} = \frac{I_H}{1-d_1} = \frac{I_L}{3-2d_2} = \frac{M_{Boost}+2}{3} I_H \tag{15}$$

Equations (14) and (15) calculate the magnitude of the current stresses on the switches, the polarity of the current depends on whether the switch is operating as a main switch or as a rectifier.

8.3 Components Selection and Efficiency Analysis

8.3.1 Selection of Switches

By means of (11), (14), and (15), the voltage and current stresses on the four switches can be calculated. When the voltage gain range of operation, the voltage of the HV side, and the load profile are known, the peak voltage and current stresses of the four switches of the proposed converter can be calculated. Accordingly, these peak electrical stresses should be within the safe operating area (SOA) of the selected switches.

8.3.2 Design of Inductors

The magnitude of the currents flowing through the three inductors of the proposed converter can be calculated via (12) and (13), hence, the selected inductors should tolerate these current levels. When the operating voltages at the HV and LV sides, the range of voltage gain, the allowed ripple currents ($\Delta i_{L1} \rightarrow \Delta i_{L3}$), and the switching frequency f_s of the proposed converter are known, the proper inductance values can be calculated by means of (16).

$$\begin{cases} L_1 \geq \dfrac{(M_{Boost}-1)V_L}{(M_{Boost}+2)f_s\Delta i_{L1}} = \dfrac{(1-M_{Buck})M_{Buck}V_H}{(1+2M_{Buck})f_s\Delta i_{L1}} \\ L_2 \geq \dfrac{(M_{Boost}-1)V_L}{(M_{Boost}+2)f_s\Delta i_{L2}} = \dfrac{(1-M_{Buck})M_{Buck}V_H}{(1+2M_{Buck})f_s\Delta i_{L2}} \\ L_3 \geq \dfrac{(M_{Boost}-1)V_L}{(M_{Boost}+2)f_s\Delta i_{L3}} = \dfrac{(1-M_{Buck})M_{Buck}V_H}{(1+2M_{Buck})f_s\Delta i_{L3}} \end{cases} \quad (16)$$

8.3.3 Design of Capacitors

The voltage across the six capacitors can be calculated using (5), (6), (8), and (9), thus, the selected capacitors should tolerate these voltage levels. When the load profile at the HV and LV sides, the range of voltage gain, the allowed ripple voltages ($\Delta V_{C1} \rightarrow \Delta V_{C6}$), the allowed ripple current in L_1, and f_s of the proposed converter are known, the proper capacitance values can be derived by means of (17).

$$\begin{cases} C_1 \geq \dfrac{\Delta i_{L1}}{8f_s\Delta V_{C1}} \\ C_2 \geq \dfrac{2(M_{Boost}-1)i_H}{(M_{Boost}+2)f_s\Delta V_{C2}} = \dfrac{2(1-M_{Buck})M_{Buck}i_L}{(1+2M_{Buck})f_s\Delta V_{C2}} \\ C_3 \geq \dfrac{(M_{Boost}-1)i_H}{(M_{Boost}+2)f_s\Delta V_{C3}} = \dfrac{(1-M_{Buck})M_{Buck}i_L}{(1+2M_{Buck})f_s\Delta V_{C3}} \\ C_4 \geq \dfrac{2(M_{Boost}-1)i_H}{(M_{Boost}+2)f_s\Delta V_{C4}} = \dfrac{2(1-M_{Buck})M_{Buck}i_L}{(1+2M_{Buck})f_s\Delta V_{C4}} \\ C_5 \geq \dfrac{(M_{Boost}-1)i_H}{(M_{Boost}+2)f_s\Delta V_{C5}} = \dfrac{(1-M_{Buck})M_{Buck}i_L}{(1+2M_{Buck})f_s\Delta V_{C5}} \\ C_6 \geq \dfrac{(M_{Boost}-1)i_H}{(M_{Boost}+2)f_s\Delta V_{C6}} = \dfrac{(1-M_{Buck})M_{Buck}i_L}{(1+2M_{Buck})f_s\Delta V_{C6}} \end{cases} \quad (17)$$

8.3.4 Efficiency Analysis

Efficiency calculation is essential to properly select and design the cooling system, in addition, it gives an insight about the operating points where the proposed converter has the highest/lowest

efficiency. The total power loss P_{Loss} can be calculated by (18), where P_{L_cond}, P_{L_core}, P_{C_cond}, P_{Q_cond}, and P_{Q_sw} are the conduction and core losses of the three inductors, the conduction losses of the six capacitors, the conduction and switching losses of the switches.

$$P_{loss} = P_{L\_cond} + P_{L\_core} + P_{C\_cond} + P_{Q\_cond} + P_{Q\_sw} \tag{18}$$

The conduction and core losses of the three inductors can be calculated using (19) and (20), where R_{L1}, R_{L2}, R_{L3}, l_{c1}, l_{c2}, l_{c3}, A_{c1}, A_{c2}, A_{c3}, ΔB_1, ΔB_2, and ΔB_3 are the equivalent series resistances of the three inductors, the magnetic flux path lengths of the three inductors' cores, the cross sectional areas of the three inductors' cores, and ac magnetic flux density of the three inductors.

$$P_{L\_cond} = \sum_{i=1}^{i=3} I_{Li}^2 \, R_{Li} \tag{19}$$

$$P_{L\_core} = \sum_{i=1}^{i=3} l_{ci} \, A_{ci} \, (a \, \Delta B_i^b \, f_s^C) \tag{20}$$

Equation (19), is the empirical Steinmetz equation, and *a*, *b*, and *c* are fitting values and can be extracted from the core manufacturer datasheet. The conduction loss of the capacitors can be extracted via (20), where $R_{C1} \rightarrow R_{C6}$ are the equivalent series resistances of the six capacitors.

$$P_C = \frac{\Delta i_{L1}^2}{12} R_{C1} + \frac{d_1}{1 - d_1} I_H^2 (4R_{C2} + R_{C3} + 4R_{C4} + R_{C5} + R_{C6}) \tag{21}$$

The conduction losses of the switches can be derived using (21), where $R_{S1} \rightarrow R_{S4}$ are the on resistances of the switches. The switching loss of the switches can be calculated by (22) and (23), noting that the switching loss is only considered for the main switches for the considered mode of operation and discarded for the synchronous rectifiers (because they realize ZVS during turn-on and turn-off transitions). Equation (23) is used to calculate the switching loss for any of the four

switches, where t_{ri}, t_{fi}, and C_{OSSi} are the rising and falling times, and the parasitic output capacitance of switch Q_i.

$$P_{Q\_cond} = I_H^2 \left(\left(\frac{3\sqrt{d_1}}{1-d_1} \right)^2 R_{S1} + \left(\frac{R_{S2}+R_{S3}+R_{S4}}{1-d_1} \right) \right) \tag{21}$$

$$P_{Q\_sw} = \begin{cases} P_{Q1\_sw} & \text{(Step-up mode)} \\ P_{Q2\_sw} + P_{Q3\_sw} + P_{Q3\_sw} & \text{(Step-down mode)} \end{cases} \tag{22}$$

$$P_{Qi\_sw} = f_s(0.5V_{Qi} i_{Qi}(t_{ri} + t_{fi}) + 0.5{V_{Qi}}^2 C_{OSSi}) \tag{23}$$

Finally, the efficiency η can be calculated using (24):

$$\eta = \begin{cases} \dfrac{V_L\, I_L}{V_L\, I_L + P_{Loss}} & \text{(Step-up mode)} \\ \dfrac{V_H\, I_H}{V_H\, I_H + P_{Loss}} & \text{(Step-down mode)} \end{cases} \tag{24}$$

8.4 Comparative Study

In this section, the proposed topology is compared with five other BDC topologies. These topologies are the B3LC, the switched-capacitor converter (SCC) in [195], the bidirectional version of the quadratic converter in [194], and the converters in [193] and [196]. Table 8.1 gives a summary of the number of passive and active components of the compared topologies. Additionally, it shows the maximum normalized voltage stress on the switches and the voltage gain in the step-up and step-down operations of the compared topologies. The voltage gain relationships with duty cycle of the compared converters are given in Figure 8.5 and Figure 8.6. The maximum normalized voltage stress on the switches of the converters is plotted versus M_{Boost}, as depicted in Figure 8.7.

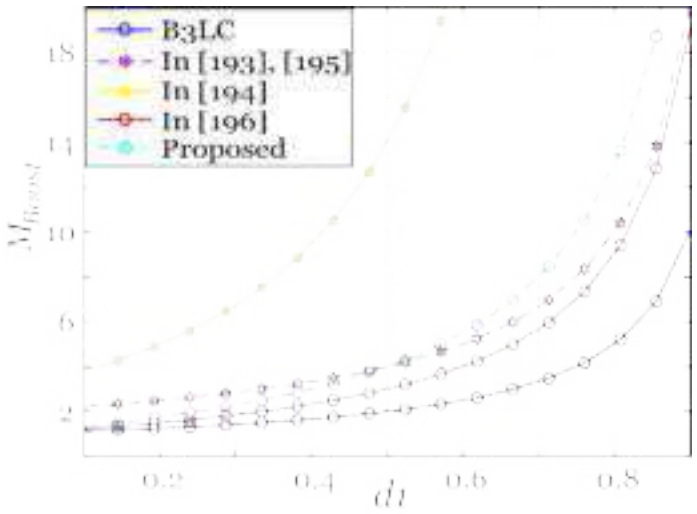


Figure 8.5: Voltage gain of the compared converters in the step-up mode versus the duty cycle.

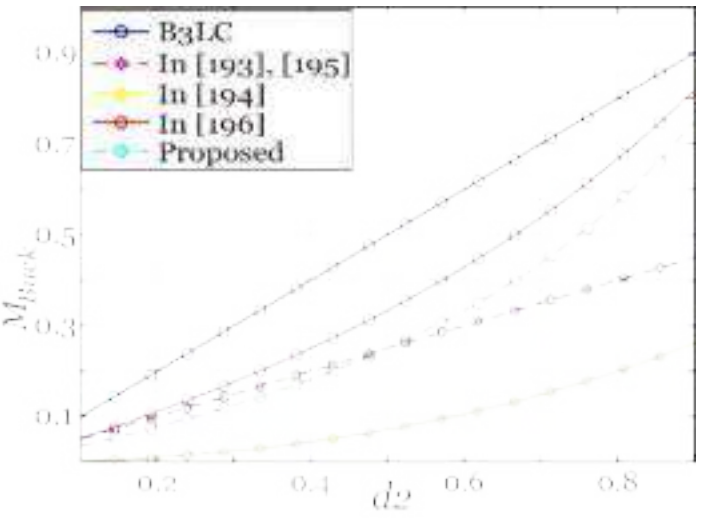


Figure 8.6: Voltage gain of the compared converters in the step-down mode versus the duty cycle.

The B3LC, and the converters in [193] and [196] do not have a common ground between the LV and the HV ports, which may increase the leakage currents and require additional filtering. In the step-up mode, the proposed converter has a higher voltage gain compared to the B3LC, the

converter in [196], the quadratic converter (for $d_1 < 0.5$), the SCC (for $d_1 > 0.5$), and the converter in [193] (for $d_1 > 0.5$), as shown in Figure 8.5.

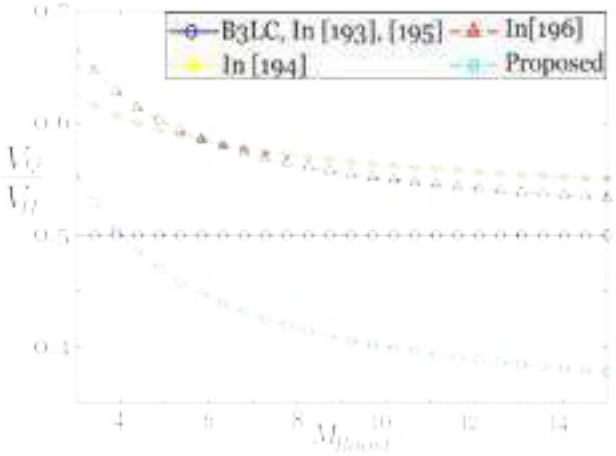


Figure 8.7: Maximum normalized voltage stress on the switches of the compared converters versus the voltage gain.

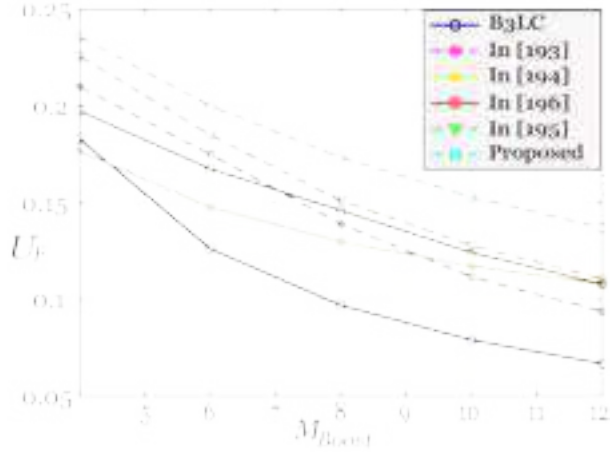


Figure 8.8: Switch utilization factor for the compared converters.

In step-down mode, the proposed converter has a lower voltage gain compared to the B3LC, the converter in [196], the quadratic converter (for $d_2 > 0.5$), the SCC (for $d_2 < 0.5$), and the converter in [193] (for $d_2 < 0.5$), as shown in Figure 8.6. Figure 8.7 shows that the proposed converter has less voltage stress on its power switches in comparison to the quadratic converter, the one in [196], the B3LC (for $M_{Boost} > 4$), the SCC (for $M_{Boost} > 4$), and the converter in [193] (for $M_{Boost} > 4$).

Table 8.1: Comparison Between the Proposed and Other BDC Topologies

Topology	Components	Maximum voltage stress (V_Q)	Common ground	Voltage gain	
				Step-up mode	Step-down mode
B3LC	4 Switches 1 Inductor 2 Capacitors	$\frac{V_H}{2}$	No	$M_{Boost} = \frac{1}{1-d_1}$	$M_{Buck} = d_2$
In [193]	4 Switches 2 Inductors 3 Capacitors	$\frac{V_H}{2}$	No	$M_{Boost} = \frac{2}{1-d_1}$	$M_{Buck} = \frac{d_2}{2}$
Quadratic in [194]	4 Switches 2 Inductor 3 Capacitors	$\left(1+\sqrt{\frac{1}{M_{Boost}}}\right)V_H$	Yes	$M_{Boost} = \left(\frac{1}{1-d_1}\right)^2$	$M_{Buck} = (d_2)^2$
SCC in [195]	5 Switches 2 Inductor 4 Capacitors	$\frac{V_H}{2}$	No	$M_{Boost} = \frac{2}{1-d_1}$	$M_{Buck} = \frac{d_2}{2}$
In [196]	3 Switches 2 Inductors 4 Capacitors	$\left(\frac{M_{Boost}+1}{2M_{Boost}}\right)V_H$	No	$M_{Boost} = \frac{1+d_1}{1-d_1}$	$M_{Buck} = \frac{d_2}{2-d_2}$
Proposed	4 Switches 3 Inductors 6 Capacitors	$\left(\frac{M_{Boost}+2}{3M_{Boost}}\right)V_H$	Yes	$M_{Boost} = \frac{1+2d_1}{1-d_1}$	$M_{Buck} = \frac{d_2}{3-2d_2}$

$$U_F = \frac{P_{out}}{\sum V_{Qi}\, i_{Qi\,(rms)}} \tag{25}$$

In order to assess the comparative cost of the semiconductor devices of the compared converters, the switch utilization factor (U_F) is used, as it is the ratio between the output power of the converter and the total processed power by the switches, as shown in (25).

Where P_{out} is the output power of the converter, V_{Qi} and $i_{Qi(rms)}$ are the voltage stress and the root-mean-square (rms) of the current stress on switch Q_i. Figure 8.8 shows the utilization factor of the compared converters versus M_{Boost} when P_{out} =2kW and V_H = 800V. It is clear that the proposed converter has the highest utilization factor compared to the other five BDC topologies, which indicates that the cost of the semiconductor devices is relatively lower compared to the other converters.

8.5 Experimental Results and Analysis

To validate the feasibility of the proposed BDC topology and the correctness of its theoretical analysis, a scaled-down 2-kW/800-V laboratory prototype was developed, presented in Figure 8.9. The power circuit of the prototype was built using SiC MOSFETs, (UJ3C065030K3S) for Q_1 and (UJ3C065080K3S) for $Q_2 \rightarrow Q_4$, and controlled by a TMS320f28335 microcontroller.

Table 8.2: Main Experimental Parameters of The Proposed Converter

Parameters and Components	Values
Rated power P_{out}	2-kW
HV side voltage V_H	800V
LV side voltage V_L	80V→200V
Switch Q_1	UJ3C065030K3S
Switches $Q_2 \rightarrow Q_4$	UJ3C065080K3S
Inductor L_1	250 µH
Inductors L_2, L_3	330 µH
Capacitors $C_1 \rightarrow C_3$	150 µF
Capacitors C_4, C_5	180 µF
Capacitor C_6	50 µF
Switching frequency f_s	100 KHz
Microcontroller	TMS320f28335

Figure 8.9: Experimental prototype.

Current sense resistors are used to measure the currents of the inductors and the switches. The switching frequency is 100 kHz, and the values of the inductors and capacitors are given in Table 8.2. Two case studies are investigated in this section. In case study I, the converter works in step-up mode, while in case study II, the converter works in step-down mode.

8.5.1 Case Study I

This case study investigates the performance of the proposed converter when it operates in step-up mode. The operating parameters of this case study are as follows: V_L = 100V, d_1 = 0.7, and R_1 = 320Ω, where R_1 is the resistive load connected to the HV side. The experimental results for this case study are shown in Figure 8.10. Based on (5)-(7), the voltage across $C_2 \rightarrow C_6$ and the voltage gain M_{Boost} can be calculated, as follows: $V_{C2} = V_{C3} = V_{C5} \approx 233.3$V, $V_{C4} \approx 333.3$V, V_H = 800V, and M_{Boost} = 8, which closely agree with the experimental results in Figure 8.10(b) and Figure 8.10(c). The currents and ripple currents of the three inductors can be calculated using (12), (13), and (16), as follows: I_{L1} = 20A, $I_{L2} = I_{L3}$ = 2.5A, Δi_{L1}= 2.8A, $\Delta i_{L2} \approx$ 2.12A, $\Delta i_{L3} \approx$ 2.12A, which closely comply with the experimental results in Figure 8.10(a). The voltage stress on the four switches can be derived via (11), as following: $V_{Q1} = V_{Q2} = V_{Q3} = V_{Q4} \approx 333.3$V, which closely agree with the results shown in Figure 8.10(d) and Figure 8.10(e). It is also clear from Figure 8.10(d) and Figure 8.10(e) that the synchronous rectifiers (i.e. $Q2 \rightarrow Q4$) realize ZVS during turn-on and turn-off transitions. The current stresses on the switches can be calculated using (14) and

(15), as: i_{Q1} = 25A, $i_{Q2} = i_{Q3} = i_{Q4} \approx$ 8.3A, which closely comply with the results in Figure 8.10(f).

8.5.2 Case Study II

This case study investigates the performance of the proposed converter when it operates in step-down mode. The operating parameters of this case study are as follows: V_H = 800V, d_2 = 0.5, and R_2 = 20Ω, where R_2 is the resistive load connected to the LV side. The experimental results for this case study are shown in Figure 8.11. The voltage across $C_1 \rightarrow C_5$ can be calculated using (8)-(10), as following: $V_{C2} = V_{C3} = V_{C5}$ = 200V, V_{C4} = 400V, V_L = 200V, and M_{Buck} = 0.25, which is close to the experimental results in Figure 8.11(b) and Figure 8.11(c). By means of (12), (13), and (16), the currents and the ripple currents of the inductors can be calculated using (12), (13), and (16), as follows: I_{L1} = 10A, $I_{L2} = I_{L3}$ = 2.5A, Δi_{L1}= 4A, $\Delta i_{L2} \approx$ 3A, $\Delta i_{L3} \approx$ 3A, which closely complies with the experimental results in Figure 8.11(a). The voltage stress on the switches can be calculated using (11), as follows: $V_{Q1} = V_{Q2} = V_{Q3} = V_{Q4} \approx$ 400V, which closely agree with the results shown in Figure 8.11(d) and Figure 8.11(e). In addition, Figure 8.11(d) shows that the synchronous rectifier (i.e. Q_1) realizes ZVS during turn-on and turn-off transitions. Using (14) and (15), the current stresses on the switches can be derived as: i_{Q1} = 15A, $i_{Q2} = i_{Q3} = i_{Q4} =$ 5A, which closely agree with the results in Figure 8.11(f).

8.5.3 Performance under Wide-Voltage-Gain Operation

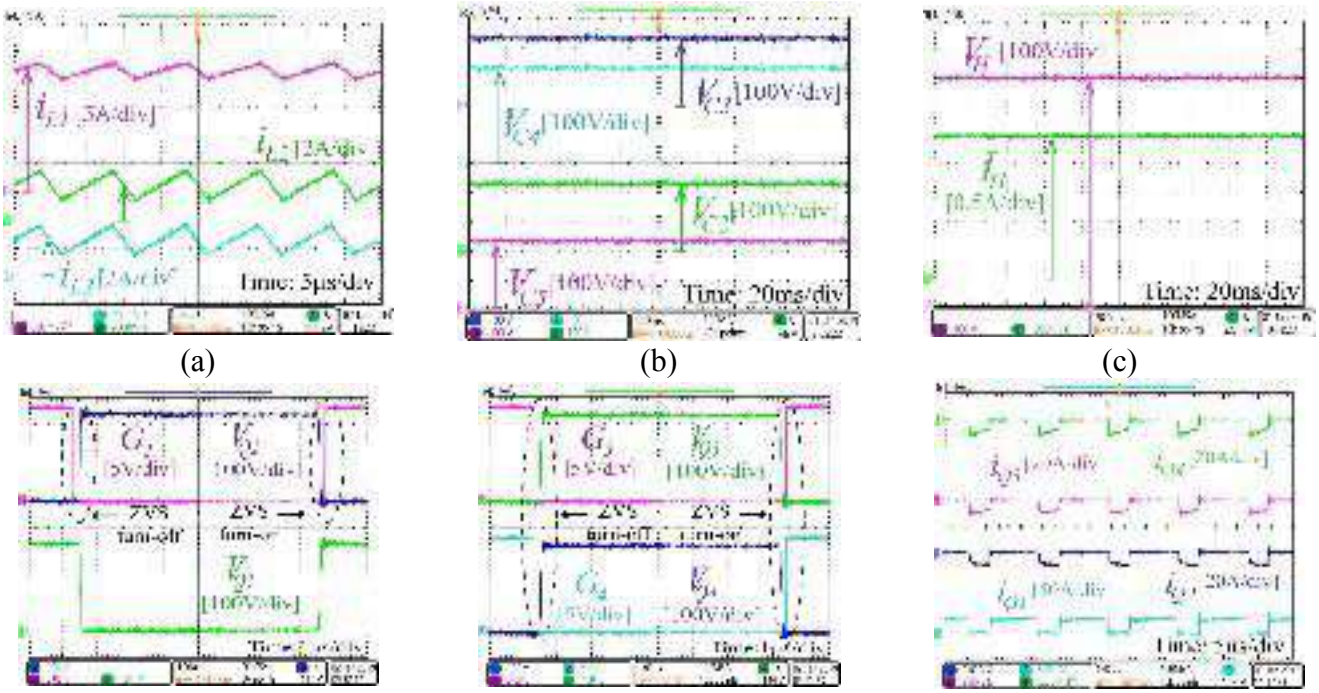
In order to assess the wide-voltage-gain range capability of the proposed converter in step-up and step-down modes, two tests were performed. In the first test, the converter operates in step-up mode with V_L =80V →200V, and a closed-loop voltage controller (i.e. proportional integral derivative (PID) controller) is used to set V_H at 800V. Figure 8.12(a) shows the results of this test, and it is clear that the converter with the adopted controller is capable of holding V_H constant at

800V with V_L changing widely, (M_{Boost} : 10→4). In the second test, the converter operates in the step-down mode with V_H = 800V and a closed-loop PID voltage controller is used to vary V_L from 200V to 80V. Figure 8.12(b) shows the results of this test, and it is clear that the converter with the adopted controller is capable of controlling V_L and varying it from 200V to 80V over six hundred milliseconds while V_H is constant at 800V, (M_{Buck} : 0.25→0.1). Both tests show that the converter has an acceptable dynamic performance under wide range of voltage gain.

8.5.1 Efficiency Analysis

The calculated power loss distributions in case study I and case study II are shown in Figure 8.13. Figure 8.13(a) shows that the efficiency of the converter in case study I is 95.29% with total losses of 98.7W, while Figure 8.13(b) shows that the efficiency of the converter in case study II is 98% with total losses of 39.3W. The loss distributions of both case studies show that the conduction losses of the capacitors are dominant, due to the utilization of electrolytic capacitors. These losses can be reduced by using film or ceramic capacitors with low equivalent series resistances.

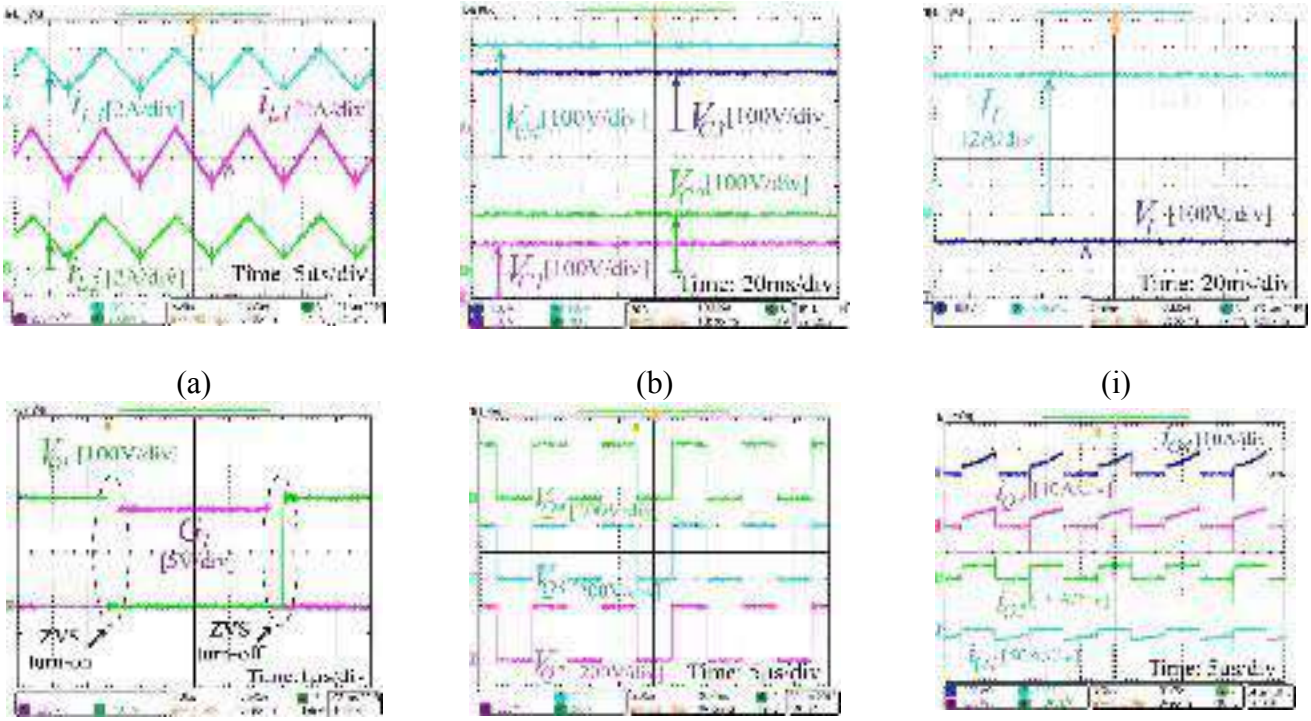
Figure 8.14. Shows the measured efficiency curves (using Tektronix PA3000 Power Analyzer) when the converter operates in step-up and step-down modes, versus V_L when it is changed from 80V to 200V while keeping V_H fixed at 800V at output power levels of 1kW and 2kW. In step-up mode, when P_{out} is 1kW, the converter has a peak efficiency of 97.8% at 200V and a minimum efficiency of 94.8% at 80V, and when P_{out} is 2kW, the converter has a peak efficiency of 97.2% at 200V and a minimum efficiency of 92.2% at 80V. In step-down mode, when P_{out} is 1kW, the converter has a highest efficiency of 98% at 200V and a minimum efficiency of 95.3% at 80V, and when P_{out} is 2kW, the converter has a maximum efficiency of 97.5% at 200V and a minimum efficiency of 92.7% at 80V.



(a) (b) (c)

(d) (e) (f)

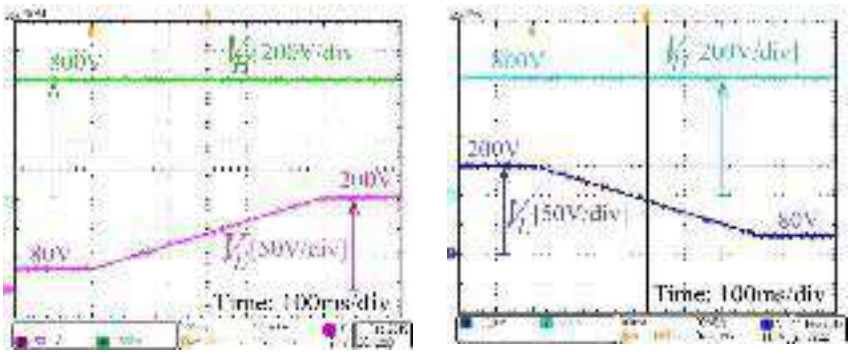
Figure 8.10: Experimental results of case study I.



(a) (b) (i)

(d) (e) (f)

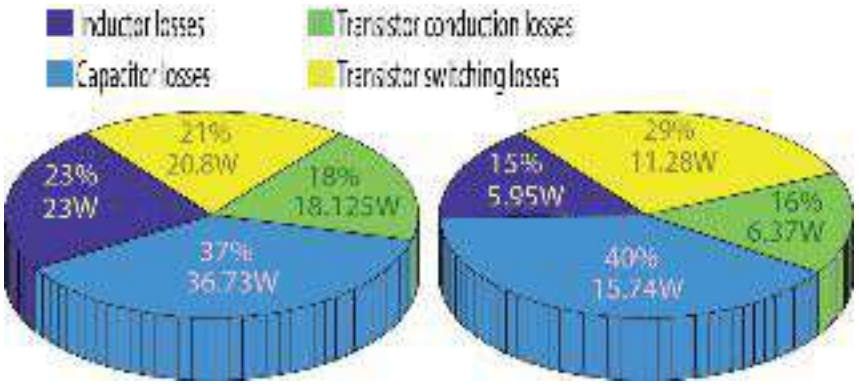
Figure 8.11: Experimental results of case study II.



(a) (b)

Figure 8.12: Dynamic performance under wide-range of voltage gain (VH = 800V, VL = 80V → 200V, and Po = 2kW). (a) Step-up mode. (b) Step-down mode.

It is plain that the proposed converter has acceptable efficiency throughout the broad range of its voltage gains. The reason for this is that the voltage stress on the switches of the proposed topology is inversely proportional with the voltage gain, as described by (11) and shown in Figure 8.7, which alleviates the switching losses of the switches at high voltage conversion ratios, hence, enhances the efficiency of the converter.



(a) (b)

Figure 8.13: Calculated power loss distributions for the experiment. (a) In case study I. (b) In case study II.

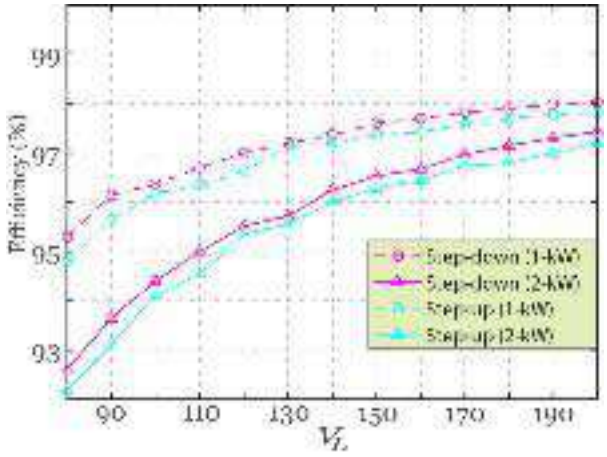


Figure 8.14: Measured efficiency curves of the proposed converter (VH = 800V, VL= 80V→200V, Po = 1kW, and 2kW).

8.6 Conclusion

A new topology of a bidirectional dc-dc converter has been proposed. The proposed converter has wide voltage conversion ratios, low voltage stress on the switches, common ground between the LV and HV sides, low current ripple, and high semiconductor utilization factor. at the LV side. Additionally, the adopted synchronous rectification reduces the conduction losses of the synchronous rectifiers. These features make the proposed topology an adequate interface for the energy storage systems with large voltage swings. A scaled-down 2-kW/800-V prototype has been built using SiC MOSFETs to verify the theoretical analysis, and the experimental results show that the converter has an acceptable steady-state and dynamic performance.

Chapter 9 A New Hybrid Structure of a Bidirectional DC-DC Converter with High Conversion Ratios for Electric Vehicles

9.1 Introduction

In this chapter, a new bidirectional dc-dc conv erter that is based on the quadratic and switched-capacitor structures is proposed for Electric Vehicle applications. The proposed converter has high voltage conversion ratios, low voltage stress on the semiconductor devices, constant potential difference between the grounds of its low voltage and high voltage ports, and continuous current at its low voltage port. Synchronous rectification is utilized to enhance the efficiency of the converter. In addition, an extended version of the proposed converter is discussed in this chapter. Finally, the experimental results obtained from a 2-kW/800-V scaled-down prototype validate the feasibility of the proposed topology and the correctness of its theoretical analysis.

9.2 Circuit Structure and Operating Principles of the Proposed Converter

9.2.1 Circuit of the Proposed Topology

The proposed converter has six switches ($Q_1 \rightarrow Q_6$), two inductors (L_1 and L_2), and five capacitors ($C_1 \rightarrow C_5$). The proposed topology is presented in Figure 9.1, as it is composed of a quadratic converter (Q_1, Q_2, Q_4, Q_5, L_1, L_2, C_1, C_3, and C_4) with an integrated switched capacitor network (Q_3, Q_6, C_2, and C_5). It has two ports, namely: the low voltage (LV) port, where the ESU is connected, and the high voltage (HV) port, where the dc bus of the load is connected.

9.2.2 Analysis and Operation in Step-Up Mode

In this mode, the power flows from the LV side to the HV side. The operation is divided into two switching states, namely: State 0 and State 1. In state 0, $Q_1 \rightarrow Q_3$ are off, $Q_4 \rightarrow Q_6$ are on, L_1 and L_2 discharge, $C_2 \rightarrow C_4$ charge, and C_5 discharges. In state 1, $Q_1 \rightarrow Q_3$ are on, $Q_4 \rightarrow Q_6$ are off,

L_1 and L_2 charge, $C_2 \rightarrow C_4$ discharge, and C_5 charges. In this mode of operation Q_1 and Q_2 act as main switches while $Q_3 \rightarrow Q_6$ act as synchronous rectifiers. The current flow paths in the step-up operation during State 0 and State 1 are shown in Figure 9.2.

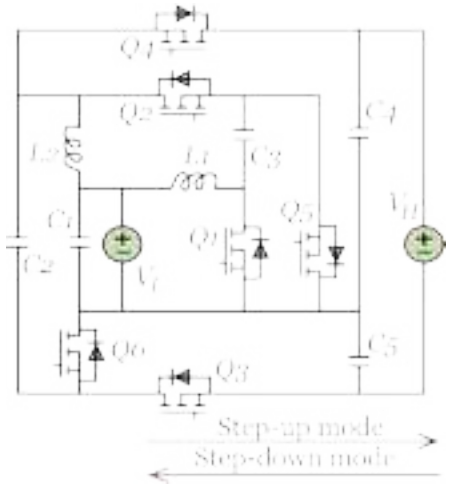


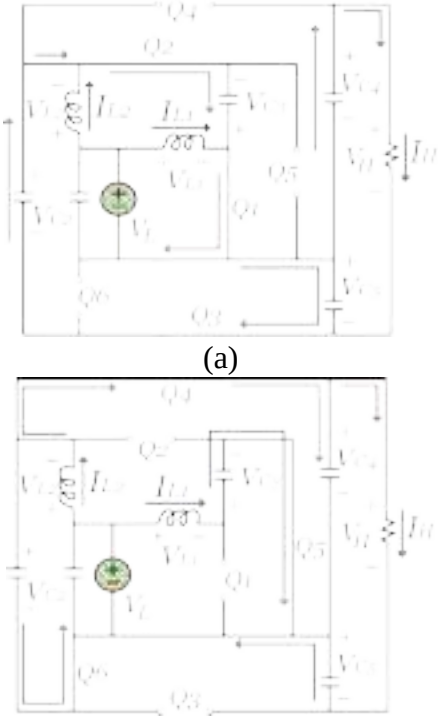
Figure 9.1: The structure of the proposed bidirectional dc-dc converter.

In the mathematical analysis of the converter, the voltages and currents at the LV and HV ports are referred to as V_L, V_H, I_L, and I_H, respectively. The voltages across $C_1 \rightarrow C_5$ are referred to as $V_{C1} \rightarrow V_{C5}$, the dc currents of L_1 and L_2 are I_{L1} and I_{L2}, and the instantaneous voltages across L_1 and L_2 are V_{L1} and V_{L2}, respectively. The charging currents of $C_1 \rightarrow C_5$ are $i_{C1\_ch} \rightarrow i_{C5\_ch}$, while the discharging currents of $C_1 \rightarrow C_5$ are $i_{C1\_dis} \rightarrow i_{C5\_dis}$. The duty cycle of $Q_1 \rightarrow Q_3$ is d_1, while the duty cycle of $Q_4 \rightarrow Q_6$ is d_2 (= 1-d_1). The key waveforms of the proposed converter in the step-up mode are shown in Figure 9.4(a), where $G_1 \rightarrow G_6$ are the gate triggering signals of $Q_1 \rightarrow Q_6$, and T is the periodic switching time.

The converter in State 0 can be analyzed by applying *Kirchhoff's Voltage Law* (KVL) and *Kirchhof's Current Law* (KCL) on the equivalent circuit in Figure 9.2(b), we can derive the following relationships:

$$\begin{cases} V_{L1} = V_L - V_{C3} \\ V_{L2} = V_L - V_{C4} \\ V_{C2} = V_{C4} \end{cases} \quad (1)$$

$$\begin{cases} i_{C2\_ch} = I_{L2} - I_H - i_{C4\_ch} \\ i_{C3\_ch} = I_{L1} \\ i_{C5\_dis} = I_H \end{cases} \quad (2)$$



(a)

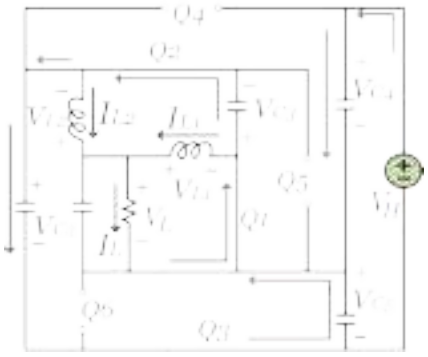
(b)

Figure 9.2: Current flow paths in step-up mode. (a) State 1. (b) State 0.

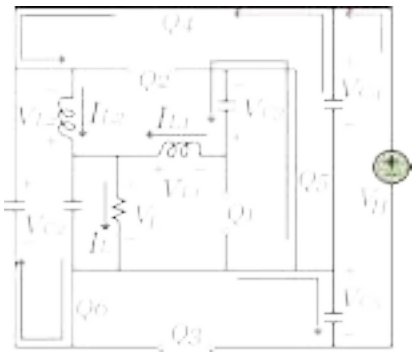
The converter in State 1 can be analyzed by applying KVL and KCL rules on the equivalent circuit in Figure 9.2(a), we can derive the following relationships:

$$\begin{cases} V_{L1} = V_L \\ V_{L2} = V_L + V_{C3} \end{cases} \quad (3)$$

$$\begin{cases} i_{C2\_dis} = I_H + i_{C5\_ch} \\ i_{C3\_dis} = I_{L2} + i_{C5\_ch} \\ i_{C4\_dis} = I_H \end{cases} \quad (4)$$



(a)



(b)

Figure 9.3: Current flow paths in step-down mode. (a) State 1. (b) State 0.

In State 1, Q_1 and Q_2 are turned on by G_1 and G_2, respectively. In this switching states, Q_3 acts as a synchronous rectifier, hence, to provide zero voltage switching (ZVS) for Q_3 during the turn on and turn off instants a time delay is applied between the rising edge of G_3 and the rising edge of G_1 and another time delay is applied between the falling edge of G_3 and the falling edge of G_1. During these delay times, current flows through the body diode of Q_3, thus, the voltage across between its drain and source drops to the forward voltage of the body diode (≈ 0V), which allows the ZVS realization. In State 0, Q_4, Q_5, and Q_6 conduct and act as synchronous rectifiers. In order to provide ZVS to them, a time delay should be applied between the rising edge of $G_4 \rightarrow G_6$ and the falling edge of G_1, and another time delay should be applied between the falling edge of $G_4 \rightarrow G_6$ and the ring edge of G_1, as shown in Figure 9.4(a).

By applying the volt-second balance rule on the three inductors, the voltages across the capacitors and the voltage gain in step-mode (M_{Boost}) can be extracted, as follows:

$$V_{C2} = V_{C4} = V_L \left(\frac{1}{1-d_1}\right)^2 \tag{5}$$

$$V_{C3} = V_L \frac{1}{1-d_1} \tag{6}$$

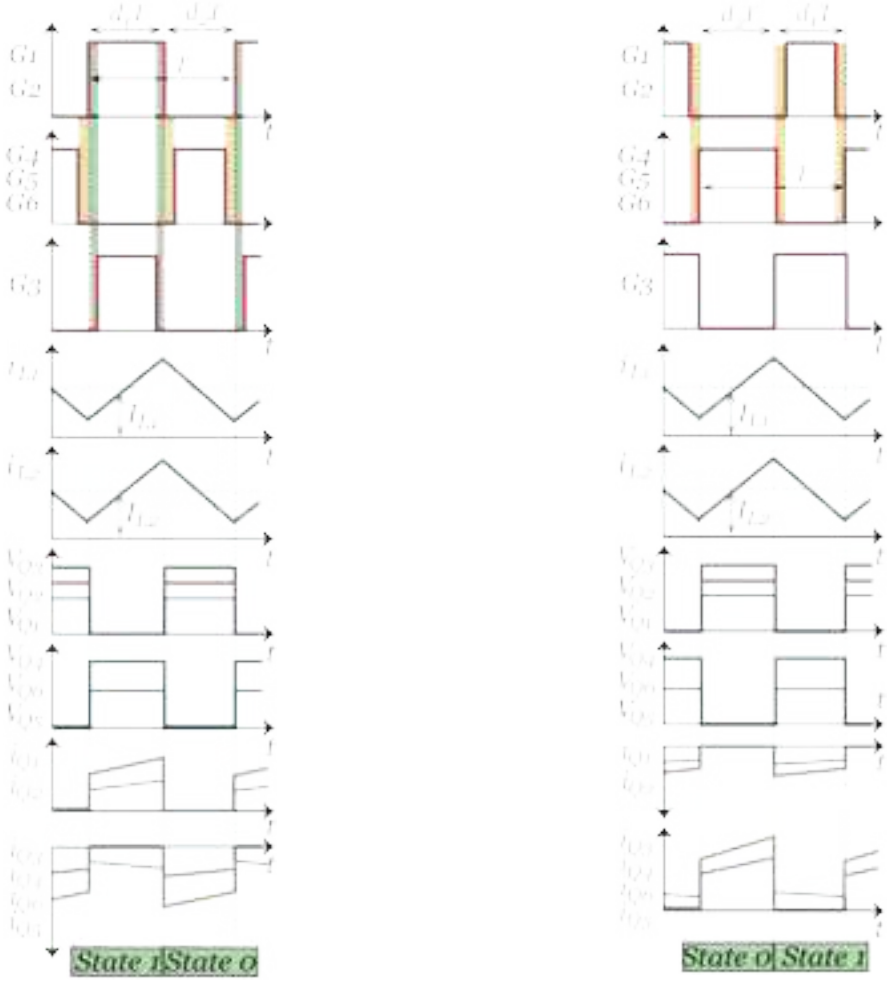
$$V_{C5} = V_L \frac{2-d_1}{(1-d_1)^2} \tag{7}$$

$$V_H = V_{C4} + V_{C5} = V_L \frac{3-d_1}{(1-d_1)^2} \tag{8}$$

$$M_{Boost} = \frac{V_H}{V_L} = \frac{3-d_1}{(1-d_1)^2} \tag{9}$$

9.2.3 Analysis and Operation in Step-Down Mode

In this mode, the power flows from the HV side to the LV side. Similarly, the operation has two switching states, namely: State 0 and State 1. In state 0, $Q_1 \rightarrow Q_3$ are off, $Q_4 \rightarrow Q_6$ are on, L_1 and L_2 charge, $C_2 \rightarrow C_4$ discharge, and C_5 charges. In state 1, $Q_1 \rightarrow Q_3$ are on, $Q_4 \rightarrow Q_6$ are off, L_1 and L_2 discharge, $C_2 \rightarrow C_4$ charge, and C_5 discharges. In this mode of operation $Q_3 \rightarrow Q_6$ act as main switches while Q_1 and Q_2 act as synchronous rectifiers. The current flow paths in the step-down operation during State 0 and State 1 are presented in Figure 9.3. In this mode, G_3 is complementary to $G_4 \rightarrow G_6$, a time delay is applied between the falling edge of G_1 and the rising edges of $G_4 \rightarrow G_6$, and another time delay is applied between the rising edge of G_1 and the falling edges of $G_4 \rightarrow G_6$ to provide ZVS to Q_1 and Q_2 during the turn on and turn off instants, as depicted in Figure 9.4(b).



(a) (b)

Figure 9.4: Important waveforms of the proposed converter. (a) Step-up mode. (b) Step-down mode.

Since $Q_1 \rightarrow Q_3$ are complementary to $Q_4 \rightarrow Q_6$, hence, the voltages across the capacitors and the voltage gain in step-down operation (M_{Buck}) can be directly extracted from (5)-(9) by replacing d_1 by (1-d_2), as follows:

$$V_{C2} = V_{C4} = V_H \frac{1}{2 + d_2} \tag{10}$$

$$V_{C3} = V_H \frac{d_2}{2 + d_2} \tag{11}$$

$$V_{C5} = V_H \frac{1 + d_2}{2 + d_2} \tag{12}$$

$$V_L = V_H \frac{{d_2}^2}{2 + d_2} \tag{13}$$

$$M_{Buck} = \frac{V_L}{V_H} = \frac{{d_2}^2}{2 + d_2} \tag{14}$$

9.2.4 Voltage and Current Stresses on the Switches

The voltage stresses across the six switches can be deduced by applying the KVL rule on the equivalent circuits of the proposed converter in Figure 9.2 and Figure 9.3, as follows:

$$V_{Q1} = V_{Q5} = V_L \frac{1}{1 - d_1} = V_H \frac{d_2}{2 + d_2} \tag{15}$$

$$V_{Q2} = V_L \left(\frac{1}{1 - d_1}\right)^2 = V_H \frac{1}{2 + d_2} \tag{16}$$

$$V_{Q3} = V_{Q4} = V_{Q6} = V_L \frac{2 - d_1}{(1 - d_1)^2} = V_H \frac{1 + d_2}{2 + d_2} \tag{17}$$

By means of (9), the voltage stresses described by (15)-(17) can be expressed as functions in M_{Boost}, as follows:

$$V_{Q1} = V_{Q5} = V_H \frac{\sqrt{1 + 8M_{Boost}} - 1}{4M_{Boost}} \tag{18}$$

$$V_{Q2} = V_H \frac{4M_{Boost} - \sqrt{1 + 8M_{Boost}} + 1}{8M_{Boost}} \tag{19}$$

$$V_{Q3} = V_{Q4} = V_{Q6} = V_H \frac{4M_{Boost} + \sqrt{1 + 8M_{Boost}} - 1}{8M_{Boost}} \tag{20}$$

The normalized voltage stresses on the six switches of the proposed converter are plotted in Figure 9.5. The current stresses on the power switches and inductors can be deduced by applying the charge-second balance on (2) and (4), as follows:

$$I_{L1} = I_H \frac{1 + d_1}{(1 - d_1)^2} = I_L \frac{2 - d_2}{2 + d_2} \tag{21}$$

$$I_{L2} = I_H \frac{2}{1 - d_1} = I_L \frac{2d_2}{2 + d_2} \tag{22}$$

$$i_{Q1} = I_H \frac{1 + d_1}{d_1(1 - d_1)^2} = I_L \frac{2 - d_2}{(2 + d_2)(1 - d_2)} \tag{23}$$

$$i_{Q2} = I_H \frac{1 + d_1}{d_1(1 - d_1)} = I_L \frac{d_2(2 - d_2)}{(2 + d_2)(1 - d_2)} \tag{24}$$

$$i_{Q3} = I_H \frac{1}{d_1} = I_L \frac{{d_2}^2}{(2 + d_2)(1 - d_2)} \tag{25}$$

$$i_{Q4} = i_{Q6} = I_H \frac{1}{1 - d_1} = I_L \frac{d_2}{(2 + d_2)} \tag{26}$$

$$i_{Q5} = I_H \frac{1+d_1}{(1-d_1)^2} = I_L \frac{2-d_2}{(2+d_2)} \tag{27}$$

9.3 Design of Components and Efficiency Analysis of the Proposed Converter

9.3.1 Power Switches Selection

Equations (15)-(17) and (23)-(27) describe the voltage and current stresses on the six switches, respectively. Accordingly, when the range of voltage gain and load are known, the peak stresses can be calculated. The calculated current and voltage stresses should be within the safe-operating-area (SOA) of the selected power switches.

9.3.2 Design of Inductors

When the ranges of the operating voltage gain and load are known, the allowed maximum current ripples of the inductors (i.e. Δi_{L1} and Δi_{L2}) and the switching frequency f_s are determined, the minimum required inductance can be calculated as follows:

$$\begin{cases} L_1 \geq \dfrac{d_1 V_L}{f_s \Delta i_{L1}} \\ L_2 \geq \dfrac{d_1 V_L}{f_s \Delta i_{L2}} \left(\dfrac{2-d_1}{1-d_1}\right) \end{cases} \tag{28}$$

Additionally, the peak current stresses of the two inductors can be deduced by means of (21) and (22), hence, the designed inductors should tolerate these currents.

9.3.3 Design of Capacitors

The voltages across the capacitors can be calculated using (5)-(8) and (10)-(13). The relationships between the capacitances of the five capacitors and their corresponding ripple voltage are described by (29). Hence, when the operating voltage gain and loading ranges are knows, the required capacitance and voltage rating of the five capacitors can be deduced.

$$\begin{cases} C_1 \geq \dfrac{d_1 V_L}{8 {f_s}^2 \Delta V_{C1}} \left(\dfrac{1}{L_1} + \dfrac{1}{L_2(1-d_1)} \right) \\ C_2 \geq \dfrac{I_H}{f_s \Delta V_{C2}} \\ C_3 \geq \dfrac{(1+d_1) I_H}{f_s (1-d_1) \Delta V_{C3}} \\ C_4 \geq \dfrac{d_1 I_H}{f_s \Delta V_{C4}} \\ C_5 \geq \dfrac{(1-d_1) I_H}{f_s \Delta V_{C5}} \end{cases} \tag{29}$$

9.3.4 Efficiency Analysis

Calculating the efficiency of the power converter is very important to adequately design the cooling system, additionally, it gives an idea about the operating conditions where the proposed topology has the maximum/minimum efficiency. The power loss of the converter P_{Loss} is described by (30), where $P_{Q(cond)}$, $P_{Q(sw)}$, $P_{L(cond)}$, $P_{L(core)}$, and $P_{C(cond)}$ are the conduction and switching losses of the six switches, the conduction and core losses of the two inductors, and the conduction loss of the five capacitors.

$$P_{loss} = P_{Q(cond)} + P_{Q(sw)} + P_{L(cond)} + P_{L(core)} + P_{C(cond)} \tag{30}$$

These losses can be calculated using (31)-(36), as follows:

$$P_{Q(cond)} = \sum_{j=1}^{j=6} i_{Qj(rms)}^2 r_{dsj} \tag{31}$$

$$P_{Q(sw)} = \begin{cases} P_{Q1(sw)} + P_{Q2(sw)} & \text{(Step-up mode)} \\ \sum_{j=3}^{j=6} P_{Qj(sw)} & \text{(Step-down mode)} \end{cases} \tag{32}$$

$$P_{Qj(sw)} = f_s (0.5 V_{Qj} i_{Qj} (t_{rj} + t_{fj}) + 0.5 {V_{Qj}}^2 C_{OSSj}) \tag{33}$$

Where $r_{ds1} \rightarrow r_{ds6}$, $t_{r1} \rightarrow t_{r6}$, $t_{f1} \rightarrow t_{f6}$, $C_{OSS1} \rightarrow C_{OSS6}$ are the on resistances, the rising times, the falling times, and the parasitic output capacitances of the six switches. The switching loss of the

proposed converter, described by (32), depends on the mode of operation, as in step-up mode $Q_3 \rightarrow Q_6$ are soft-switched, while in step-down mode Q_1 and Q_2 are soft-switched. The root-mean-square (rms) currents of the six switches can be calculated as in (34).

$$\begin{aligned} i_{Q1(rms)} &= I_H \left(\frac{1+d_1}{\sqrt{d_1}(1-d_1)^2} \right) \\ i_{Q2(rms)} &= I_H \left(\frac{1+d_1}{\sqrt{d_1}(1-d_1)} \right) \\ i_{Q3(rms)} &= I_H \left(\frac{1}{\sqrt{d_1}} \right) \\ i_{Q4(rms)} &= i_{Q6(rms)} = I_H \left(\frac{1}{\sqrt{1-d_1}} \right) \\ i_{Q5(rms)} &= I_H \left(\frac{1+d_1}{\sqrt{(1-d_1)^3}} \right) \end{aligned} \tag{34}$$

The conduction and core losses of the two inductors are described by (35) and (36), where r_{L1}, r_{L2}, l_{c1}, l_{c2}, A_{c1}, A_{c2}, ΔB_1, and ΔB_2 are the series resistances of the two inductors, the lengths of the magnetic flux path of the cores of the two inductors, the cross sectional areas of the cores of the two inductors, and ac magnetic flux density of the two inductors.

$$P_{L(cond)} = {I_{L1}}^2 r_{L1} + {I_{L2}}^2 r_{L2} \tag{35}$$

$$P_{L(core)} = l_{c1}\, A_{c1} \left(a\, \Delta B_1^b\, f_s^C \right) + l_{c2}\, A_{c2} \left(a\, \Delta B_2^b\, f_s^C \right) \tag{36}$$

As a, b, and c are fitting parameters that can be derived from the datasheet of the cores. The conduction losses of the five capacitors can be calculated using (37), where $r_{C1} \rightarrow r_{C5}$ are the equivalent series resistances of the five capacitors. The rms values of the capacitors' currents are described by (38).

$$P_{C(cond)} = \sum_{j=1}^{j=5} i_{Cj(rms)}^2 r_{Cj} \tag{37}$$

$$\begin{cases} i_{C1(rms)} = \dfrac{d_1 V_L}{2\sqrt{3} f_s}\left(\dfrac{1}{L_1} + \dfrac{1}{L_2(1-d_1)}\right) \\ i_{C2(rms)} = I_H \sqrt{\dfrac{3{d_1}^2 - 3d_1 + 1}{{d_1}^2 (1-d_1)^2}} \\ i_{C3(rms)} = I_H \sqrt{\dfrac{(1+d_1)^2}{d_1 (1-d_1)^3}} \\ i_{C4(rms)} = I_H \sqrt{\dfrac{3{d_1}^2 - 3d_1 + 1}{(1-d_1)^2}} \\ i_{C5(rms)} = I_H \sqrt{\dfrac{1-d_1}{d_1}} \end{cases} \tag{38}$$

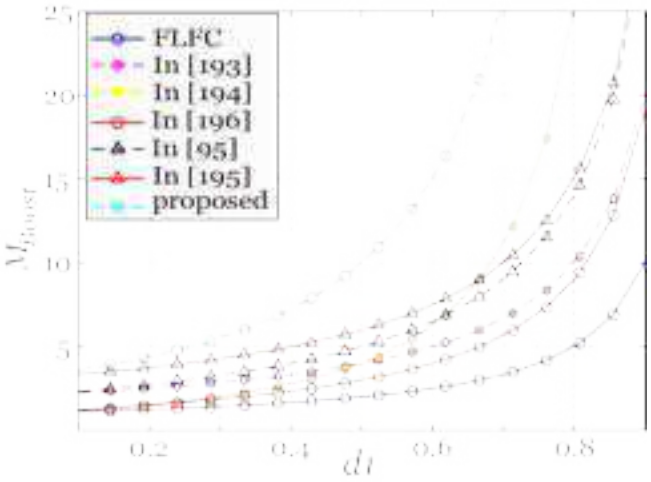
Finally, the efficiency η is depicted by (39):

$$\eta = \begin{cases} \dfrac{V_L I_L}{P_{Loss} + V_L I_L} & \text{(Step-up mode)} \\ \dfrac{V_H I_H}{P_{Loss} + V_H I_H} & \text{(Step-down mode)} \end{cases} \tag{39}$$

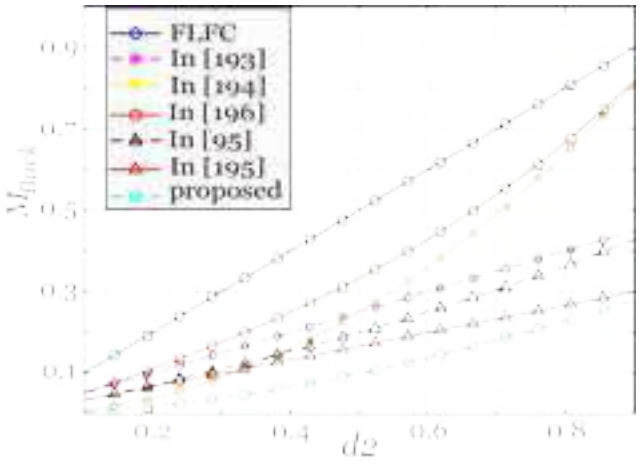
9.4 Comparative Study

The proposed converter is compared with seven other BDC topologies in this section. The BDC architectures in this comparative study are a four-level flying capacitor (FLFC) converter, the quadratic BDC in [194], the switched-capacitor BDC in [195] with two multiplier cells, the new three-level BDC in [193], the hybrid BDC with switched-capacitor cell in [196], the hybrid converter with a quasi-Z-source and a switched-capacitor networks in [95], and the conventional cascaded bidirectional converter (CCBC). Table 9.1 concludes the features of each BDC topology including the number of active and passive components, the voltage gain in step-up and step-down

modes, and the potential difference between the grounds of the LV and HV ports ($V_{Grounds}$). The voltage gain curves of the compared converters versus the duty cycle in step-up and step-down modes are shown in Figure 9.6. The proposed converter has the highest voltage gain in the step-up mode and the lowest voltage gain in the step-down mode in comparison to the other converters in this study. The converters in [193] and [196] have HF PWM potential difference between the grounds of their ports which limits their applications.



(a)



(b)

Figure 9.5: Comparison of voltage gain between the proposed converter and other BDC solutions. (a) In step-up mode. (b) In step-down mode.

In order to compare the relative total cost of the power switches used in each topology, the semiconductor utilization factor (U_F) is utilizes, and it is defined by (40), where P_o is the output power of the converter, V_{Qj} and $i_{Qj\ (rms)}$ are the voltage stress and the rms current stress on switch Q_j.

$$U_F = \frac{P_o}{\sum V_{Qj}\ i_{Qj\ (rms)}} \tag{40}$$

Table 9.1: COMPARISON BETWEEN THE PROPOSED AND OTHER BDC SOLUTIONS

Topology	Components	$V_{Grounds}$	Voltage gain	
			Step-up mode	Step-down mode
FLFC	6 Switches 1 Inductor 4 Capacitors	0V	$M_{Boost} = \frac{1}{1-d_1}$	$M_{Buck} = d_2$
Converter in [193]	4 Switches 2 Inductors 3 Capacitors	HF PWM voltage	$M_{Boost} = \frac{2}{1-d_1}$	$M_{Buck} = \frac{d_2}{2}$
Quadratic in [194]	4 Switches 2 Inductor 3 Capacitors	0V	$M_{Boost} = \left(\frac{1}{1-d_1}\right)^2$	$M_{Buck} = {d_2}^2$
Converter in [195] (n=2)	6 Switches 1 Inductor 6 Capacitors	0V	$M_{Boost} = \frac{3}{1-d_1}$	$M_{Buck} = \frac{d_2}{3}$
Converter in [196]	3 Switches 2 Inductors 4 Capacitors	HF PWM voltage	$M_{Boost} = \frac{1+d_1}{1-d_1}$	$M_{Buck} = \frac{d_2}{2-d_2}$
Converter in [95]	5 Switches 2 Inductors 6 Capacitors	Constant voltage	$M_{Boost} = \frac{2+d_1}{1-d_1}$	$M_{Buck} = \frac{d_2}{3-d_2}$
CCBC	4 Switches 2 Inductor 3 Capacitors	0V	$M_{Boost} = \left(\frac{1}{1-d_1}\right)^2$	$M_{Buck} = {d_2}^2$
Proposed	6 Switches 2 Inductors 5 Capacitors	Constant voltage	$M_{Boost} = \frac{3-d_1}{(1-d_1)^2}$	$M_{Buck} = \frac{{d_2}^2}{2+d_2}$

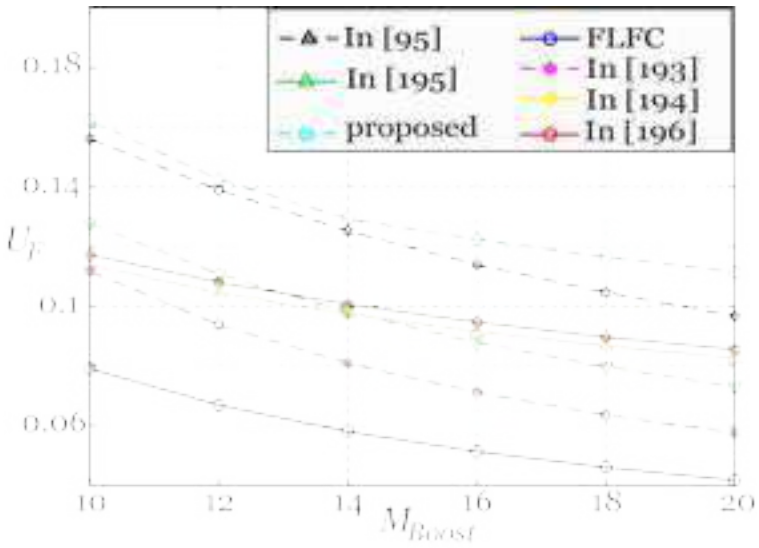


Figure 9.6: Semiconductor utilization factor for the compared BDC solutions.

The ratio between the output power of a dc-dc converter and the total power processed by the power switches of that converter should be as high as possible to reduce the cost of the semiconductor devices. Figure 9.7 shows the semiconductor utilization factor curves of the compared converters versus M_{Boost} when P_o = 2kW and V_H = 800V. It is clear that the proposed converter has the highest semiconductor utilization factor compared to the other converters.

The comparative study shows that the proposed BDC topology combines a number of features such as high voltage conversion ratios, high semiconductor utilization factor, and constant potential difference between the grounds of its LV and HV ports, which make it an excellent interface for the ESUs.

9.5 Extended Structure of the Proposed Converter

Since the proposed converter encompasses a switched-capacitor network, hence, this network can have more than one switched-capacitor cell in order to extend the voltage gain range and reduce the voltage stress on the individual power switches.

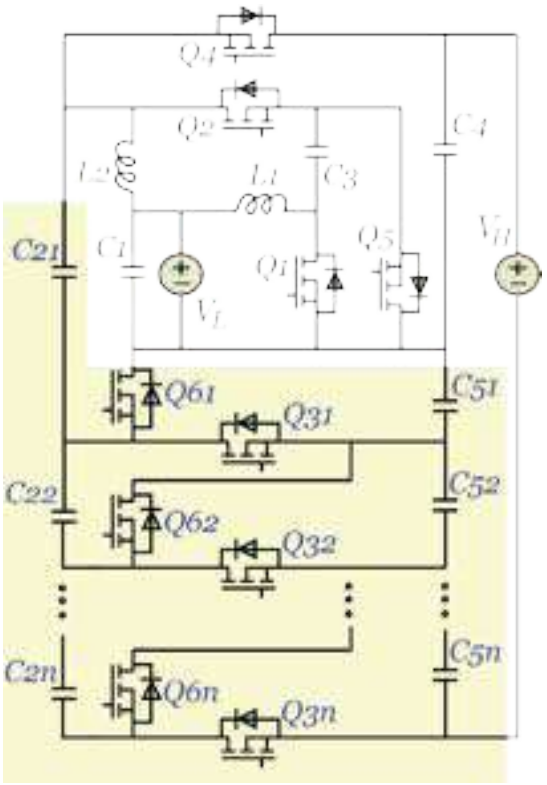


Figure 9.7: The extended structure of the proposed converter with n switched-capacitor cells.

Figure 9.8 shows the extended structure of the proposed converter with *n* switched-capacitor cells. The extended structure with *n* switched-capacitor cells is composed of *4+2n* power switches, *3+2n* capacitors, and two inductors. The switches $Q_{31} \rightarrow Q_{3n}$ and $Q_{61} \rightarrow Q_{6n}$ have the same switching states as Q_3 and Q_6, respectively, discussed in Section II, as $Q_{31} \rightarrow Q_{3n}$ only conduct in state 1, while $Q_{61} \rightarrow Q_{6n}$ only conduct in state 0. Similarly, $C_{21} \rightarrow C_{2n}$ and $C_{51} \rightarrow C_{5n}$ have the same charge/discharge states as C_2 and C_5, respectively, illustrated in Section II, where $C_{21} \rightarrow C_{2n}$ charge in state 0 and discharge in state 1, while $C_{51} \rightarrow C_{5n}$ discharge in state 0 and charge in state 1.

The voltage across the capacitors of the extended structure are described by (41), while the voltage at the HV port is defined by (42).

$$\begin{cases} V_{C21} = V_{C4} = \dfrac{V_L}{(1-d_1)^2} = \dfrac{V_H}{1+n+nd_2} \\ V_{C22} \to V_{C2n} = \dfrac{(2-d_1)V_L}{(1-d_1)^2} = \dfrac{(1+d_2)V_H}{1+n+nd_2} \\ V_{C3} = \dfrac{V_L}{1-d_1} = \dfrac{d_2 V_H}{1+n+nd_2} \\ V_{C51} \to V_{C5n} = \dfrac{(2-d_1)V_L}{(1-d_1)^2} = \dfrac{(1+d_2)V_H}{1+n+nd_2} \end{cases} \tag{41}$$

$$V_H = V_{C4} + \sum_{j=1}^{j=n} V_{C5j} = V_L \frac{1+n(2-d_1)}{(1-d_1)^2} \tag{42}$$

Accordingly, the voltage gains in step-up mode $\left(\grave{M}_{Boost}\right)$ and step-down mode $\left(\grave{M}_{Buck}\right)$ can be defined as in (43) and (44).

$$\grave{M}_{Boost} = \frac{V_H}{V_L} = \frac{1+n(2-d_1)}{(1-d_1)^2} \tag{43}$$

$$\grave{M}_{Buck} = \frac{V_L}{V_H} = \frac{{d_2}^2}{1+n(1+d_2)} \tag{44}$$

Figure 9.9 shows the voltage gain curves of the extended structure in step-up and step-down modes. The voltage stresses across the power switches of the extended structure are described by (45)-(48).

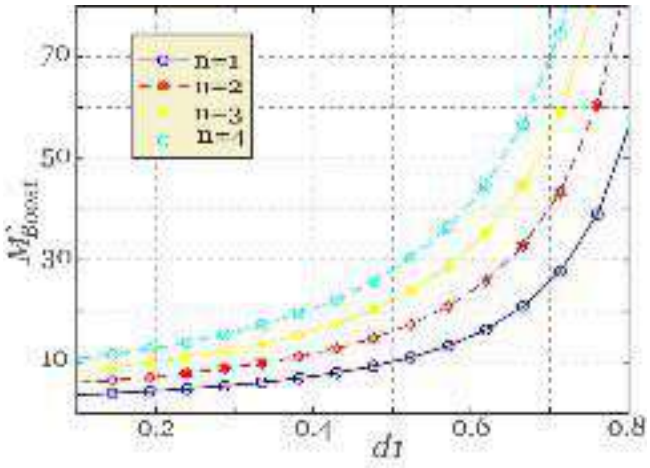
$$V_{Q1} = V_{Q5} = \frac{V_L}{1-d_1} = \frac{d_2 V_H}{1+n+nd_2} \tag{45}$$

$$V_{Q2} = \left(\frac{V_L}{1-d_1}\right)^2 = \frac{V_H}{1+n+nd_2} \tag{46}$$

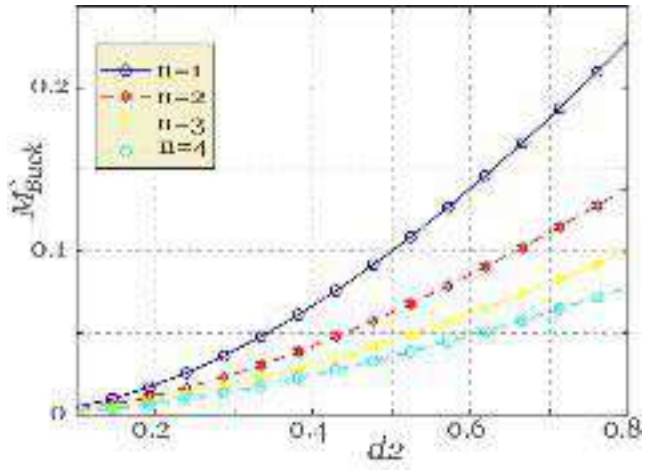
$$V_{Q31} \rightarrow V_{Q3n} = V_{Q4} = \frac{(2-d_1)V_L}{(1-d_1)^2} = \frac{(1+d_2)V_H}{1+n+nd_2} \tag{47}$$

$$V_{Q61} \rightarrow V_{Q6n} = \frac{(2-d_1)V_L}{(1-d_1)^2} = \frac{(1+d_2)V_H}{1+n+nd_2} \tag{48}$$

By means of (43), equations (45-(48) can be defined as functions in the voltage gain, as following:



(a)



(b)

Figure 9.8: Voltage gain of the proposed extended structure with different number of switched-capacitor cells. (a) In step-up mode. (b) In step-down mode.

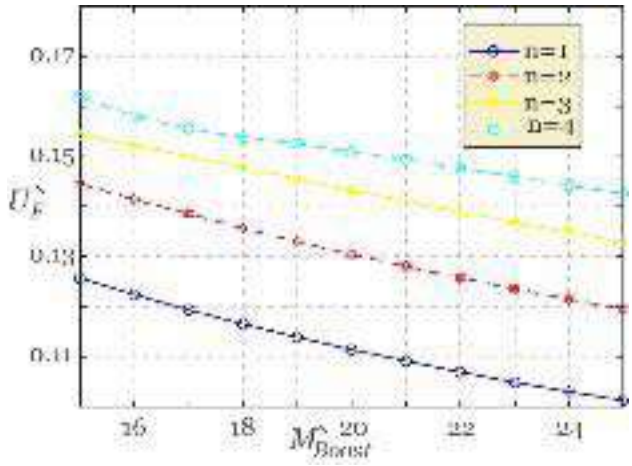


Figure 9.9: Semiconductor utilization factor of the proposed extended structure with different number of switched-capacitor cells.

$$V_{Q1} = V_{Q5} = V_H \left(\frac{\sqrt{n^2 + 4\grave{M}_{Boost}(1+n)} - n}{2\grave{M}_{Boost}(1+n)} \right) \tag{49}$$

$$V_{Q2} = V_H \left(\frac{2\grave{M}_{Boost}(1+n) - n\sqrt{n^2 + 4\grave{M}_{Boost}(1+n)} + n^2}{2\grave{M}_{Boost}(1+n)} \right) \tag{50}$$

$$V_{Q31} \rightarrow V_{Q3n} = V_{Q4} = V_{Q61} \rightarrow V_{Q6n} = V_H \left(\frac{2\grave{M}_{Boost}(1+n) + \sqrt{n^2 + 4\grave{M}_{Boost}(1+n)} - n}{2\grave{M}_{Boost}(1+n)} \right) \tag{51}$$

The currents of the two inductors can be calculated using (52) and (53), while the current stresses of the power switches are described by (54)-(58).

$$I_{L1} = I_H \frac{n + d_1}{(1-d_1)^2} = I_L \frac{1 + n - d_2}{1 + n + nd_2} \tag{52}$$

$$I_{L2} = I_H \frac{n+1}{1-d_1} = I_L \frac{d_2(1+n)}{1+n+nd_2} \tag{53}$$

$$i_{Q1} = I_H \frac{n + d_1}{d_1(1 - d_1)^2} = I_L \frac{1 + n - d_2}{(1 - d_2)(1 + n + nd_2)} \tag{54}$$

$$i_{Q2} = I_H \frac{n + d_1}{d_1(1 - d_1)} = I_L \frac{d_2(1 + n - d_2)}{(1 - d_2)(1 + n + nd_2)} \tag{55}$$

$$i_{Q31} \rightarrow i_{Q3n} = I_H \frac{1}{d_1} = I_L \frac{{d_2}^2}{(1 - d_2)(1 + n + nd_2)} \tag{56}$$

$$i_{Q4} = i_{Q61} \rightarrow i_{Q6n} = I_H \frac{1}{(1 - d_1)} = I_L \frac{d_2}{(1 + n + nd_2)} \tag{57}$$

$$i_{Q5} = I_H \frac{n + d_1}{(1 - d_1)^2} = I_L \frac{1 + n - d_2}{1 + n + nd_2} \tag{58}$$

The rms currents of the power switches can be calculated via (59), as follows:

$$\begin{aligned}
i_{Q1(rms)} &= I_H \left(\frac{n + d_1}{\sqrt{d_1}(1 - d_1)^2} \right) \\
i_{Q2(rms)} &= I_H \left(\frac{n + d_1}{\sqrt{d_1}(1 - d_1)} \right) \\
i_{Q31} \rightarrow i_{Q3n} &= I_H \left(\frac{1}{\sqrt{d_1}} \right) \\
i_{Q4(rms)} = i_{Q61(rms)} &\rightarrow i_{Q6n(rms)} = I_H \left(\frac{1}{\sqrt{1 - d_1}} \right) \\
i_{Q5(rms)} &= I_H \left(\frac{n + d_1}{\sqrt{(1 - d_1)^3}} \right)
\end{aligned} \tag{59}$$

Figure 9.10 shows the semiconductor utilization factor of the extended structure of the proposed converter with different number of switched-capacitor cells. It shows that as the number of the switched-capacitor cells increases, the semiconductor utilization factor of the converter gets enhanced.

9.6 Experimental Results and Analysis

In order to validate the proposed topology and assess the correctness of its theoretical analysis, an experimental setup was developed, shown in Figure 9.11. The power rating of the prototype is 2 kW, the voltage of the HV side is 800V, and the voltage of the LV port is allowed to swing between 80V and 160V (with output power of 2 kW). The power circuit of the developed setup is composed of Silicon Carbide (SiC) MOSFETs. The controller used is a TMS320f28335 microcontroller from Texas Instruments, and the switching frequency is 100 kHz. The values of the used inductors and capacitors, and the part numbers of the power switches are enlisted in Table 9.2. The built prototype has one switched-capacitor network (n = 1). Two case studies are discussed in this section, namely: case study I and case study II. In case study I, the operation of the proposed converter is investigated in step-up mode, while in case study II, the operation of the proposed converter is evaluated in step-down mode. The experimental results of case study I and case study II are shown in Figure 9.12 and Figure 9.13, respectively.

Table 9.2: Main Experimental Parameters of The Proposed Converter

Parameters and Components	Values
Rated power P_o	2-kW
HV side voltage V_H	800-V
LV side voltage V_L	80-V→160-V
Switch Q_1, Q_2	UF3C065040K3S
Switches Q_3, Q_4, Q_6	E3M0120090D
Switch Q_5	UJ3C065080K3S
Inductors L_2, L_3	250 µH
Capacitors C_1, C_2, C_3	150 µF
Capacitors C_4, C_5	180 µF
Switching frequency f_s	100 kHz
Microcontroller	TMS320f28335

Figure 9.10: Experimental prototype.

9.6.1 Case Study I

In this case study, the operation of the proposed converter is evaluated in step-up mode. The parameters of operation are as following: V_L = 80V, d_1 = 0.5, and the load connected to the HV port is represented by a resistor of 320Ω. The voltage across the capacitors of the converter can be calculated using (5)-(7), the voltage at the HV port of the converter and the step-up voltage gain in this case study can be deduced via (8) and (9), respectively, as following: V_{C2} = V_{C4} = 320V, V_{C3} = 160V, V_{C5} = 480V, V_H = 800V, and M_{Boost} = 10, which closely agree with the experimental results in Figure 9.12(b) and Figure 9.12(c). The currents and the ripple currents of L_1 and L_2 can be calculated using (21), (22), and (28), as follows: I_{L1} = 15A, I_{L2} = 10A, Δi_{L1} = 1.6A, and Δi_{L2} = 4.8A. These values are in close agreement with the results in Figure 9.12(a). The voltage stress across the six switches can be calculated by means of (15)-(17), as follows: V_{Q1} = V_{Q5} = 160V, V_{Q2} = 320V, V_{Q3} = V_{Q4} = V_{Q6} = 480V. The experimental results in Figure 9.12(d), Figure 9.12(e), and Figure 9.12(f) confirm the correctness of the calculated values. The current stresses of the six switches can be calculated by (23)-(27), as: i_{Q1} = 30A, i_{Q2} = 15A, i_{Q3} = 5A, i_{Q4} = i_{Q6} = 5A, and i_{Q5} = 15A, which closely agree with the results in Figure 9.12(g), Figure 9.12(h), and Figure 9.12(i).

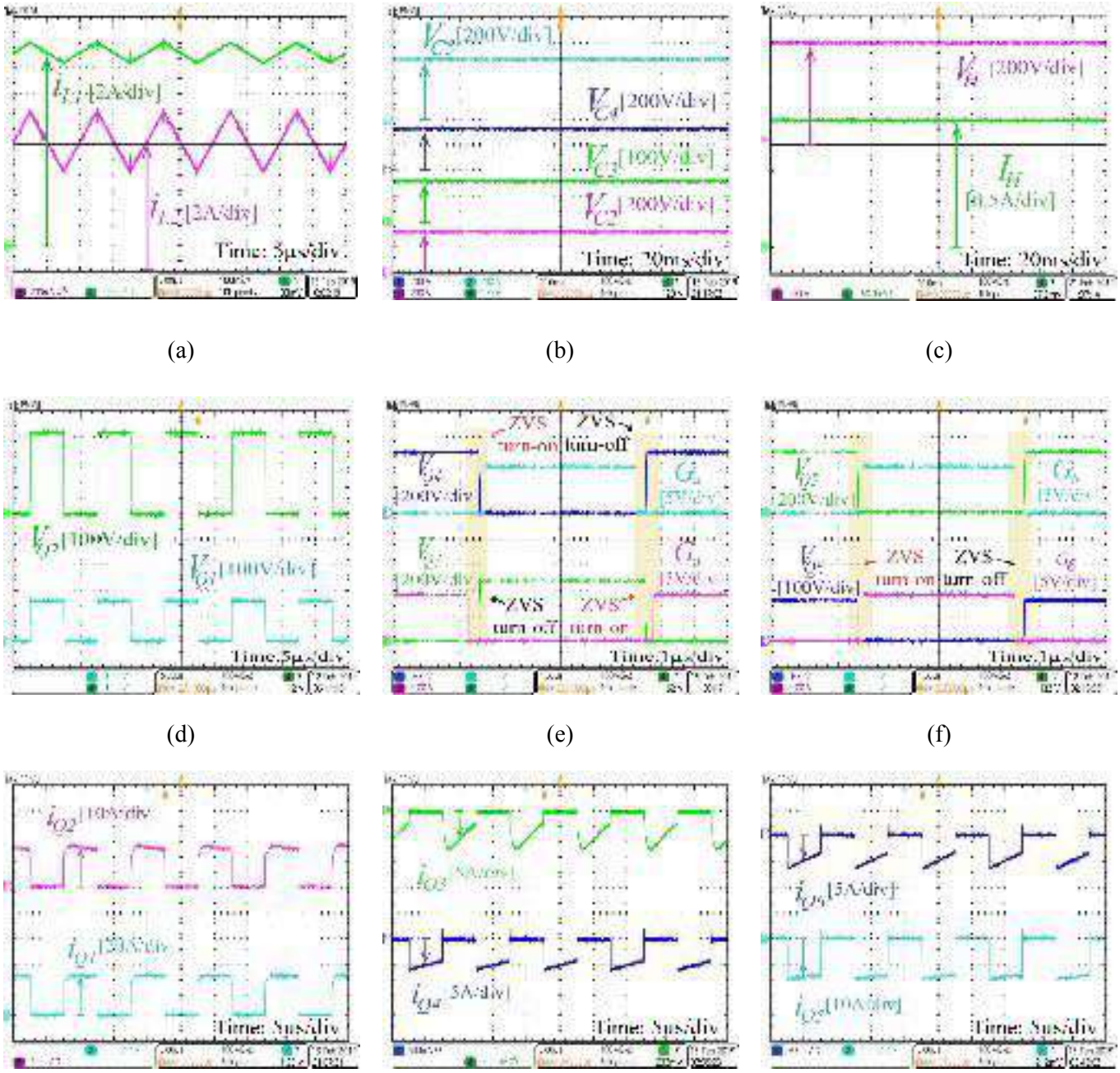


Figure 9.11: Experimental results of case study I.

In this case study, $Q_3 \rightarrow Q_6$ act as synchronous rectifiers, thus, when a delay is applied to their gate pulses, ZVS can be achieved at the turn on and turn off instants, which is confirmed by Figure 9.12(e) and Figure 9.12(f).

9.6.2 Case Study II

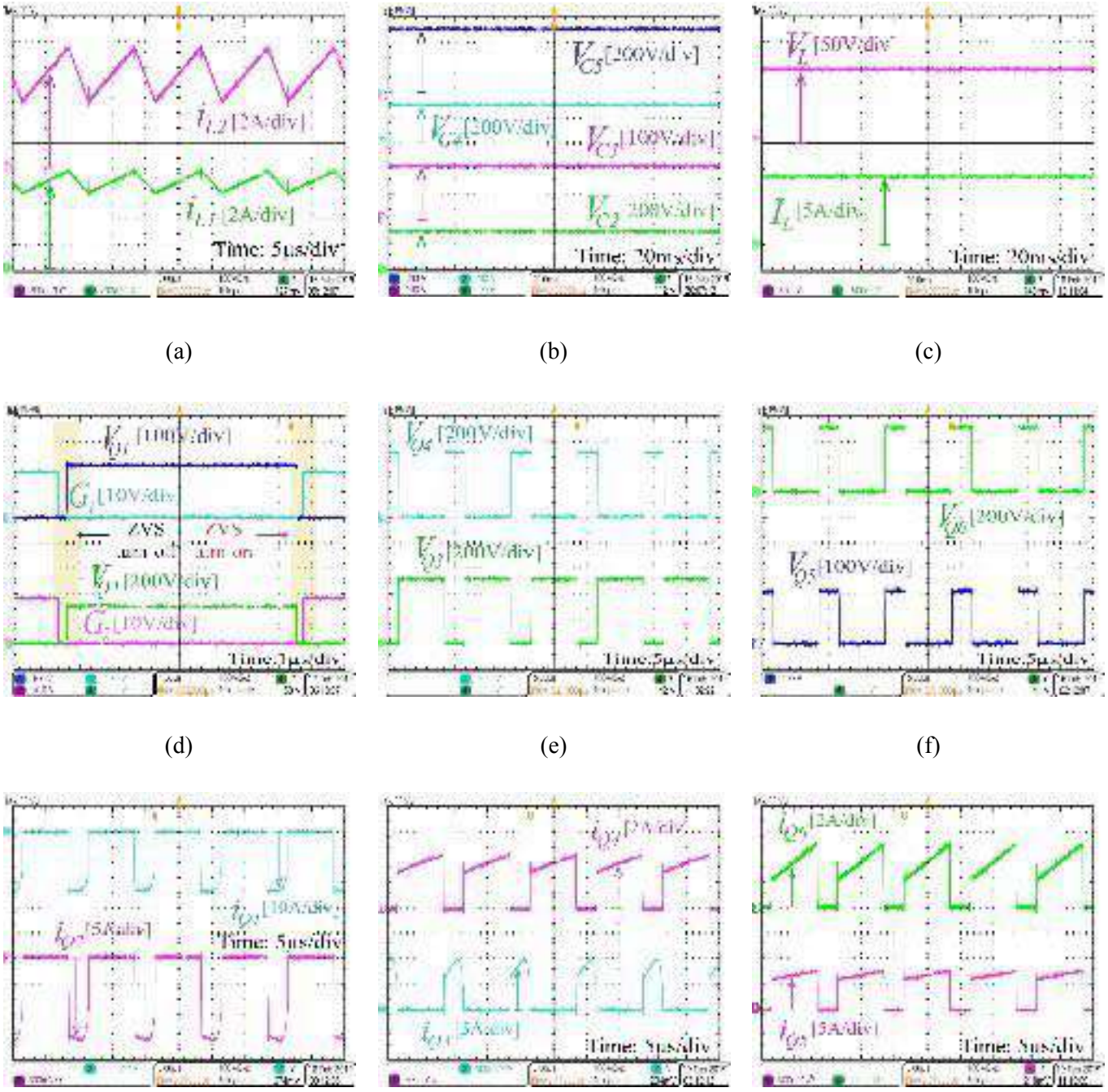
In this case study, the operation of the proposed converter is evaluated in step-down mode. The parameters of operation are as following: V_H = 800V, d_2 = 0.7, and the load connected to the LV port is represented by a resistor of 10.5Ω.

The voltage across the capacitors of the converter can be deduced using (10)-(12), the voltage at the LV port of the converter and the step-down voltage gain in this case study can be calculated using (13) and (14), respectively, as following: $V_{C2} = V_{C4} \approx 296.3$V, $V_{C3} \approx 207.4$V, $V_{C5} \approx 503.7$V, $V_L \approx 145.19$V, and $M_{Buck} \approx 0.18$, which closely agree with the experimental results in Figure 9.13(b) and Figure 9.13(c).

The currents and the ripple currents of L_1 and L_2 can be calculated using (21), (22), and (28), as follows: $I_{L1} \approx 6.6$A, $I_{L2} \approx 7.14$A, $\Delta i_{L1} \approx 1.74$A, and $\Delta i_{L2} \approx 4.23$A. These values are in close agreement with the results in Figure 9.13(a). The voltage stress across the six switches can be calculated by means of (15)-(17), as follows: $V_{Q1} = V_{Q5} \approx 207.4$V, $V_{Q2} \approx 296.3$V, $V_{Q3} = V_{Q4} = V_{Q6} \approx 503.7$V.

The experimental results in Figure 9.13(d), Figure 9.13(e), and Figure 9.13(f) confirm the correctness of the calculated values. The current stresses of the six switches can be calculated by (23)-(27), as: $i_{Q1} \approx 22.1$A, $i_{Q2} \approx 15.48$A, $i_{Q3} \approx 8.33$A, $i_{Q4} = i_{Q6} \approx 3.57$A, and $i_{Q5} \approx 6.63$A, which closely agree with the results in Figure 9.13(g), Figure 9.13(h), and Figure 9.13(i).

In this case study, Q_1 and Q_2 act as synchronous rectifiers, hence, when a time delay is applied to their gate pulses, ZVS can be realized at the turn on and turn off transitions, which is confirmed by Figure 9.13(d).



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Figure 9.12: Experimental results of case study II

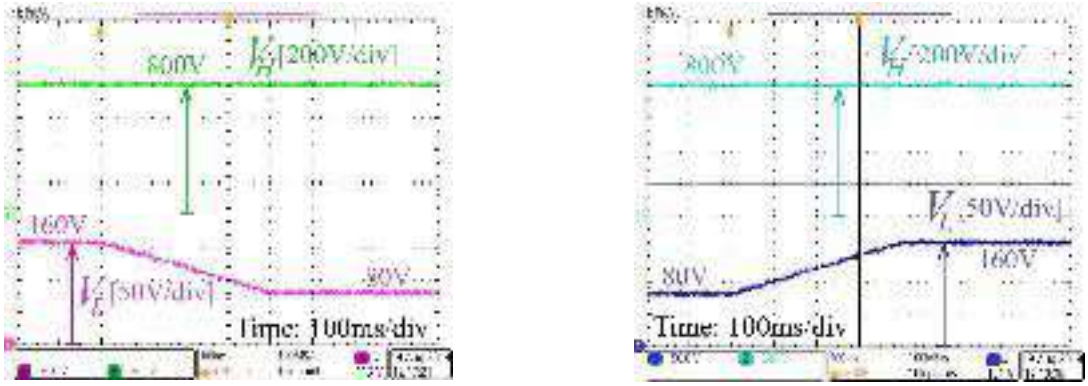
9.6.3 Dynamic Performance with Wide-Voltage-Gain Operation

To evaluate the capability of the proposed converter to operate successfully with wide voltage gain, two tests have been conducted. The first test is for the step-up operation, while the second test is for the step-down operation. Two closed-loop Type-III voltage controllers are utilized to control the voltage at the LV and HV ports during the step-down and step-up operations, respectively. In the first test, the load is connected to the HV port, and a programmable dc power supply is connected to the LV port, as V_L is changed gradually from 160V down to 80V and the closed-loop voltage controller holds V_H constant at 800V, as shown in Figure 9.14(a). In the second test, the load is connected to the LV port, and a dc power supply is connected to the HV port, as V_H is fixed at 800V and the closed-loop voltage controller gradually changes V_L from 80V up to 160V, as shown in Figure 9.14(b). The results of these two tests confirm the acceptable performance of the proposed converter to operate stably under wide voltage gain range.

Figure 9.15 shows the dynamic performance of the proposed converter under sudden changes in the load. In the first test, the LV port is connected to an 80V power supply and the closed-loop voltage controller holds the voltage of the HV port at 800V while the load connected to the HV port has step-changed from 640Ω to 320Ω, as shown in Figure 9.15(a). In the second test, the HV port is connected to an 800V power supply and the closed-loop voltage controller holds the voltage of the LV port at 80V while the load connected to the LV port has step-changed from 3.5Ω to 7Ω, as shown in Figure 9.15(b). The results of both tests prove that the converter with the utilized closed-loop voltage controllers has a good dynamic performance under sudden load changes.

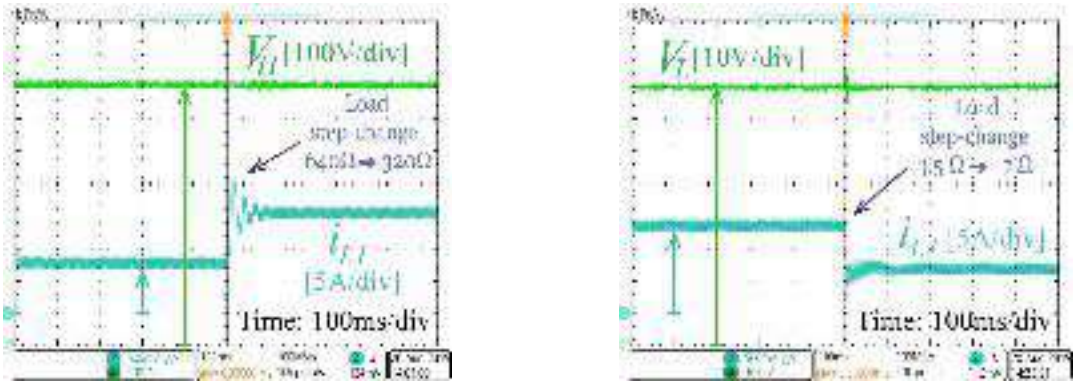
In order to gradually build up the voltage on the capacitors of the converter and avoid high inrush currents during the starting instant, a soft-starting algorithm has been adopted. This

algorithm is based on gradually increasing the value of the duty cycle from zero to the desired reference value during the starting transition.



(a) (b)

Figure 9.13: Performance of the proposed converter under wide-range of voltage gain (VH = 800V, VL = 80V→160V, and Po = 2kW). (a) Step-up mode. (b) Step-down mode.



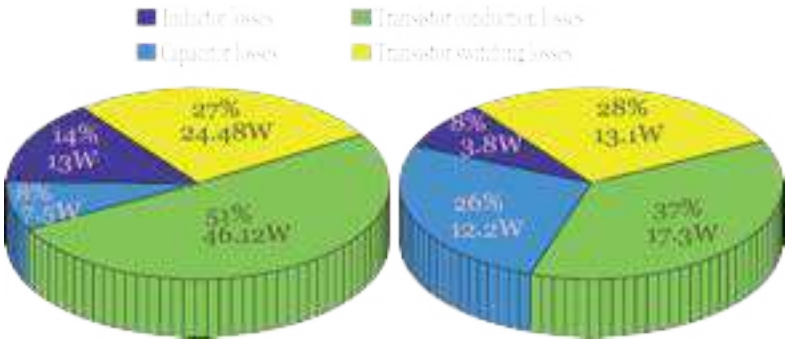
(a) (b)

Figure 9.14: Dynamic performance of the proposed converter under abrupt change in load. (a) Step-up mode. (b) Step-down mode.

9.7 Efficiency Analysis

Figure 9.16 shows the calculated loss distributions for case study I and case study II. In case study I, the calculated efficiency of the converter is 95.6% with total losses of 91.1W. The conduction and switching losses of the transistors, and the conduction losses of the inductors and capacitors account for 51%, 27%, 14%, and 8%, respectively, of the total losses of the converter,

as shown in Figure 9.16(a). In case study II, the calculated efficiency of the converter is 97.7% with total losses of 46.4W.



(a) (b)

Figure 9.15: Calculated power loss distributions for the experiment (a) Case study I. (b) Case study II.

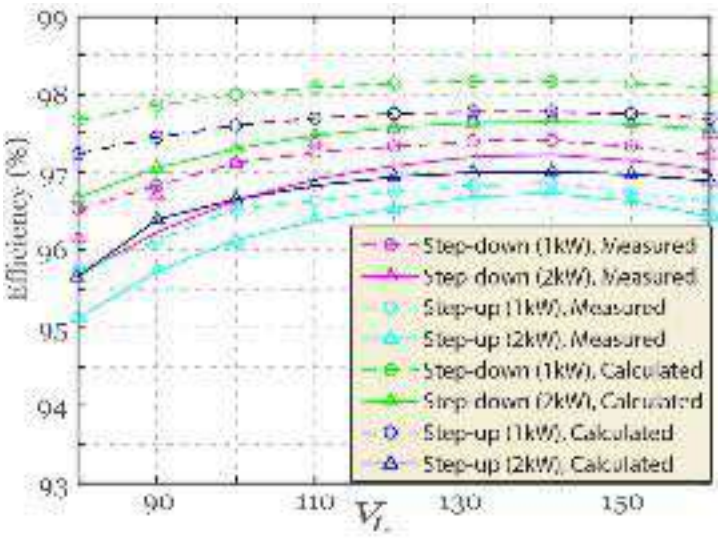


Figure 9.16: Measured efficiency curves of the proposed converter in step-up and step-down modes (VH =800V, Po =1kW, 2kW, and VL =80V→160V).

The conduction and switching losses of the transistors, and the conduction losses of the inductors and capacitors account for 37%, %, 28%, 8%, and 26%, respectively, of the total losses of the converter, as shown in Figure 9.16(b).

The measured and calculated efficiency curves in step-up and step-down modes when V_H = 800V, V_L = 80V→160V, and P_o = 1kW and 2kW, are shown in Figure 9.17. In the step-up mode, when P_o = 1kW, the minimum measured efficiency is 95.7% at V_L = 80V, and the maximum efficiency is 96.8% at V_L = 140V, while when P_o =2kW, the minimum efficiency is 95.1% at V_L = 80V, and the maximum efficiency is 96.6% at V_L = 140V. In the step-down mode, when P_o = 1kW, the minimum efficiency is 96.5% at V_L = 80V, and the maximum efficiency is 97.4% at V_L = 140V, while when P_o =2kW, the minimum efficiency is 95.7% at V_L = 80V, and the maximum efficiency is 97.2% at V_L = 140V. The high efficiency of the converter even with high voltage conversion ratios is due to the low voltage stress on the semiconductor devices, the high voltage gain of the converter, hence, high voltage conversion ratios can be obtained at moderate values of duty cycle, and the utilization of SiC MOSFETs in the prototype.

9.8 Conclusion

A new bidirectional dc-dc converter based on a hybrid structure of the quadratic converter with an integrated switched capacitor network has been proposed and analyzed in this chapter. The proposed topology has high voltage conversion ratios, high semiconductor utilization factor, and constant potential difference between the grounds of its ports. These features allow the converter to operate efficiently at high voltage gains without the need to operate at extreme values of duty cycle values, which make the presented topology an excellent interface for electric vehicles' energy storage units and the dc-link of the inverter. In addition, an extended version of the proposed converter has been discussed in order to enhance further the voltage gain of converter and reduce the voltage stress on its individual switches.

Chapter 10 Cascaded High Frequency AC-Link Systems with Reduced Switch Count for Large-Scale PV-Assisted EV Fast Charging Stations

10.1 Introduction

Electric vehicles are emerged as an alternative to conventional gas engine vehicles. Developing high-power fast charging stations is a promising solution to the problems of long charging time and limited range per charge [197]-[199]. In the literature, there are basically two main architectures for fast charging stations:

1) In the first architecture, there is a common LV ac-bus, where each EV charger in the fast charging station has its own dedicated ac-dc conversion stage to interface it to the ac grid [200], [201].
2) In the second architecture, the fast charging station has a common LV dc bus, where all the EV chargers are comprised of dc-dc converters, and connected to a common LV dc bus, then a central dc-ac conversion stage is utilized to interface the LV dc bus system to the ac grid [202]-[204].

The main advantage of the second architecture is the simple power electronic interface required to interface the EV chargers, renewable energy sources, or energy storage units to the LV dc bus of the charging station.

For a large-scale system, with a multi Megawatt power rating, the fast charging station needs to be directly connected to the MV ac power network. Considering the second fast charging station architecture, the topology of the central dc-ac power conversion stage can be without transformers, or using a transformer. For the topologies without transformers, the cascaded z-source inverter and the cascaded quasi z-source inverter are taking a lot of interest in the recent literature [205]-[207]. They can provide a high boosting gain and by connecting them in series they can reach the voltage

level of the MV grid without the need for a transformer. On the other hand, both the cascaded z-source inverter and cascaded quasi z-source inverter do not provide galvanic isolation between the input port, where all the EV chargers and the renewable sources are connected, and the output port where the MV ac grid is connected, moreover, they require bulky dc-link capacitors and dc-link inductors which can increase the size and decrease the reliability of the system with large number of cascaded inverters. For the transformer-based topologies, the CHF-link system is gaining a lot of interest [208]-[214] due to the development of high voltage wide-bandgap semiconductor devices that can switch efficiently at high frequencies [215], [216] and the new magnetic core materials like Nanocrystalline that have high maximum flux density and low core losses at high frequencies [217], [218].

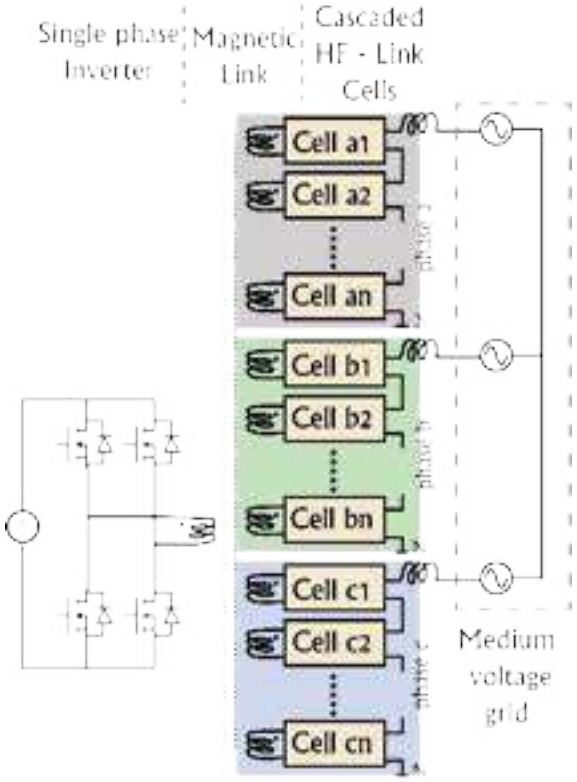


Figure 10.1:Generic Block Diagram of a CHF-link System.

The CHF-link system is a power electronic interface that interconnects a LV dc bus system with the MV ac grid and provides galvanic isolation via a MF/HF transformer. The generic block diagram of the CHF-link system is shown in Figure 10.1, where it is composed of a single phase inverter (can be multiple of parallel single phase inverters to handle more power), a HF/MF transformer with a multi-winding secondary, and cascaded HF-link cells. The single phase inverter is used to convert the LV dc input to a HF/MF voltage waveform required for the HF/MF transformer.

The transformer acts as a HF/MF magnetic link. The cell is an AC/AC power converter, and when the cells are connected in series, they convert the HF/MF voltage from the transformer secondary windings to a sinusoidal voltage with the nominal grid frequency. Different cell topologies have been proposed in literature. In [208]-[212], the authors proposed a topology for the cell that is composed of a rectifier bridge to rectify the HF voltage of the transformer, a dc-link capacitor to smooth the rectified voltage, and a single phase inverter to convert the rectified voltage to a low-frequency voltage component. This cell is a HF dc-link cell. The number of active switches in this cell topology is four switches per cell. The CHF-link system with this cell topology is called CHF dc-link system. The main disadvantage of this cell topology is the utilization of dc-link capacitors which are sizable, and with the large number of cells, the size of this system will be large, and the reliability of the system will drop down, added to this, this cell does not provide bidirectional power flow capability.

In [213] and [214], a new topology is proposed for the cell based on a matrix converter to eliminate the dc-link capacitors, and provide bidirectional power flow capability. This cell is a HF ac-link cell. The CHF-link system with this cell topology is a CHF ac-link system. The number of active switches in this cell topology is eight switches per cell which is double that needed for the

HF dc-link cell. The increased number of switches with their associated driving circuits and heat sinks increases the cost, size and weight of the CHF ac-link system.

In this chapter, two new HF ac-link cell topologies are proposed. Both of the proposed cell topologies get rid of the dc-link capacitors, provide bidirectional power flow capability, and require less number of active switches compared to the HF ac-link cell proposed in [213] and [214]. The topologies of the proposed HF ac-link cell 1 and the proposed HF ac-link cell 2 are presented and compared with the previously proposed cell architectures in literature in Table 10.1.

The proposed HF ac-link cell 1 is composed of a center-tapped transformer secondary winding connected to a two-arm half-bridge matrix converter, each arm is composed of anti-series connected IGBTs. This cell is comprised of four active switches and can only work in a bipolar operation, hence, can realize two voltage levels, either a positive voltage or a negative voltage. The proposed HF ac-link cell 2 is comprised of six switches and has the same topology of the proposed HF ac-link cell 1 with an extra third arm that connects between the output terminals of the half-bridge matrix converter. This third arm has two main advantages:

1) Provides a zero state, thus, each cell is able to work in both bipolar and unipolar operation, which results in three voltage levels that can be realized by each cell.

2) Provides a bypass across the cell in case of an open-circuit fault takes place in either the upper or lower arms of the half-bridge matrix converter, which helps to isolate the faulted cells and achieve fault tolerant operation easily.

A novel multilevel HCC is proposed to directly generate the switching signals from the reference current without the burden of closed-loop controllers used with the conventional voltage-controlled switching strategies [219]. The proposed multilevel HCC provides a simple and powerful switching strategy that utilizes the slope of the error between the reference current and

the actual phase current to select the adequate voltage level to be realized in order to reduce the magnitude of this error. Moreover, the proposed multilevel HCC provides natural commutation, which eliminates the need for clamping circuits usually used with matrix converters like in [214]. The PV-assisted fast charging station presented in this chapter utilizes a bidirectional power flow controller that injects the excess in the generated power from the PV system to the grid, and withdraws power from the grid to the LV-dc bus system inside the station when the demand of the EV chargers exceeds the generated PV power. The changing power flow levels between the fast charging station and the MV ac grid can cause severe voltage fluctuations at the point of common coupling (*PCC*), considering a realistic weak grid. In literature, there are commonly two approaches to damp and eliminate these voltage fluctuations. The first approach utilizes energy storage systems (ESSs) like the batteries, ultra-capacitors and flywheels to smoothen the transitions between different power flow levels [220]-[222]. This approach utilizes the ESSs to manipulate the active power injected to/from the *PCC* in order to smooth out the abrupt changes in the power flow levels. The second approach manipulates the reactive power injected to the grid to damp any voltage fluctuations at the *PCC* [226]. The second approach is superior over the first one for large-scale applications, with multi-Megawatt rating, since it eliminates the need for large ESSs. The second approach is adopted in the control scheme of the proposed PV-assisted fast charging station to hold the voltage at the *PCC*, V_{PCC}, constant.

With the increasing penetration of distributed generators into the power grids, the grid codes require these sources to remain grid-connected during grid disturbances to ride-through the faults by supplying the grid with active/reactive power to assist the voltage recovery and enhance the grid stability [223]-[228]. This Low-Voltage Ride-Though (LVRT) capability is adopted in the control scheme of the proposed PV-assisted fast charging station to support the grid with the

necessary reactive power in order to meet the grid code requirements during voltage sags.

10.2 Proposed Architecture of the PV-Assisted Fast Charging Station

10.2.1 Basic Block Diagram of the Proposed CHF ac-link Systems

Figures 10.2(a) and 10.2(b) show the architecture of the PV-assisted fast charging station with the proposed HF ac-link cell 1 and the proposed HF ac-link cell 2, respectively. The fast charging station has a LV dc bus where both the EV chargers and the PV system are connected to. A single phase inverter is used to convert the dc voltage of the LV dc bus system to the HF/MF voltage required by the HF/MF transformer. Multiple single phase inverters can be connected in parallel to handle high power levels. The transformer acts as a HF/MF magnetic link that steps-up the voltage level of the LV dc bus system, which has a voltage of VDC, and provides a galvanic isolation between the LV dc bus of the fast charging station and the MV ac grid. The secondary windings of the transformer are connected to the AC/AC power conversion stages, in the form of cells connected in series to realize high voltage levels with the voltage stress on the switches held at an acceptable level. Table 10.1 shows the architectures of the cells that have been proposed in literature and compares their features and operational modes with the proposed HF ac-link cells 1 and 2. Both of the proposed cell topologies get rid of the dc-link capacitors, hence, the CHF-link system that utilizes any of them can be considered as a CHF ac-link system. The number of the transformer secondary windings is 2n for n cells. Each half-bridge matrix converter is connected to two transformer secondary windings as depicted in figures 10.2(a) and 10.2(b). The transformer turns ratio between the primary winding and one of the secondary windings is 1: *m*.

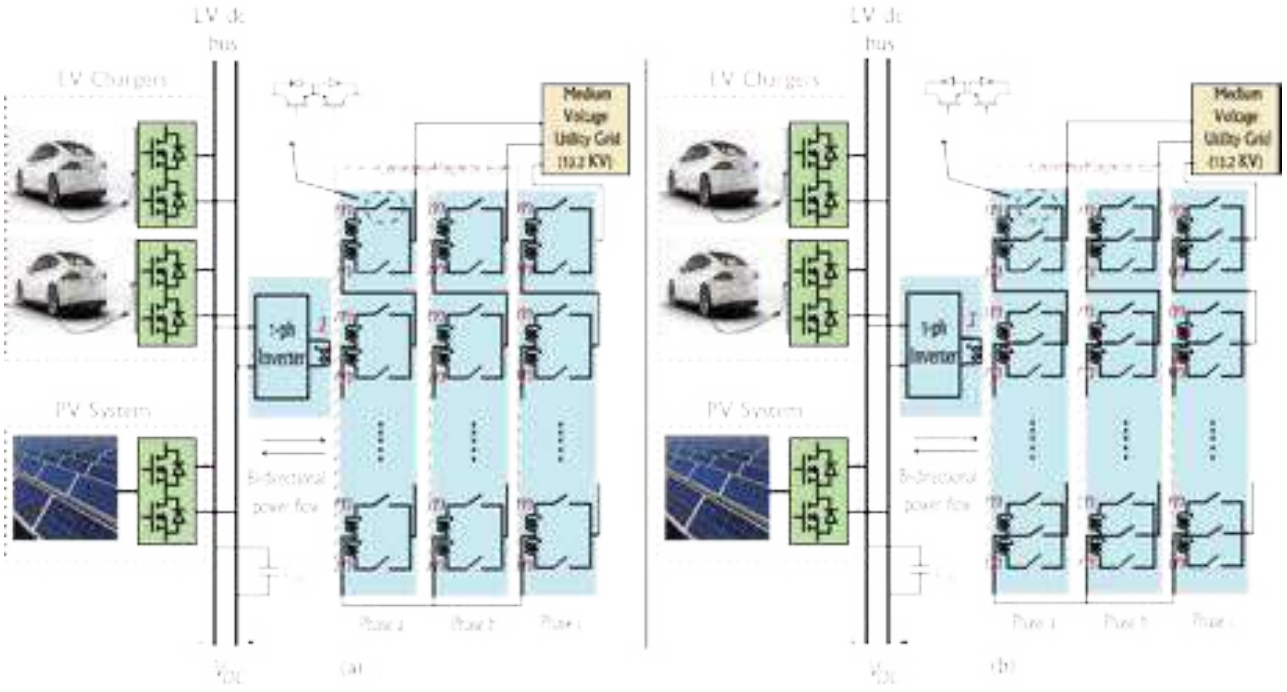
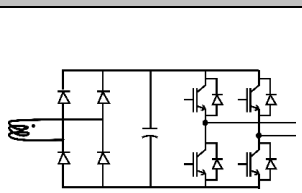
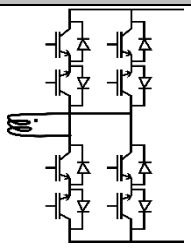
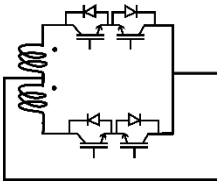
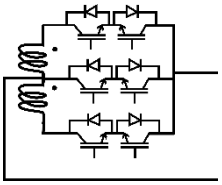


Figure 10.2: (a) The proposed PV-assisted fast charging station with the CHF ac-link cell 1. (b) The proposed PV-assisted fast charging station with the CHF ac-link cell 2.

The reference value for V_{DC} is held constant via the bidirectional power flow controller, as discussed in the next subsections. When the single phase inverter works with a duty cycle of 50%, the voltage at the transformer primary side will be $-V_{DC}$ for 50% of the periodic time and V_{DC} for the rest of the periodic time. The voltage at one of the transformer secondary windings is $(-m.V_{DC})$ for half of the periodic time and $(m.V_{DC})$ for the rest of the periodic time.

For the CHF-link system with the proposed HF ac-link cell 1, each cell works only in a bipolar operation, thus each cell can output either $(m.V_{DC})$ or $(-m.V_{DC})$. On the other hand, the CHF-link system with the proposed HF ac-link cell 2, each cell can work in a unipolar operation, hence, each cell can realize three voltage levels, $(m.V_{DC})$, $(-m.V_{DC})$, or 0. By controlling the time of realization of these voltage levels, as discussed in the next subsections, the cell can convert the HF/MF voltage to a low-frequency voltage component.

Table 10.1: CHF-LINK SYSTEM CELLS, THEIR FEATURES AND OPERATIONAL MODES

Cell Type	HF dc-link Cell in [208]-[212]	HF ac-link Cell in [213], [214]	Proposed HF ac-link Cell 1	Proposed HF ac-link Cell 2
Schematic Diagram				
Number of levels/cell	3	3	2	3
Number of active switches/cell	4	8	4	6
Number of levels/phase (for *n* cells/phase)	$2n+1$	$2n+1$	$n+1$	$2n+1$
Unipolar Operation	Yes	Yes	No	Yes
Bipolar Operation	Yes	Yes	Yes	Yes
DC Link Capacitor(s)	Yes	No	No	No
Bidirectional power flow capability	No	Yes	Yes	Yes

10.2.2 Analysis of the CHF-Link System with the Proposed HF ac-link Cell 1

As discussed earlier, each cell can convert the transformer secondary winding voltage to either ($m.V_{DC}$) or ($-m.V_{DC}$). The output voltage of a cell_{ij}, where j and i are the cell number and the phase, respectively, can be represented as

$$V_{ij} = K_{ij} \,.\, (Q.m.V_{DC}) \tag{1}$$

$$\text{Or} \quad V_{ij} = H_{ij}.m.V_{DC} \tag{2}$$

Where V_{ij} is the output voltage of cell_{ij}, K_{ij} is the switching state of the cell which is either 1 or -1, Q is the switching state of the single phase inverter connected to the transformer primary winding and it can be either 1 or -1. Here, H_{ij} is equal to $K_{ij}.Q$, which represents the desired output state from cell_{ij}.

From (1), phase *i* voltage can be described as:

$$V_i = \sum_{j=1}^{n} V_{ij} \tag{3}$$

Where *n* is the total number of cells per phase.

The number of cells of phase *i* with H_{ij} equal to 1 is P_i, and N_i is the number of cells of phase *i* with H_{ij} equal to -1, where

$$P_i + N_i = n \tag{4}$$

Substituting (3) in (4),

$$V_i = (P_i - N_i).m.V_{DC} \tag{5}$$

From (5), by changing P_i and N_i, the realized phase voltage can be controlled, and thus, for *n* cells/phase, the number of phase voltage levels are *n* + 1.

10.2.3 Analysis of the CHF-Link System with the Proposed HF ac-link Cell 2

The proposed HF ac-link cell 2 can realize three voltage levels, ($m.V_{DC}$), ($-m.V_{DC}$), or 0. The output voltage of $cell_{ij}$, V_{ij}, can be described by equations (1) and (2), where K_{ij}, and H_{ij}, can be 1, -1, or 0. The total phase voltage for leg *i* can be described by (3) and (5). As long as each cell can realize three voltage levels, the total number of cells per phase can be depicted by (6)

$$P_i + N_i + Z_i = n \tag{6}$$

Where Z_i is the number of cells of phase *i* with H_{ij} equals to 0. By adequately adjusting P_i, Z_i, and N_i, the realized phase voltage can be controlled, hence, for *n* cells/phase, the number of phase voltage levels that can be realized is 2*n* + 1.

10.3 The Proposed Control Strategy and LVRT Capability of the System

10.3.1 A Simplified Multilevel Hysteresis Current Controller

The proposed simplified multilevel HCC is composed of three stages, namely: level selector, cell selector, and switching logic, as shown in Figure 10.3. The proposed multilevel HCC switching strategy starts by calculating the error, e, between the reference current i_a^* and the actual current, i_a, (phase a is taken as an example). An error sample at instant *k*, *e(k)*, and a delayed error sample, *e(k-1)*, are fed to the level selector which selects the adequate voltage level that should be realized to minimize *e(k)*. After the level selector determines the reference voltage level, the cell selector determines the desired output state from each cell, H_{a1}, H_{a2}, …, H_{an}, to realize the desired voltage level. Each of these states takes a value of 1, -1, or 0, in case of the proposed HF ac-link cell 2, while for the proposed HF ac-link cell 1, each state can be 1, or -1. The desired output states of the cells are then fed to the switching logic block. In addition, the polarity of i_a, r_a, and the switching state of the single phase inverter connected to the HF transformer primary winding, *Q*, are fed to the switching logic block. The switching logic generates the switching signals for the switches of each cell. Similar multilevel HCC to that shown in Figure 10.3 for phase *a* are used for phases *b* and *c*. The sampling time of the error, T_s, determines the maximum switching frequency as shown in (7).

$$\text{Maximum frequency} = \frac{1}{2 \text{ X } T_s} \tag{7}$$

Figure 10.4 illustrates the algorithm of the level selector. It starts by calculating the positive band level, *PB*, the negative band level, *NB*, and the slope of the error, *de(k)* as in (8), (9) and (10).

$$PB = \text{ error tolerance} \tag{8}$$

$$NB = \text{- error tolerance} \tag{9}$$

$$de(k) = e(k) - e(k\text{-}1) \tag{10}$$

When *e(k)* is less than NB and slope of the error is negative, this means the actual current has to be reduced and the present voltage level is not adequate to achieve that, so, the voltage level reference is decremented. When *e(k)* is greater than PB and the slope of the error is positive, this means the actual current has to be increased by increasing the voltage level reference. Otherwise, the voltage level reference is kept the same without any change.

For the proposed HF ac-link cell2, the switching logic block is fed by the desired output states for each cell, the current polarity and the single-phase inverter switching state to generate the switching signals of the switches of each cell. The *Q* signal is used to determine whether the voltage at the transformer secondary winding is ($m.V_{DC}$) or ($-m.V_{DC}$). The desired output state, H_{ij}, is used to determine whether the cell needs to output ($m.V_{DC}$), ($-m.V_{DC}$), or 0. The current polarity signal of phase *i*, r_i, is used to determine whether the cell is working in a current conduction mode or in current natural commutation mode.

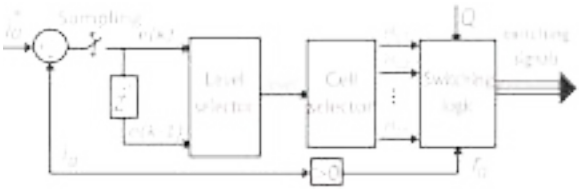


Figure 10.3: The proposed multilevel HCC for phase a.

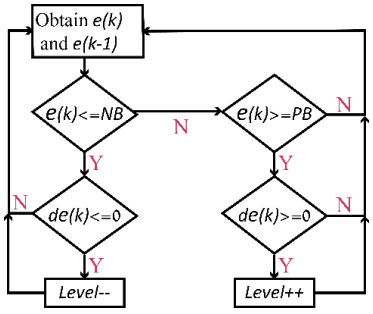


Figure 10.4: The flowchart of the level selector algorithm.

Figure 10.5: Design example of CHF ac-link with two cells per phase.

Level 1	-1	-1	$-2m.V_{DC}$
Level 3	-1	1	0
	1	-1	
Level 5	1	1	$2m.V_{DC}$

Figure 10.5 shows a design example of CHF ac-link system (with the proposed HF ac-link cell 2), where each cell can produce either (*m.*
in Figure 10.5 shows the different voltage levels that can be realized by this system, where five voltage levels can be realized between the term
Adjusting the desired output states of the two cells (H_{a1} and H_{a2}) is used to realize a certain voltage level, as shown by equations (2) and (3). As an example, voltage level 2 ($V_{AN} = -m.V_{DC}$) can be realized by ($H_{a1} = -1$ and $H_{a2} = 0$) or by ($H_{a1} = 0$ and $H_{a2} = -1$).

In Figure 10.7, ten modes of operation for the proposed HF ac-link cell 2 are shown. The value of Q is reflected on the polarity of the voltage at the transformer secondary winding, where ($m.V_{DC}$) appears when Q = 1, as depicted in modes 1-4, and ($–m.V_{DC}$) appears when Q = 0, as in modes 5-8. Modes 9 and 10 are dedicated for the zero state of the cell, where the value of Q is neglected and the phase current polarity, r_a, is used to determine which switch of the middle arm to turn on.

The investigated cell in Figure 10.7 has three arms, each arm is composed of two anti-series IGBTs to provide four-quadrant-operation, the middle arm is dedicated to provide the zero state of the cell, while the other two arms are used to realize either ($m.V_{DC}$) or ($–m.V_{DC}$). The middle arm has switches S_{5a}, and S_{6a}, the upper arm has switches S_{1a}, and S_{2a}, and the lower arm has switches S_{3a}, and S_{4a}.

Table 10.2: THE SWITCHING MODES FOR CELL J IN PHASE A FOR THE PROPOSED HF AC-LINK CELL 2

Mode	Q	H_{aj}	r_a	Switching signals					
				S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{5a}	S_{6a}
1	1	1	1	1	0	0	0	0	0
2	1	1	0	0	1	0	0	0	0
3	1	-1	1	0	0	1	0	0	0
4	1	-1	0	0	0	0	1	0	0
5	0	1	1	0	0	1	0	0	0
6	0	1	0	0	0	0	1	0	0
7	0	-1	1	1	0	0	0	0	0
8	0	-1	0	0	1	0	0	0	0
9	x	0	1	0	0	0	0	1	0
10	x	0	0	0	0	0	0	0	1

The switching logic is depicted in Table 10.2, as it shows the switching modes for cell j in phase a of a CHF ac-link system with the proposed HF ac-link cell 2, where $r_a = 1$ when $i_a>0$ and $r_a = 0$ otherwise. The shaded rows in Table 10.2 are the modes dedicated to provide natural commutation for the matrix converter, where a path is provided to the phase current to sink to the positive power rail of the transformer secondary winding. This natural current commutation technique eliminates the need for clamp circuits, usually used with matrix converters [214].

For the proposed HF ac-link cell1, the switching logic is the same except it has eight modes of operation, modes 1-8. Modes 9 and 10 are excluded as the middle arm is absent.

10.3.2 Operation under Normal Conditions

As shown in Figure 10.6, the proposed fast charging station has a dc bus, where all the EV chargers and the PV system are connected to. The EV chargers withdraw their need of power, from

the dc bus system. A large PV system is connected to the dc bus system to supply the Megawatt fast charging station with power, in order to decrease the dependency on the main power grid. The power processing unit of the PV system has a Maximum Power Point Tracker (MPPT) which determines the optimal operating points on the PV system characteristic curves in order to extract the maximum power from the PV arrays. Figure 10.6 shows a single line diagram of the proposed PV-assisted fast charging station, where P_{EV} is the withdrawn power from the dc bus system by the EV chargers, and P_{PV} is the injected PV power to the dc bus system. A bidirectional power flow controller is needed to inject the generated power from the PV system that exceeds the demand of the EV chargers to the grid, and withdraw power from the grid to the dc bus system when the EV chargers demand exceeds the generated PV power. By applying a closed-loop controller to set the voltage across the dc-bus capacitor, C_{dc}, V_{DC}, at a reference level, V_{DC}^{*}. This is achieved by a Proportional Integral (PI) controller, which compares V_{DC}^{*} with V_{DC}. The manipulated variable of this PI controller is the reference direct current component, i_{d}^{*}. According to (11), when the direct current component of the three phase currents flowing between the fast charging station and the grid, i_d, is positive, the station injects power to the MV ac grid, and when i_d is negative, the station withdraws power from the grid.

$$P_{PCC} = \frac{3}{2} V_{PCC} X i_d \tag{11}$$

Where V_{PCC} is the voltage at the *PCC*, and P_{PCC} is the active power flowing through the *PCC*, and it equals the difference between P_{PV}, P_{EV}, and losses in the fast charging station converters and feeders.

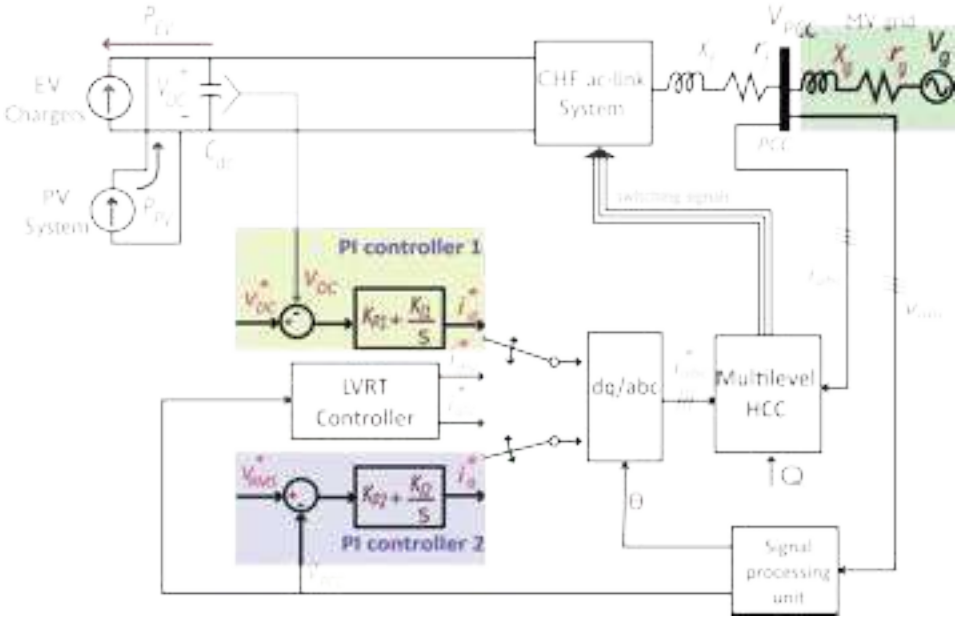


Figure 10.6: Single line diagram of the proposed PV-assisted EV charging station and its control scheme in normal operation and during grid faults.

With the changing levels of P_{PCC} between the fast charging station and the grid, and considering a week grid, with high grid equivalent impedance, noticeable fluctuations will appear in V_{PCC}, which can harm any loads connected at the *PCC*. Figure 10.8(a) shows a phasor diagram of the system presented in Figure 10.6 at two different power levels. Both I_1 and I_2 represent the RMS phase current flowing through the *PCC* at two power flow levels, and the operation in both cases is done at unity power factor, where the phase current is aligned with V_{PCC}.

For the first case in Figure 10.8(a), I_1 is flowing through the *PCC*, the component ($I_1 r_g$) represents the voltage drop through the resistive part of the grid equivalent impedance, r_g,, and it is parallel to I_1 in the phasor diagram. The component ($I_1 x_g$) represents the voltage across the reactive component of the grid equivalent impedance, x_g, and it is perpendicular on the I_1 vector. The voltage at the *PCC* in the first case, V_{PCC1}, equals the vector sum of the grid voltage, V_g, $I_1 r_g$, and $I_1 x_g$. For the second case, with the same vector calculations, V_{PCC2} equals the vector sum of

the grid voltage, V_g, $I_2 r_g$, and $I_2 x_g$. From these two cases shown in Figure 10.8(a), as the injected current to the grid increases, V_{PCC} decreases, which means, with different P_{PCC} levels, the system will suffer from noticeable fluctuations in V_{PCC}.

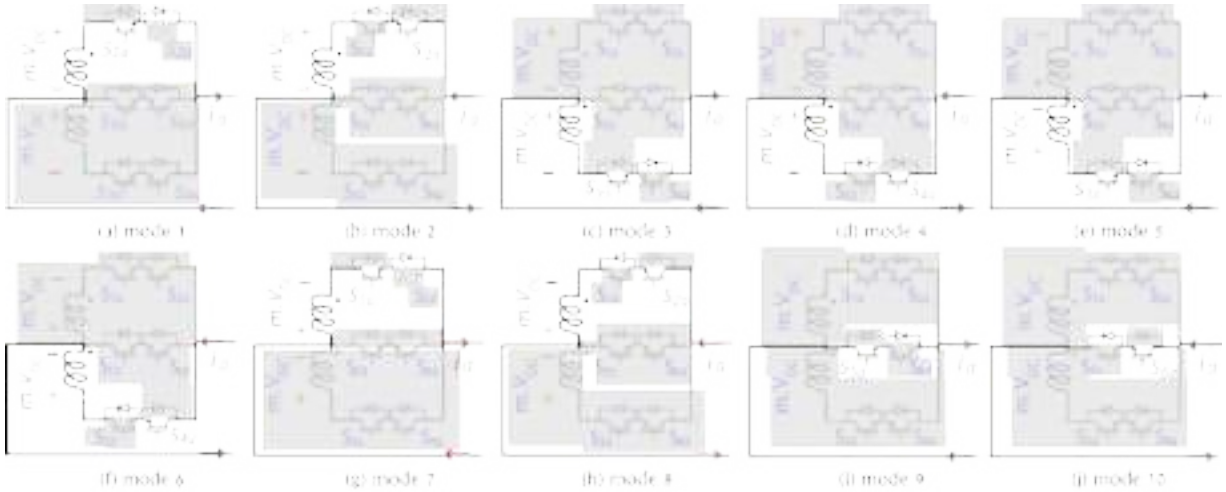


Figure 10.7: Operational modes of the proposed HF ac-link cell 2.

In Figure 10.8(b), the two cases shown in Figure 10.8(a) are reinvestigated, where the first case with I_1 flowing through the *PCC* is the same, aligned with V_{PCC1}, but in the second case, I_2 is phase-shifted from V_{PCC2}, this phase shift can be controlled and adjusted to set V_{PCC} at a reference level, V_{RMS}^*. This can be achieved by a PI controller that is fed by the error between V_{PCC} and the reference RMS voltage at the *PCC*, V_{RMS}^*, the manipulated variable of this PI controller is the reference quadrature current component of the three phase currents flowing between the fast charging station and the grid, i_q^*. Figure 10.6 shows the complete control scheme of the proposed PV-assisted fast charging station, where PI controller 1 is the closed-loop regulator dedicated for managing the bidirectional power flow between the grid and the fast charging station, and PI controller 2 is assigned for regulating V_{PCC}. After setting i_d^* and i_q^*, inverse Park and inverse Clark transformations are utilized to calculate the reference three phase currents, i_{abc}^*. The three phase

reference currents are then fed to the multilevel HCC to generate the switching signals for the switches inside the cells. The signal processing unit is used to calculate the magnitude of V_{PCC} and the instantaneous angle of $V_{PCC,}$ θ.

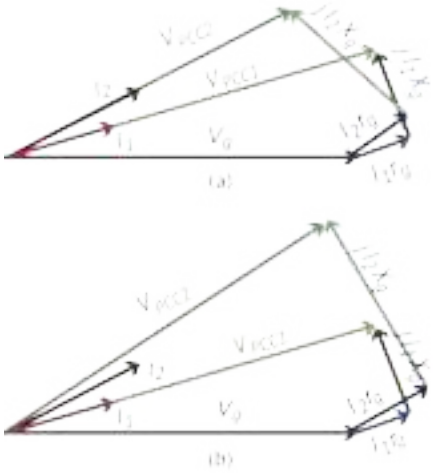


Figure 10.8: (a) Phasor diagram of the system without applying the VPCC regulator, (b) phasor diagram of the system with the VPCC regulator applied.

10.3.3 The LVRT Capability of the Proposed Fast Charging Station

The capability of the system to ride-through grid faults and disturbances is very important, and there are many grid codes that put strict requirements for grid-connected converters in order to support the grid with active and reactive power during faults. One of the popular grid codes for LVRT requirement is the E. ON code which is a German grid code and widely adopted in many literature [226]-[228]. Figure 10.9 shows the relationship between the voltage dip and the ratio between the reactive component of the injected current to the grid, and the rated current of the grid-connected converter system, according to the E. ON code. When voltage sag is detected, the LVRT controller is enabled and PI controller 2 is aborted. The LVRT controller calculates, i_{dlv}^{*} , and i_{qlv}^{*}, which are the reference direct component and the the reference quadrature component of the grid currents, respectively during the voltage sag. From Figure 10.9, the E. ON curve divides

the operation into three regions, region I is for V_{PCC} less than or equal 50% of the nominal grid voltage, and in this region the converter injects only reactive current, while in region III, V_{PCC} is close to or equal the nominal grid voltage, and in this region the LVRT controller is disabled and PI controller 1 and PI controller 2 are enabled to calculate the reference grid current components. In region II, there is a linear relationship between i_{qlv}^{*} and the percentage of V_{PCC} to the nominal grid voltage, V_{PCC}%, and this relationship is depicted in (12).

$$i_{qlv}^{*} = 2(1 - V_{PCC}\,\%) \tag{12}$$

i_{dlv}^{*} can be calculated using (13)

$$i_{dlv}^{*} = \sqrt{i_{rated}^{2} - i_{qlv}^{*2}} \tag{13}$$

Where i_{rated} is the rated current of the CHF ac-link system. In a voltage sag case, PI controller 1 sets the limit for i_{dlv}^{*} of the LVRT controller at i_{d}^{*}, as this is the maximum direct current component the system can supply. During deep voltage sag case, when i_{dlv}^{*} is less than i_{d}^{*}, PI controller 1 is aborted, and in this case the MPPT inside the power processing units of the PV system is disabled to avoid overvoltage scenarios on the LV dc bus system.

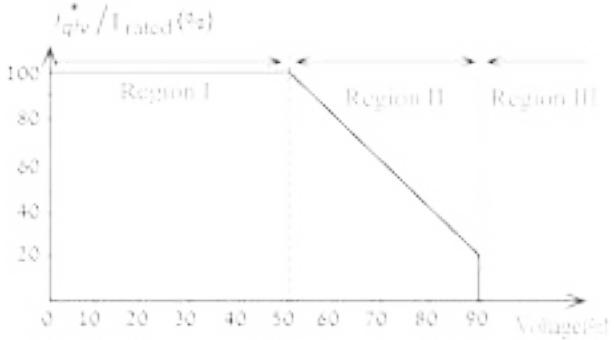


Figure 10.9: Reactive current requirement during grid fault, according to the E.ON code.

10.4 Simulation Results

Two simulation models have been built in Matlab/Simulink in order to validate the proposed

architectures of a PV-assisted fast charging station with a power rating of 6-MW, with model parameters shown in Table 10.3. The single line diagram of the simulated systems is shown in Figure 10.6, where the PV system and the EV chargers are depicted as current sources, pushing power towards the LV dc bus where C_{dc} is connected, in case of the PV system, and withdrawing power from the LV dc bus, in case of the EV chargers. The PV-assisted fast charging station is connected to a 13.2-KV grid.

Table 10.3: SIMULATION MODEL PARAMETERS

System rating	6- MW
Medium voltage grid	13.2 -KV, 60 Hz
HF transformer	2 KHz
Error Sampling frequency	30KHz
Turns ratio (m)	3.2
Grid inductance (l_g)	40 mH
Feeder inductance (l_f)	50 mH
Feeder resistance (r_f)	2 Ω
Simulation Sampling Time	$1\mu s$
PI CONTROLLER 1 COEFFICIENTS	
Proportional coefficient (K_{P1})	-10
Integral coefficient (K_{I1})	-200
PI CONTROLLER 2 COEFFICIENTS	
Proportional coefficient, (K_{P2})	-0.002
Integral coefficient (K_{I2})	-2

10.4.1 Effect of Number of Cells per Phase on the Power Quality and the Total System Cost

In this subsection, eight simulation cases are carried out. Figure 10.10 shows the three phase voltages produced by a CHF ac-link system with the proposed HF ac-link cell 1 comprising eight, six, four, and two cells per phase, and the associated total harmonic distortion, THD%, for each case is shown above its plot. The same four cases are carried out with the proposed HF ac-link cell 2 as shown in Figure 10.11. The total number of phase voltage levels that can be realized is n+1 in case of the proposed HF ac-link cell 1, where n is the number of cells per phase, and 2n+1 in case of the proposed HF ac-link cell 2. The total number of switches of the cascaded cells connected to the transformer secondary windings of a three phase CHF ac-link system is 3.n.4, in case of the proposed HF ac-link cell 1 is used, and 3.n.6, in case of the proposed HF ac-link cell 2 is used. Figure 10.12(a) shows the THD% for the four cases for both of the proposed HF ac-link cells. The total number of switches of the cascaded cells connected to the transformer secondary windings for the four cases with the proposed HF ac-link cells are shown in Figure 10.12(b). Figure 10.12 shows that as the number of cells per phase increases, the difference in THD% for the proposed two architectures is diminished, while the difference in total number of switches increases. This means for a CHF ac-link system with large number of cells, the proposed HF ac-link cell 1 is a better choice from the cost point of view.

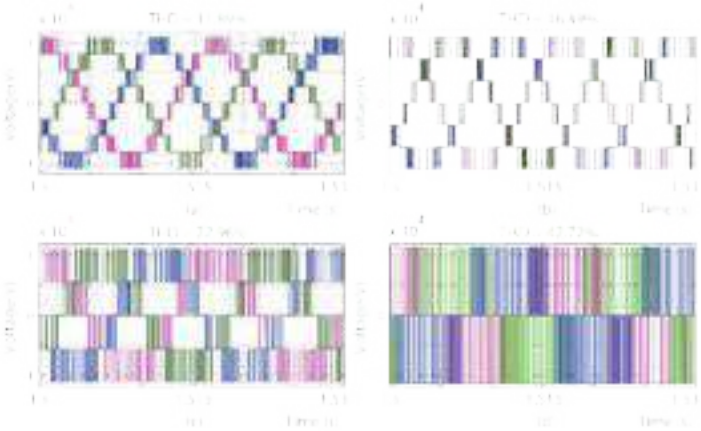


Figure 10.10: Phase voltages of the CHF-link system with the proposed HF ac-link cell 1 with (a) 8 cells, (b) 6 cells, (c) 4 cells, and (d) 2 cells per phase.

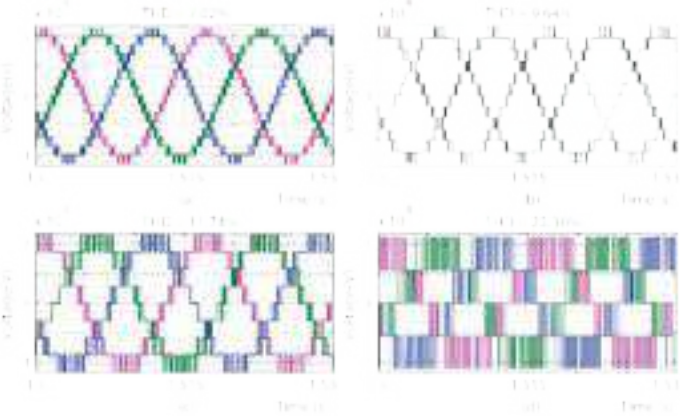


Figure 10.11: Phase voltages of the CHF-link system with the proposed HF ac-link cell 2 with (a) 8 cells, (b) 6 cells, (c) 4 cells, and (d) 2 cells per phase.

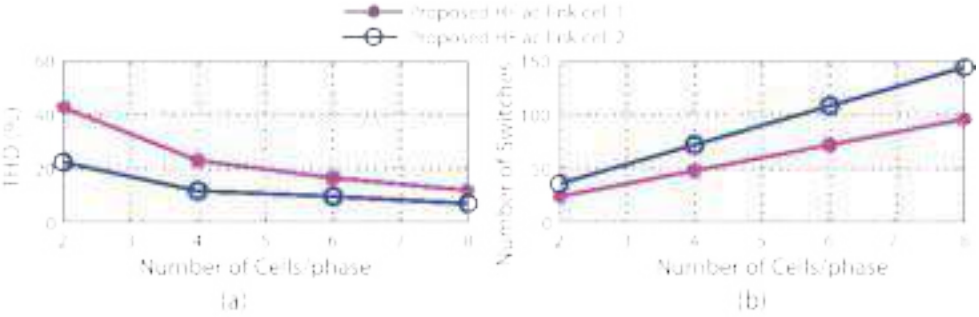


Figure 10.12: (a) THD% for different number of cells/phase with both of the proposed cells, (b) Total number of switches of the secondary side converters with different number of cells/phase with both of the proposed cells.

10.4.2 Evaluation of the bidirectional power flow controller and the PCC voltage regulator performance

The simulations in this subsection and the next subsection are carried out with a CHF ac-link system with eight cells per phase, and the proposed HF ac-link cell 1 is used.

In Figure 10.13, the dynamic performance of the bidirectional power flow controller is evaluated, as three power flow scenarios are shown. From t = 0.5 s to t = 1 s, the EV chargers withdraw 0.55 MW from the dc bus system, while the PV system injects 3.3 MW towards the dc bus system. PI controller 1 manipulates the value of i_d to hold V_{DC} at the reference level, which is set at 550V. In this case i_d = 165A, and the active power injected to the grid through the *PCC*, P_{PCC}, is 2.65 MW. From t = 1 s to t = 2 s, the EV chargers withdraw 3.3 MW from the dc bus system, while the PV system injects 1.65 MW towards the dc bus system, i_d = -104A, P_{PCC} = -1.69MW. The negative sign of P_{PCC} means that the grid is supplying the fast charging station with active power. From t = 2 s to t = 3 s, the EV chargers withdraw 4.126 MW from the dc bus system, while the PV system injects 0.55 MW towards the dc bus system, i_d = -232A, P_{PCC} = -3.75MW. Which proves the effectiveness of the bidirectional power flow controller in following up with the changing consumption of the EV chargers, and generation of the PV system. The voltage of the dc bus system is held constant with transitional overshoots less than 6%. Figure 10.15 shows the effectiveness of the V_{PCC} regulator, with the same three power flow scenarios investigated in Figure 10.13(c). Figures 10.15(c), 10.15(d), and 10.15(e) show the system response at the three power flow scenarios when PI controller 2 is disabled, while Figures 10.15(f), 10.15(g), and 10.15(h) show the system response at the three power flow scenarios when PI controller 2 is enabled. When PI controller 2 is aborted, the system is working at unity power factor, and Figures 15(a) and 15(e) show noticeable fluctuations in V_{PCC} in response to the changes in P_{PCC}, at t = 1 s, V_{PCC} goes from 7.58-KV to 7.39-KV, and at t = 2 s, V_{PCC} goes from 7.39-KV to 6.81-KV. When PI controller 2 is

enabled, the system starts injecting reactive power to the grid, as the closed-loop controller adjusts the value of i_q in order to hold the V_{PCC} at a constant level, and in this system the reference value of V_{PCC} equals 13.2kV/$\sqrt{3}$.

Figure 10.14 is an extension to the simulation case presented in Figures 10.15(f), 10.15(g), and 10.15(h), where both PI controller 1 and 2 are enabled, and it shows the response of the phase current and voltage at the *PCC* to the change in P_{PCC} at t = 1 s. For t < 1, P_{PCC} = 2.65 MW, and Q_{PCC} = 0.12 MVAR, thus the power factor = 0.37. For t > 1, P_{PCC} = -1.69MW, and Q_{PCC} = 0.32 MVAR, thus the power factor = -0.57. The change in the phase shift between the phase current and voltage at *PCC* before and after t = 1 s is shown in Figure 10.14(b).

10.4.3 Evaluation of the LVRT Capability of the System

This subsection is dedicated to test the LVRT capability of the proposed CHF ac-link system. The test scenario is composed of two faults, each fault lasts for 0.8 second, as shown in Figure 10.16. At t = 0.8s, the first fault takes place, where the grid undergoes a voltage-sag where the grid voltage, V_g, drops to 70% of its nominal value. At t = 1.6s, the second fault takes place, where the grid exhibits a voltage-sag of 50% of its nominal value. When a voltage-sag is detected, i^*_{qlv}, and i^*_{dlv} are obtained from the E. ON code graph, shown in Figure 10.9 and (13), respectively, where i_{rated} of the CHF ac-link system is set at 350A for this application.

In the first fault, the voltage sag is 70% and therefore, from Figure 10.9, i^*_{qlv} is set to 60% of i_{rated}which is equal to -210A. The negative sign indicates reactive power injection to the grid. Consequently, i^*_{dlv} is limited to 280A, according to (13). When the second fault takes place, the voltage-sag is 50%, and according to the E. ON code, i^*_{qlv} = i_{rated} = 350A, and i^*_{dlv} = 0A, respectively. As shown in Figure 10.16, when V_g drops from 7.62 KV to 5.33KV, i^*_q is boosted to -210A, and as a result, V_{PCC} is alleviated at 7.14KV which is close to the reference value. At t =

s, when the second fault takes place and V_g dips to 3.81KV, i_q^* is increased to celling level of the CHF ac-link system, as a result, V_{PCC} alleviated to 7.48KV. These results prove explicitly the capability of the LVRT controller to effectively support the voltage at the *PCC* during voltage sags.

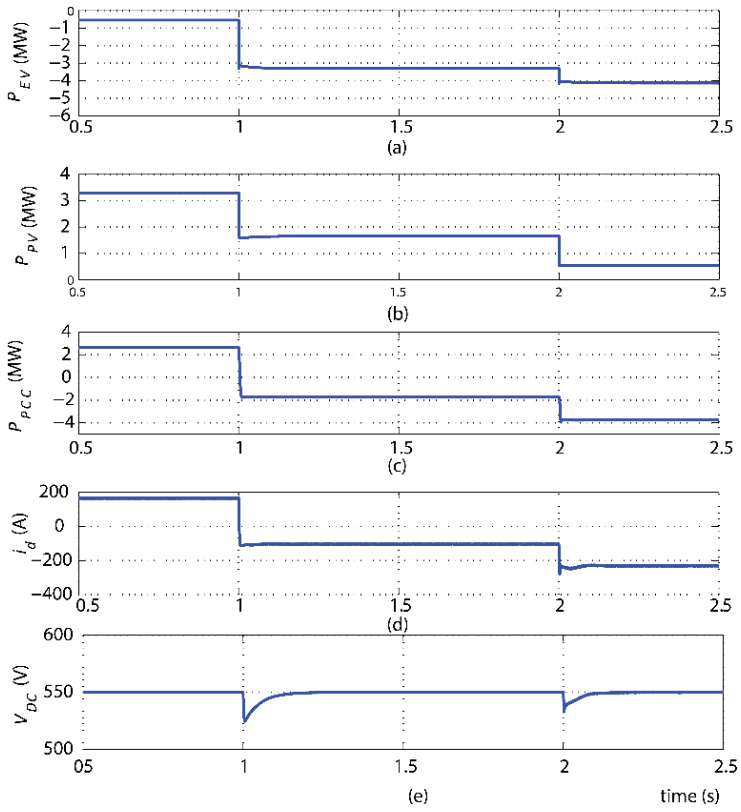


Figure 10.13: Dynamic performance of the bidirectional power flow controller.

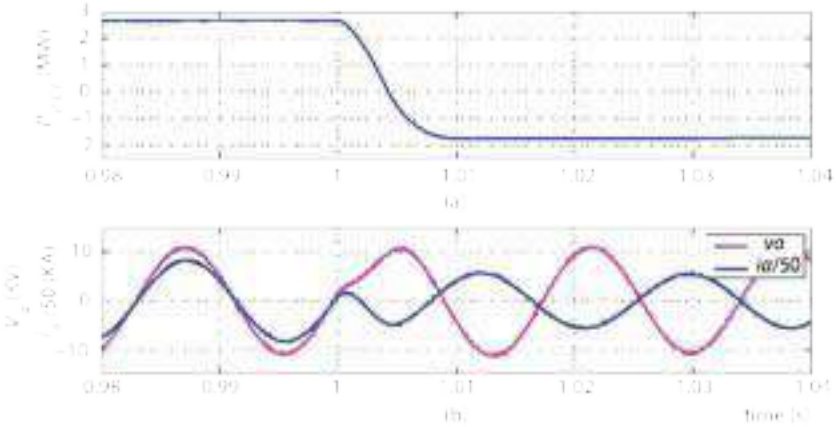


Figure 10.14: System response at two power flow levels (a) Power flow through the PCC, (b) Phase a voltage at PCC, and phase a current.

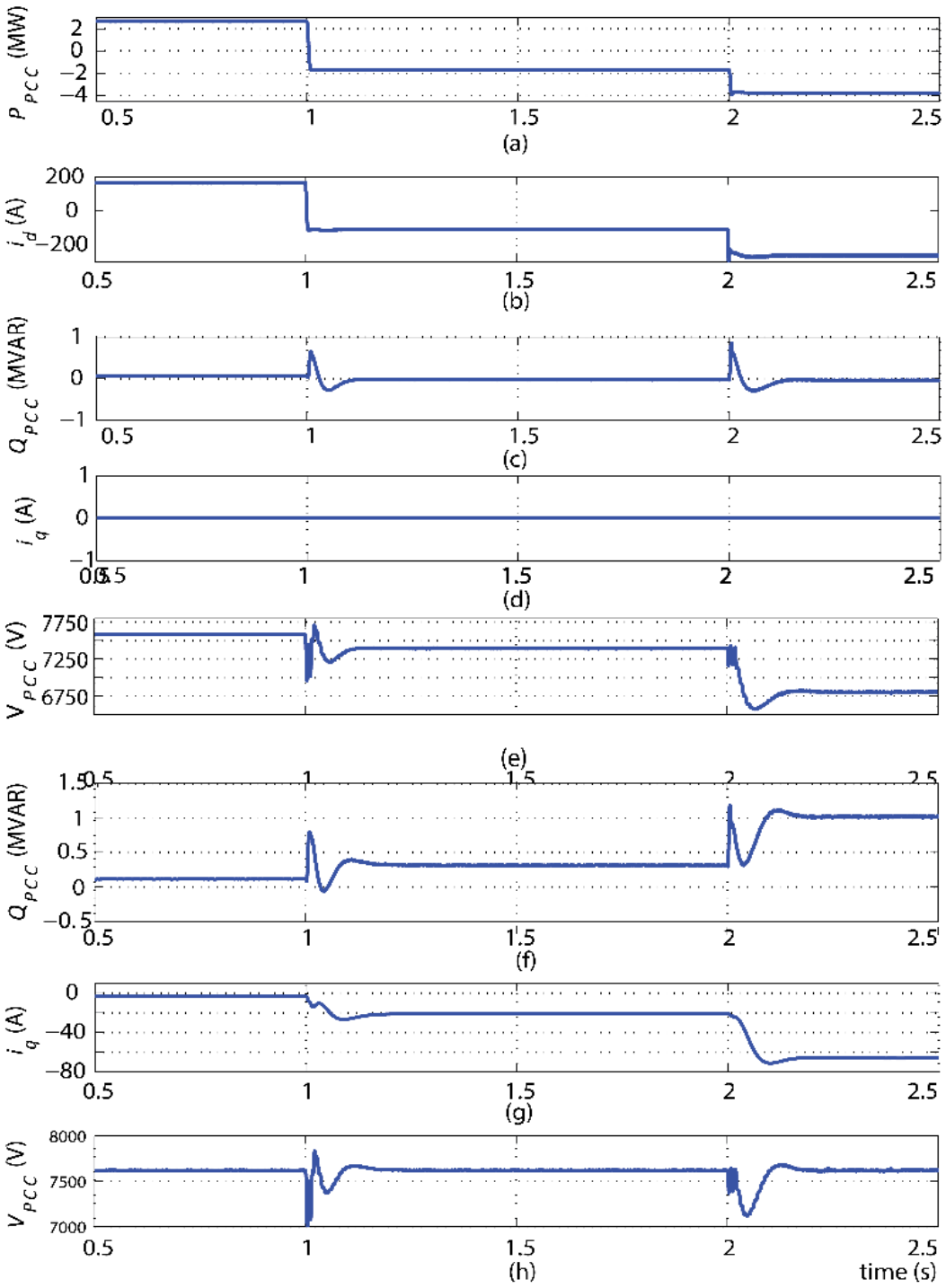


Figure 10.15: Dynamic performance of the PCC voltage regulator.

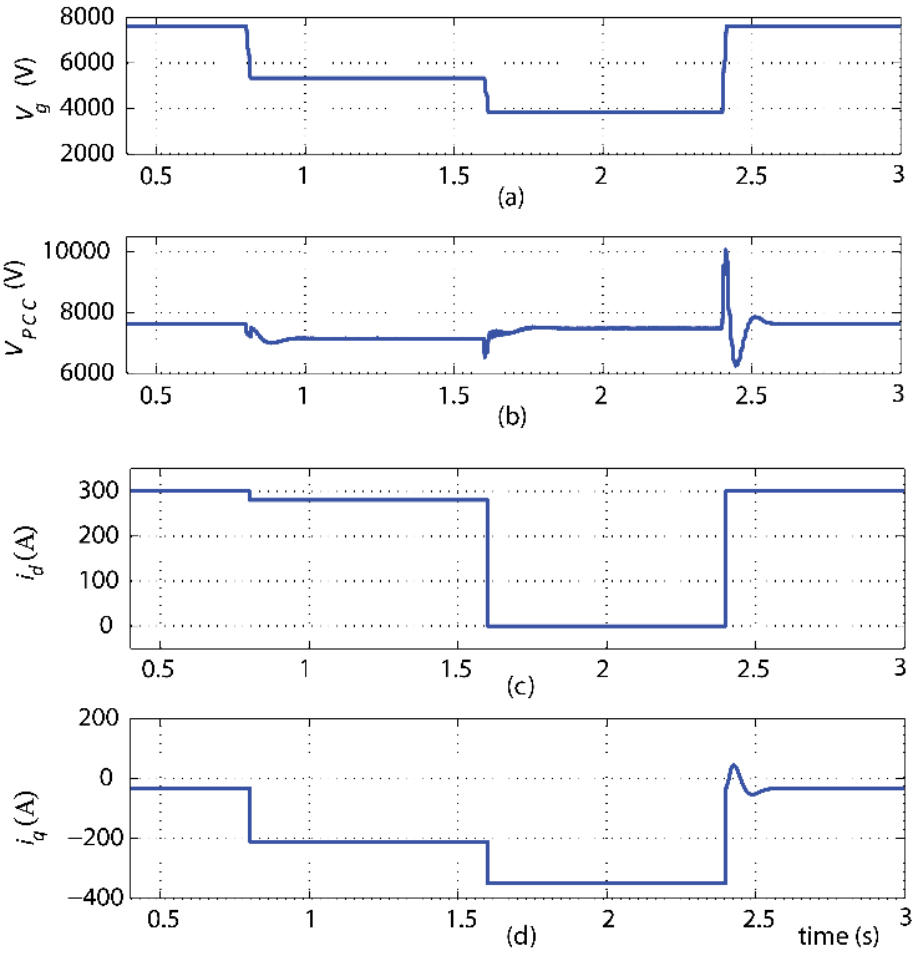


Figure 10.16: Evaluation of the LVRT capability of the proposed CHF ac-link system.

10.5 Conclusion

This chapter presented two new isolated power electronic architectures for a large-scale EV fast charging station assisted by a PV system. The proposed systems require less switches compared to other systems presented in the recent literature. A novel simplified current controller for the system was presented, which eliminates the need for the clamping circuits usually used with matrix converters. A bidirectional power flow controller was used to maximize the extracted power from the PV system without using energy storage systems. Moreover, the developed controller utilizes reactive power to compensate for the fluctuations in the voltage at *PCC* under changing power flow levels between the grid and the fast charging station. A LVRT controller was adopted to inject

the adequate active and/or reactive power levels to the grid, to keep the charging station grid-connected during faults to support the grid voltage. An example of a 6-MW system model showed the superior features of the developed system in controlling the power flow between the fast charging station and the medium-voltage ac grid. This was accomplished with high power quality during normal operation in addition to supporting the grid voltage during grid faults and disturbances by utilizing the reactive power. This which eliminates the need for large energy storage systems, commonly used to alleviate voltage sags.

Chapter 11 An Integrated PEBB using e-GaN FETs and Nanocrystalline Inductors for Multiple DC-DC, AC-DC and DC-AC Applications

11.1 Introduction

The concept of the power electronic building block (PEBB) has been proposed before [229]-[235], where a number of generic power electronic modules can be used to synthesize large number of power topologies. This concept is very important for marine and aerospace power systems as it minimizes the number of spare parts required for the power electronic equipment onboard the ship/aero plane. The PEBB has been proposed with different topologies, for instance: a push-pull configuration [229], and an anti-series topology [235]. All the proposed PEBBs were implemented either using Silicon (Si) MOSFETs/IGBTs or Silicon Carbide (SiC) MOSFETs/IGBTs.

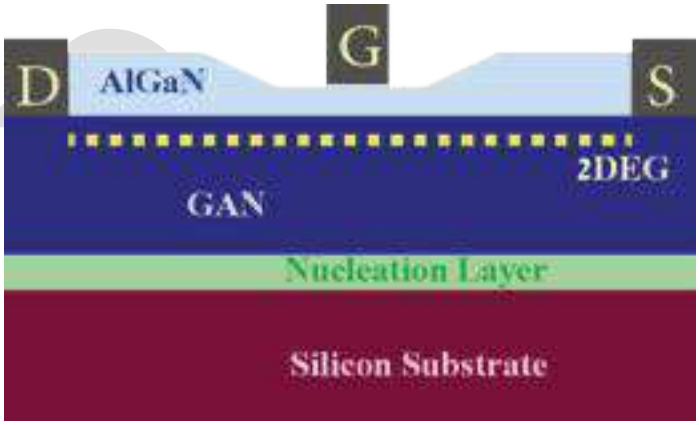


Figure 11.1: Generic structure of the lateral eGaN-FET HEMT.

The advent of enhancement Gallium Nitride (eGaN) High Electron Mobility Transistor (HEMT), with its groundbreaking features compared to its Si and SiC counterparts [236], [237], makes it an excellent candidate for the PEBB concept. The features of GaN, SiC, and Si materials are compared in Table 11.1. As shown in Figure 11.1, the generic structure of the lateral GaN

HEMT is based on the piezoelectric effect between a layer of GaN and a layer of Aluminum Gallium Nitride (AlGaN), which results in a 2-D electron gas (2-DEG) layer between the drain (D) and source (S) of the GaN HEMT, which reduces the on-resistance of the device [236]. In Table 11.2, a comparison between a number of commercial SiC, and GaN FETs with rated voltage of 600V/650V is presented. From this comparison, the eGaN HEMT from GaN Systems (GS66508T) has less on-resistance, input and output capacitances, reverse recovery charge, and total gate charge, which makes it a FET with lower switching and conduction losses compared to other devices.

In this chapter, an eGaN-FET based PEBB that is constituted by a half-bridge topology is presented. The PEBB has input and output filter capacitors, and a Nanorystalline filter inductor. Nanocrocytalline material is chosen because it has a high saturation flux density level, and high permeability in a broad frequency range [238]. These characteristics provide the possibility that the designed inductor could be small and compact. The rest of this chapter is organized as follows; section II presents the developed non-isolated eGaN PEBB, section III explains the possible topologies that can be synthesized with the developed PEBB. The results are presented in section IV and section V concludes this chapter.

Table 11.1: Material Properties of GaN, SiC, and Si

Parameter	GaN	SiC	Si
Bandgap (eV)	3.2	3.4	1.12
Breakdown Field (MV/cm)	3.3	3.5	0.3
Electron Mobility (cm^2/V.S)	2000	650	1500

Table 11.2: COMPARISON BETWEEN COMMERCIAL WBG DEVICES

	SiC	GaN	
	ROHM Semiconductor SiC-MOSFET SCT2120AF	**Transphorm Cascode-GaN TPH3205WS**	**GaN Systems eGaN-HEMT GS66508T**
V_{DS}	650V	600V	650V
Continuous I_D (25 °C)	29 A	36 A	30 A
$R_{DS(ON)}$ (T_J = 25 °C)	120 mΩ	52 mΩ	50 mΩ
Input Capacitance C_{ISS}	1200pF	2150pF	260pF
Output Capacitance C_{OSS}	90pF	119pF	65pF
Reverse Recovery Charge (Q_{rr})	53nC	136nC	0nC
Total Gate Charge ($Q_{G(TOT)}$)	61nC	27nC	6.5nC
Gate Charge (Q_{GD})	21nC	6nC	1.8nC

11.2 The Developed Non-Isolated eGaN FET-Based PEBB

The schematic of the developed non-isolated eGaN PEBB is presented in Figure 11.2, and the layout of the PEBB PCB is shown in Figure 11.3. All the parameters of the eGaN PEBB are enlisted in Table 11.3.

The eGaN PEBB is based on a half-bridge topology with integrated filter inductor, input and output capacitances, which renders it as an integrated compact solution to synthesize most of the

power electronic topologies (as discussed in section III) without the need to any extra components. Both gate drivers have isolated power supplies, which provide the gate driver of the upper switch independent on the lower switch status, this feature is critical in the cases where the upper switch stays "on" for a long period (ex. bus-clamping PWM). An isolated dc/dc converter provides an isolated supply for each gate driver, followed by a linear voltage regulator to provide 6.5V for the driver opto-coupler. The turn-on resistance (r_{on}), and the turn-off resistance (r_{off}) control the rising and falling times of the HEMT, which need to be adjusted in order to avoid voltage spikes (due to high dv/dt) and on the other hand not compromise the switching speed. According to [239], r_{on} needs to be five to ten times r_{off}. The ferrite bead (FB) at the gate pin damps the oscillations at the gate, which reduces the possibility of false turn-on.

Table 11.3: eGaN PEBB Parameters

Parameter	Value
Switches (S_1, S_2)	GS66508T
Filter Cap. (C_f)	440 µF
Isolated DC/DC converter (5V to 9V)	PDS1-S5-S9-M-TR
Driver	SI8261BAC-C-IS
r_{on}	50 Ω
r_{off}	10 Ω
Pull-down resistor	10 kΩ
Ferrite Bead (FB)	74279268
Zener Diode	MMSZ5235BS-7-F
Microcontroller	TMS320f28377s

A zener diode with reverse breakdown voltage of 6.8V to clip any voltage spikes. The banana jacks (J_1, J_2, J_3, J_4, J_5, J_6) are used to connect the supplies, loads, and/or an external customized filter inductor,

11.3 Possible Topologies Using the eGaN PEBB

In this section, the possible dc/dc, dc/ac (single-phase), and dc/ac (three-phase) are discussed. The possible configurations are shown in Figure 11.4, and two examples of dc/ac systems modulation are explained in Figure 11.5 and Figure 11.6.

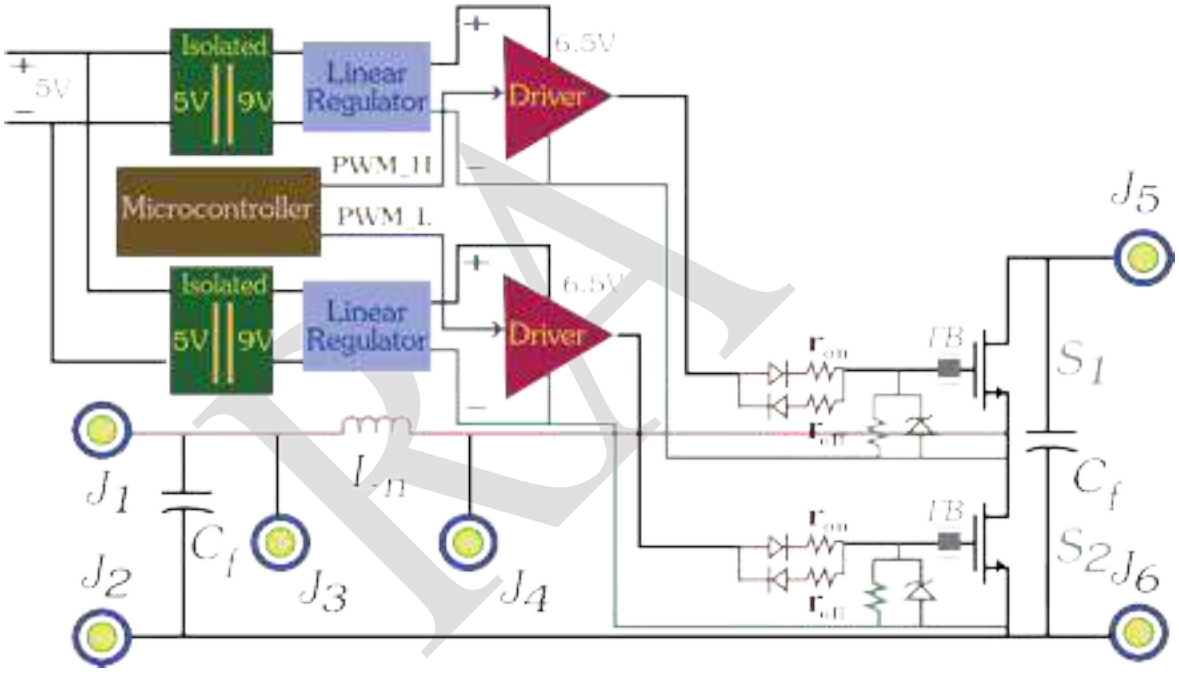
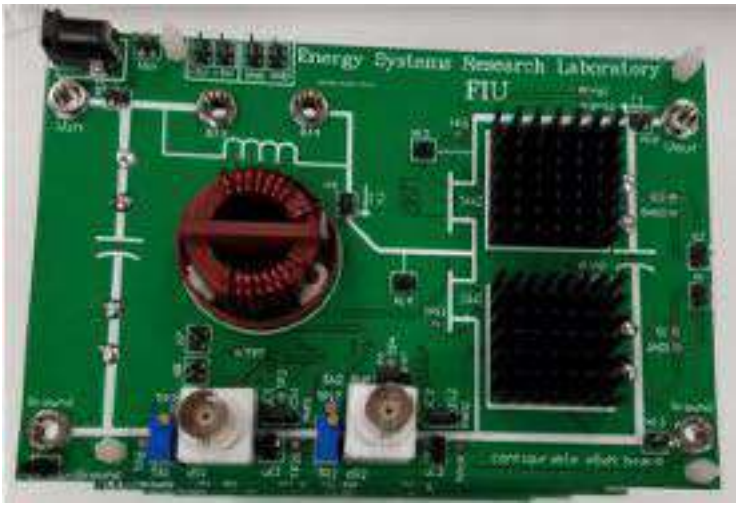


Figure 11.2: eGaN FET PEBB schematic: power stage, driver, voltage regulation, filter stage and control.



(a)

(b)

Figure 11.3: eGaN FET PEBB (a) top side, (b) bottom side.

11.3.1 DC-DC Topologies

The developed PEBB can be directly used as a bi-directional buck converter or bi-directional boost converter (depends on the location of source and load) as shown in Figure 11.4(a). The connection of the source and load can be changed as depicted in Figure 11.4(b) to synthesize an inverting bi-directional buck-boost converter. In Figure 11.4(c), a non-inverting buck-boost converter is synthesized using two PEBBs.

11.3.2 Single-Phase DC-AC Topologies

Generating an ac output using dc/dc converters can be achieved using differential mode configuration, which is based on using two bi-directional dc/dc converters to synthesize a single-phase inverter [240].

Adding a dc offset is necessary in such a way that the output of each converter is either positive (non-inverting converters) or negative (inverting converters). An example of a single-phase buck-boost inverter is shown in Figure 11.5(a). The output of each converter is depicted by (1), and (2), and the differential output is depicted in (3).

$$V_a{}^* = V_{DC} + \frac{V_{abm}^* \sin(\omega t)}{2} \quad (1)$$

$$V_b{}^* = V_{DC} + \frac{V_{abm}^* \sin(\omega t+\pi)}{2} \quad (2)$$

$$V_{ab}{}^* = V_{abm}^* \sin(\omega t) \quad (3)$$

Where (V_{abm}^*) is the magnitude of the reference differential output voltage (V_{ab}^*), and (V_{DC}) is the dc offset value. If the converters used are non-inverting, thus the output from each converter should be in the positive domain, as in Figure 11.5(b), while if the converters used are inverting, thus the output from each converter should be in the negative domain, as in Figure 11.5(c).

The concept of differential-mode connection can be used with bidirectional buck converters to build a 1-ph buck inverter, as shown in Figure 11.4(d), bidirectional boost converters to build a 1-ph boost inverter, as shown in Figure 11.4(e), inverting bidirectional buck-boost converters to build a 1-ph buck-boost inverter, as shown in Figure 11.4(f), or bidirectional non-inverting buck-boost converters to build a 1-ph buck-boost inverter, as shown in Figure 11.4(g).

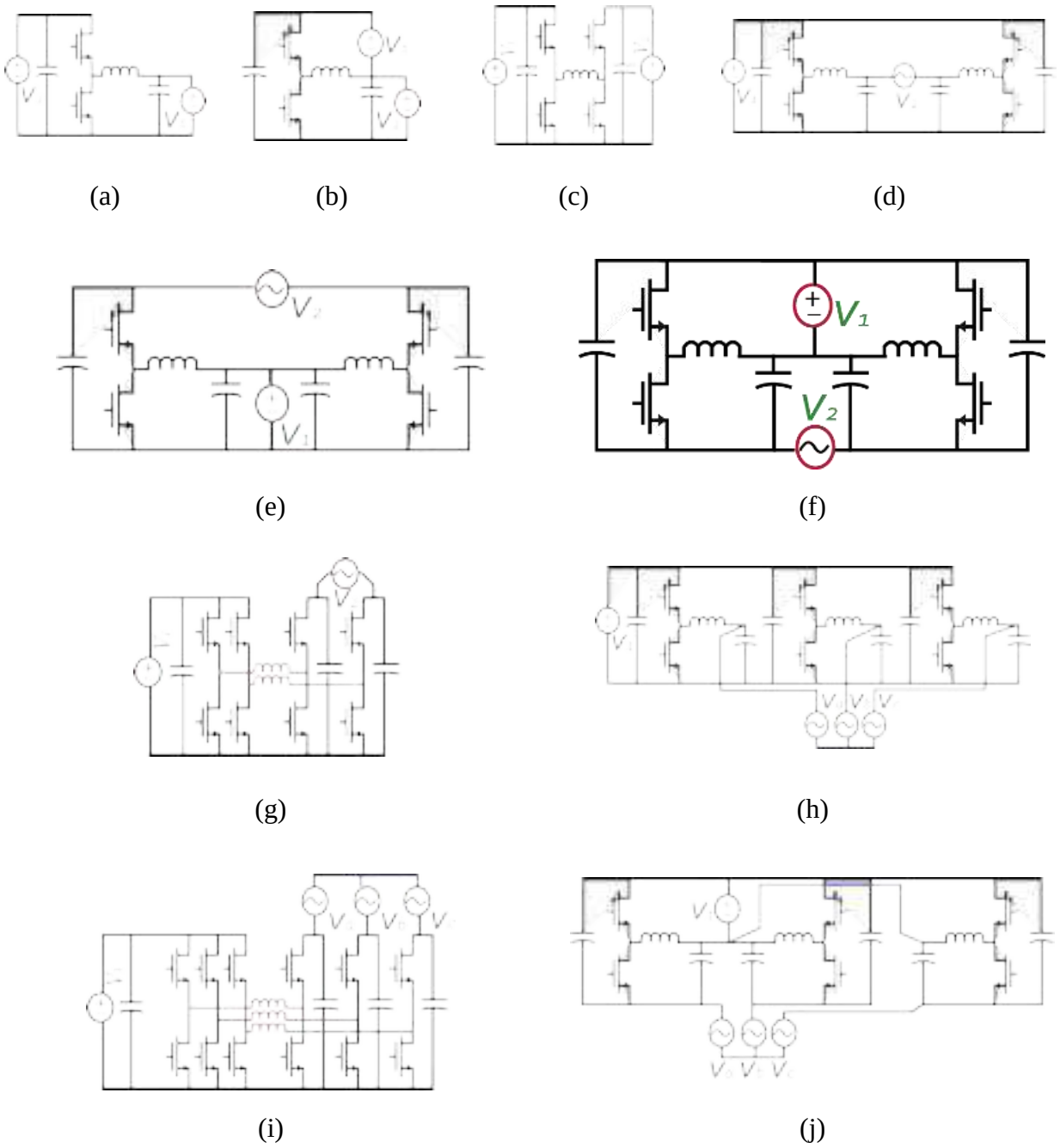
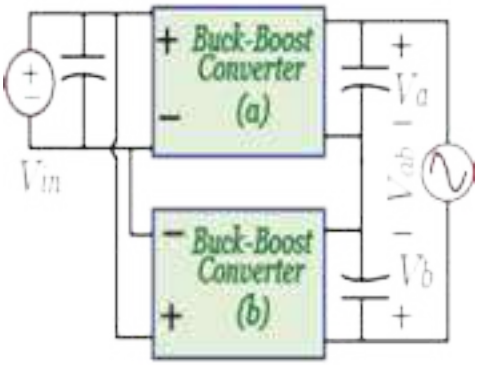
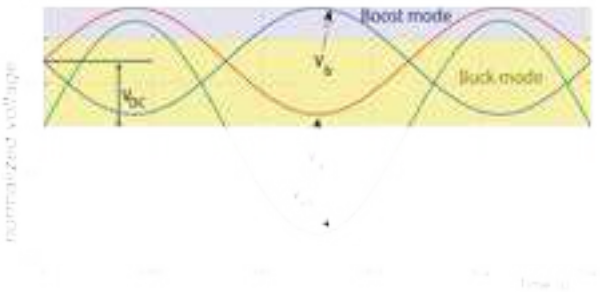


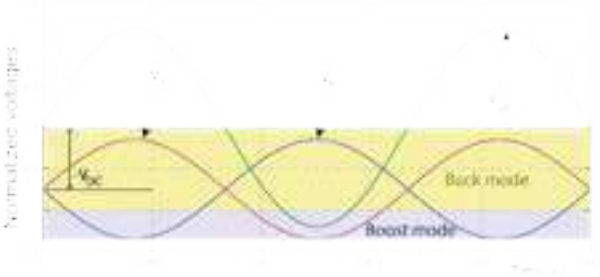
Figure 11.4: Possible configurations with the eGaN PEBB.



(a)



(b)

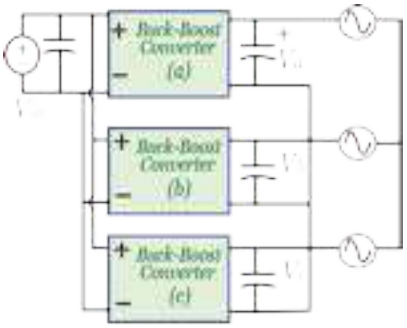


(c)

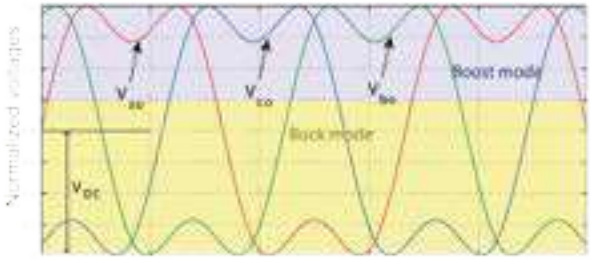
Figure 11.5: (a) Differential-mode 1-ph buck-boost inverter, (b) modulation (in case of non-inverting converters), (c) modulation (in case of inverting converters).

11.3.1 Three-Phase DC-AC Topologies

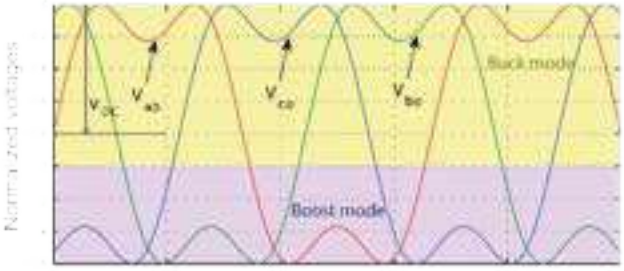
The idea of differential-mode connection can be extended to synthesize three-phase inverters using dc/dc converters [241], [242]. An example of a three-phase buck-boost inverter is shown in Figure 11.6(a).



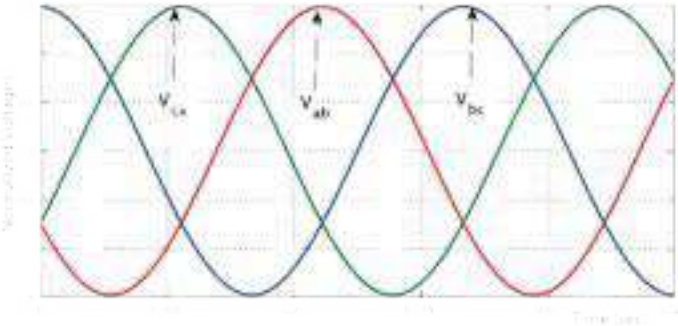
(a)



(b)



(c)



(d)

Figure 11.6: (a) Differential-mode 3-ph buck-boost inverter, (b) modulation (in case of non-inverting converters), (c) modulation (in case of inverting converters), (d) 3-ph line-line voltages.

The output of each converter is depicted in Figure 11.6 (b) (non-inverting converters), and Figure 11.6(c) (inverting converters). A third harmonic component can be added to reduce the voltage stress on the switches. The three-phase line-line voltages are the differential voltages between the three dc/dc converters, as the dc offset and the third harmonic components cancel out and three phase sinusoidal line-line voltages appear at the load terminals, as shown in Figure 11.6(d). This concept can be extended to synthesize a three phase buck inverter, as in Figure 11.4(h), or three phase buck-boost inverters, as in Figure 11.4(i), and Figure 11.4(j).

11.4 Experimental Results

A single-phase differential-mode buck-boost inverter (based on non-inverting buck-boost converters, as in Figure 11.4(g)), is investigated experimentally in this section. The circuit schematic is shown in Figure 11.7(a), as it is composed of four half bridges, two inductors, and input and output filter capacitors.

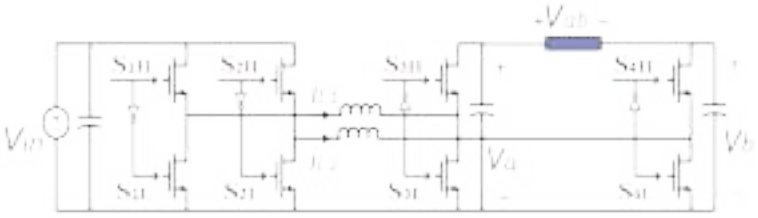
This system can be synthesized using four PEBBs. The connection diagram of the system is presented in in Figure 11.7(b), while the complete experimental setup is depicted in Figure 11.7(c). The setup is managed by the TMS320F28377S digital signal controller, generating PWM with switching frequency of 100 kHz, and the load is a 10 Ω resistor. The eGaN HEMTs used are GS66508T with rated current of 30A, rated drain-to-source voltage of 650V, on-resistance of 50 mΩ.

In the Table 11.3, the parameters for the experimental setup are shown. The inverter is operating in the buck mode, as the input voltage (V_{in}) from the power supply is equal to 189 V, the generated differential output is shown in Figure 11.8(a), with a positive peak voltage of 108 V,

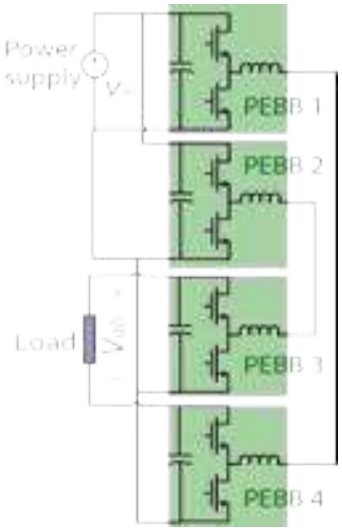
a negative peak voltage of -108 V, and a frequency of 18.66 Hz. Figure 11.8(b) shows the output voltage of each converter (V_a and V_b).

Table 11.4: Parameters For the Experimental Results

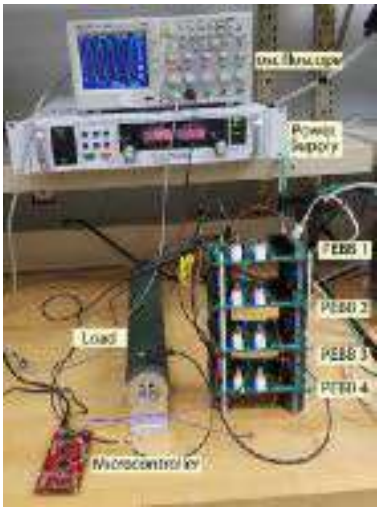
Parameters	Values
V_{source}	189 Vpk
$f_{generated}$	186 Hz
$Load$	10 Ω
f_s	100 kHz



(a)

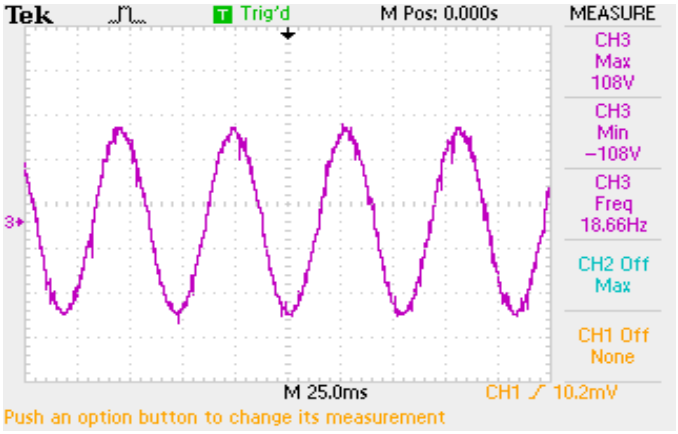


(b)

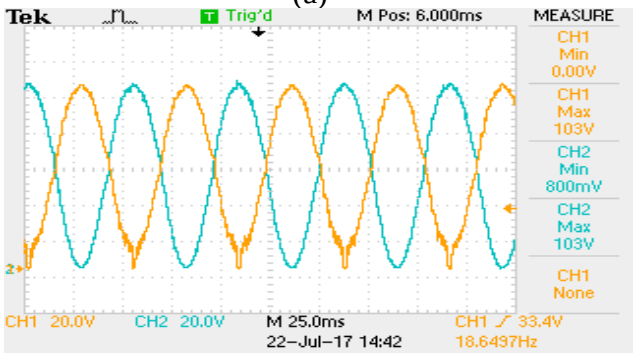


(c)

Figure 11.7: (a) Differential-mode 1-ph buck-boost inverter circuit, (b) Connection diagram, (c) Experimental setup.



(a)



(b)

Figure 11.8: (a) Differential-mode output voltage of the inverter. (b) Output voltage of each converter.

11.5 Conclusion

This chapter presents a non-isolated PEBB built with eGaN HEMT devices and Nanocrystalline inductor. The eGaN HEMTs have lower on-resistance and lower device capacitances compared to Si and SiC counterparts which make these devices have less conduction and switching losses, this results in less cooling system requirement, hence, a more compact PEBB. The utilization of the GaN HEMTs enables operation at high frequencies (≥100kHz), which yields smaller magnetics and passive components. This enables the integration of a complete system (switches, magnetics, and passive components) on a single board. One of the key challenges in designing power

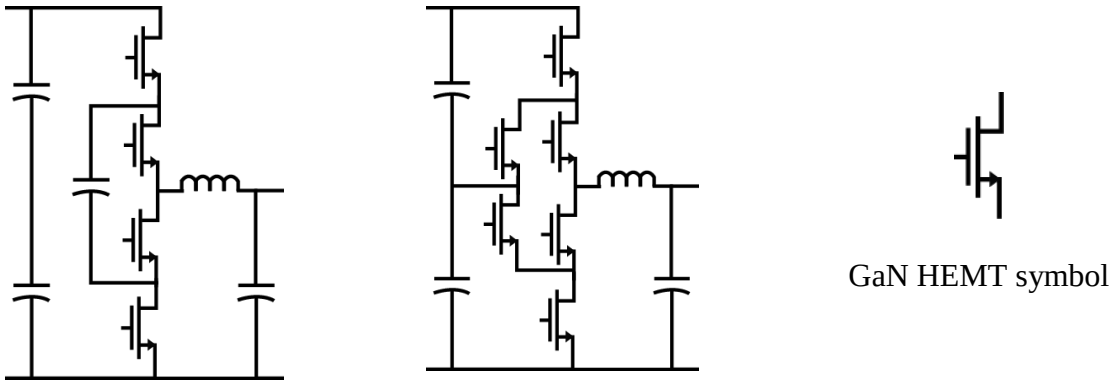
converters with GaN HEMTs is the low gate capacitance, which makes the switch vulnerable to oscillations at the gate (because of stray PCB inductance), which can lead to false turn-on since the threshold voltage of the eGaN HEMT is only 1.45V. This problem can be minimized by optimally designing the PCB and minimizing the stray inductances. The clean experimental results verify the proper operation of the system.

Chapter 12 Power Electronic Building Blocks Using Series-Stacked GaN eHEMT Modules

12.1 Introduction

The Power Electronic Building Block (PEBB) is a generic power electronic converter circuit that can be configured in different ways to synthesize popular power electronic architectures (DC-DC, DC-AC, AC-DC, and AC-AC converters). This can reduce the number of spare parts needed onboard a ship, plane, … etc., also the PEBB can reduce the manufacturing cost of the power electronic systems since the mass production of one generic power electronic architecture is more economical than producing application-specific power electronic architectures. Many literature have discussed different possible architectures for the PEBB, however, all of them are either implemented using Silicon (Si), or Silicon Carbide (SiC) Metal Oxide Field Effect Transistors (MOSFETs) or Insulated Gate Bipolar Junction Transistors (IGBTs), which suffer from high conduction and switching losses. A PEBB is built with Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) to reduce the conduction and switching losses of the transistors, since the GaN HEMTs have lower on resistance (R_{on}) and less device total charge. The major problem with GaN HEMTs is that their break down voltage is relatively lower compared to Si and SiC MOSFETs or IGBTs, which limits the utilization of GaN HEMTs to the low voltage applications. Multilevel half-bridge configurations can enable the utilization of GaN HEMTs in high voltage applications. These multilevel half-bridge configurations can possibly be based on a flying capacitor (FC) leg (as shown in Figure 12.1(a)) or a neutral point clamped (NPC) leg (as

shown in Figure 12.1(b)). The major problem of multilevel configurations is that they require a complex control scheme and more switches (as in the NPC) or more high voltage capacitors (as in the FC). In this patent application, a two level half-bridge-based PEBB is built with series-stacked GaN HEMTs. A Series-Switch-Driver (SSD) is utilized to balance out the voltage sharing between the series-stacked GaN HEMTs during transitions (turn on and turn off) and during steady state. The presented GaN-based PEBB has the capability to work at high voltages with high efficiency and require a simple control scheme.



(a) (b)

Figure 12.1: Possible multilevel half-bridge-based PEBBs.

12.2 Examples of the Existing Half-Bridge PEBBs

12.2.1 Two Level Half-Bridge-Based PEBBs Using Si/SiC MOSFETs/IGBTs

The two level half-bridge-based PEBB is composed of two transistors, these transistors can be either Si or SiC MOSFETs (shown in Figure 12.2(a)) or IGBTs (shown in Figure 12.2(b)).

This PEBB architecture is limited by the rated voltage of the transistors and suffers from high switching and conduction losses.

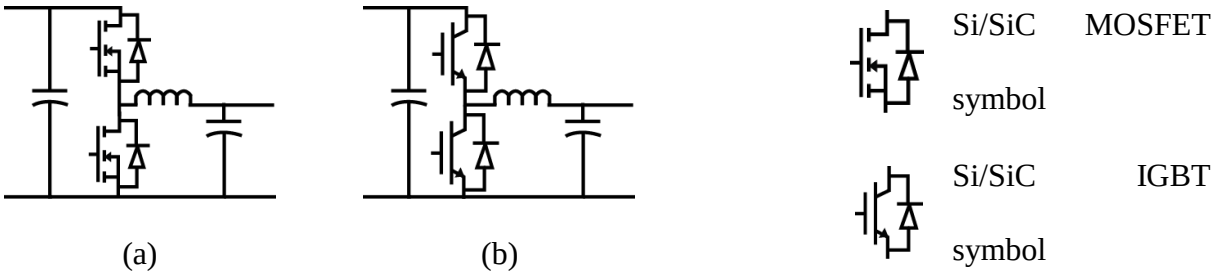


Figure 12.2: Two level half-bridge-based PEBB.

12.2.2 Two Level Half-Bridge-Based PEBB Using GaN HEMTs.

A two level half-bridge-based PEBB is built with GaN HEMTs to reduce the switching and conduction losses. The major problem of this PEBB is that the rated voltage is limited by the rated voltage of the GaN HEMTs utilized in the circuit.

Figure 12.3: Two level half-bridge-based PEBB Using GaN HEMTs.

12.2.3 Multilevel NPC-Based PEBBs Using Si/SiC MOSFETs/IGBTs

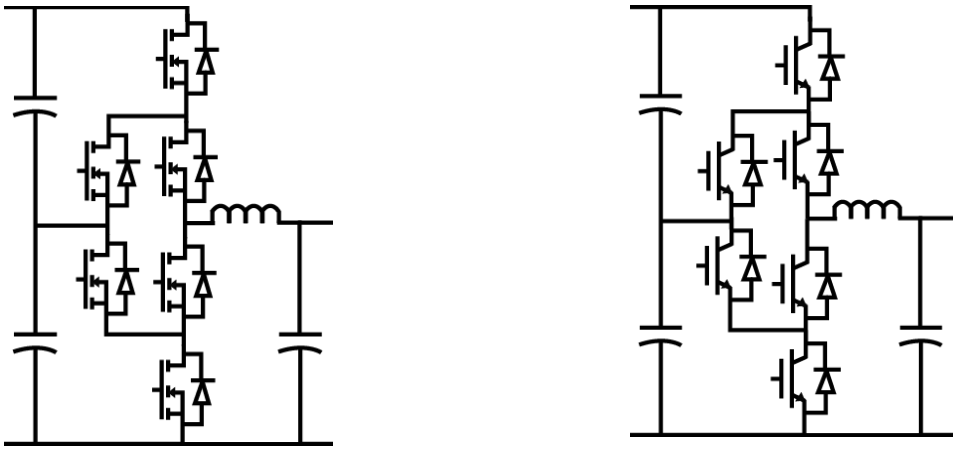
As a solution to extend the operating voltage of the PEBB beyond the rated voltage of the single transistors, a multilevel NPC half-bridge can be a PEBB.

The rated voltage of this PEBB = (number of levels – 1) × rated voltage of each transistor.

A NPC half-bridge-based PEBB built with SiC MOSFETs is presented. This NPC can be built with Si/SiC MOSFETs (as shown in Figure 12.4(a)), Si/SiC IGBTs (as shown in Figure 12.4(b)), or GaN HEMTs (as shown in Figure 12.1(b)). The major disadvantages of this PEBB architecture:

- Requires high number of semiconductor devices.

- Requires a complex control scheme.

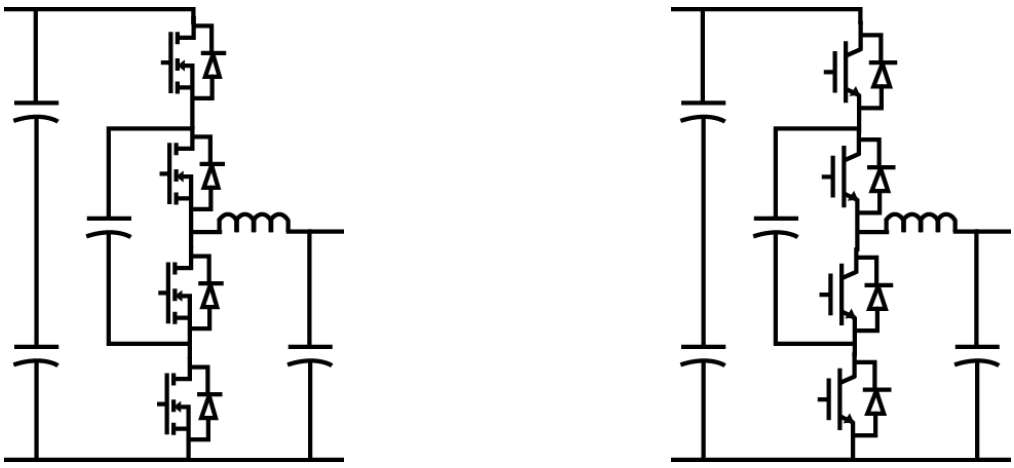


(a) (b)

Figure 12.4: NPC-based PEBB, (a) Using Si/SiC MOSFETs. (b) Using Si/SiC IGBTs.

12.2.4 Multilevel FC-Based PEBB Using Si/SiC MOSFETs/IGBTs

Another architecture that can be used to extend the rated voltage of the PEBB beyond the rated voltage of the single transistors is a FC half-bridge-based PEBB, where a FC half-bridge is used as a PEBB.



(a) (b)

Figure 12.5: FC-based PEBB, (a) Using Si/SiC MOSFETs. (b) Using Si/SiC IGBTs.

The rated voltage of this PEBB = (number of levels – 1) X rated voltage of each transistor. This NPC can be built with Si/SiC MOSFETs (as shown in Figure 12.5(a)), Si/SiC IGBTs (as shown in Figure 12.5(b)), or GaN HEMTs (as shown in Figure 12.1(a)). The major disadvantages of this PEBB architecture:

- Requires high number of high-voltage capacitors, which increases the weight and size.
- Requires a complex control scheme.

12.3 The proposed PEBB Using Series-Stacked GaN HEMTs

The proposed PEBB is presented in figure 12.6. Series-stacked GaN HEMTs with an SSD form a GaN module that is driven via only one gate pin (more details about the structure of the GaN module and its SSD are presented in section 12.4). The proposed PEBB is based on a half-bridge where it is composed of two GaN modules (upper module and lower module), two high voltage capacitors, a power inductor, and power terminals. Possible power electronic architectures that can be synthesized with the proposed PEBB are shown in section 12.5.

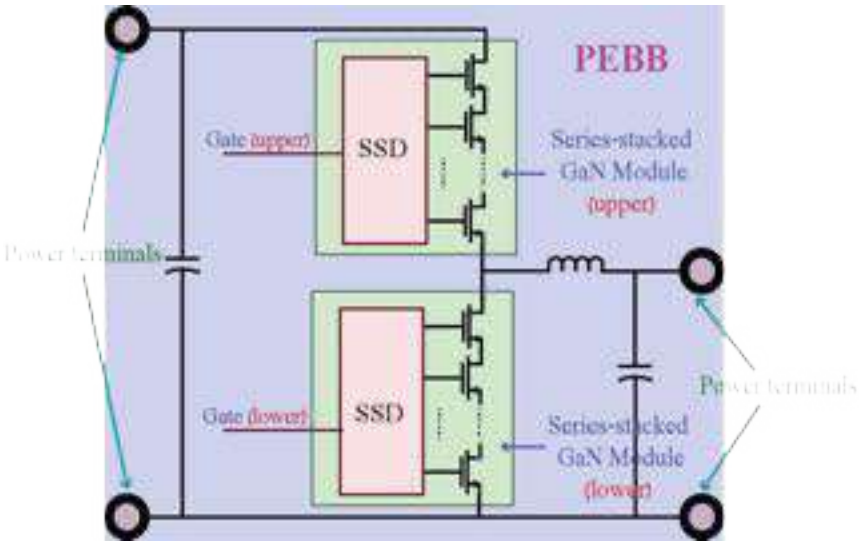


Figure 12.6: The proposed PEBB using series-stacked GaN modules.

12.4 The Series-Switch-Driver (SSD)

The SSD structure is developed to drive series-connected GaN HEMTs (constructing one GaN module). This SSD needs a single gate power supply and one Pulse Width Modulation (PWM) pin is required to drive the GaN module. The operation of the SSD can be explained in two major ways. Firstly, it gives gate charge of the HEMTs during turn-on with a minimum propagation delay between the gate-source potentials of the HEMTs. Secondly, the developed SSD assures balanced voltage sharing between the switches during switching transients and in the off state. Figure 12.7 shows the structure of a two-series-stacked-GaN-switch module and the embedded SSD. Each component of the SSD makes a specific task. The resistors R_{s1} and R_{s2} which are parallel connected with the switches ensures similar voltage sharing between the HEMTs during the off state. The voltage deviation of the HEMTs in this period is associated with the difference between the HEMTs leakage current and also unbalanced voltage at the end of the turn-off period. The capacitor C_{d1} provides the turn-on gate charge of the upper HEMT. This capacitor along with the capacitor C_{d2} are the tools to regulate the variation speed of the HEMTs drain-source voltage (dV_{ds}/dt) to end up with balanced voltage sharing during switching transitions. The Zener diodes Z_{d1} and Z_{d2} are used to clamp the gate-source voltage at a specified voltage, and the Ferrite Beads FB_1 and FB_2 and the resistor *r* damp the ringing in the gate-source voltage. The location and value of the resistor *r* and the FB specifications depend on the ringing of the gate-source voltage which itself is caused by the parasitic inductance of the gate loop. The FB1 is used in the turn-off loop of the upper HEMT since in this configuration, the gate voltage ringing occurred just in the turn-off transition. If the ringing is also observed in the turn-on transition, the FB2 will be connected in series with resistor *r*. The ferrite beads FB1 and FB2 are specified by their impedance at 100MHz

and the appropriate FBs are selected based on the amplitude and the frequency of the gate voltage ringing.

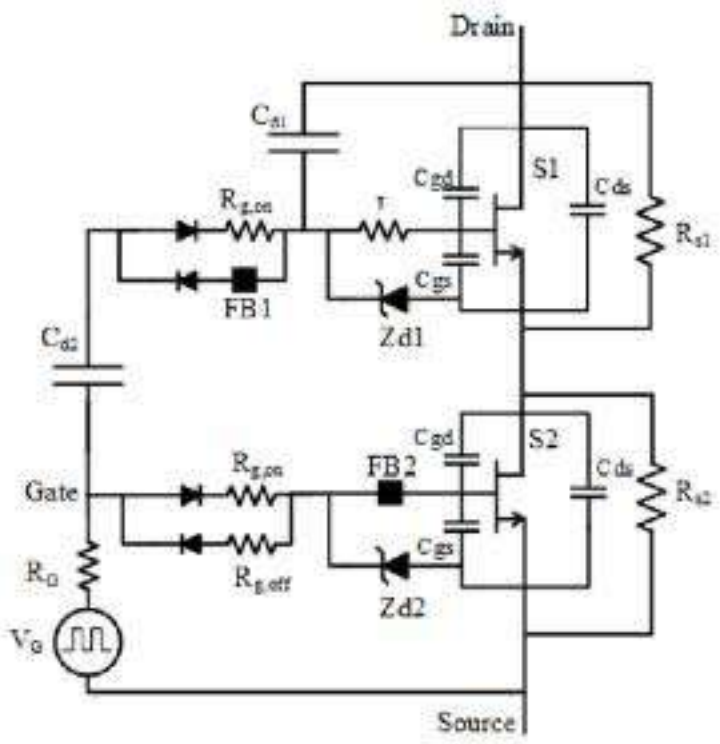


Figure 12.7: A GaN module of two HEMTs and the SSD.

To ensure the proper turning-on process of the upper HEMT, a minimum value of C_{d2} is required which depends on the required gate charge of the HEMT. As C_{d2} increases, the variation slope of the drain-source voltage (V_{ds}) of the lower HEMT during switching transitions decreases which in turn results in longer switching period and higher switching loss. The variation slope of V_{ds1} and V_{ds2} during the turn-on transition can be calculated using the following equations.

$$\frac{dv_{ds2}(t)}{dt} = \frac{(V_G - V_{gs,p})}{\frac{Q_{GD}}{V_{DS}}\left(R_G + R_{g,on1}\right) + R_G C_{d2}} \tag{1}$$

$$\frac{dv_{ds1}(t)}{dt} = \frac{C_{d2}}{\left(C_{d1} + \frac{Q_{GD}}{V_{DS}}\right)\left(\frac{Q_{GD}}{V_{DS}}\right)\left(R_G + R_{g,on1}\right) + R_G C_{d2}} \frac{(V_G - V_{gs,p})}{} \tag{2}$$

Where $V_{gs,p}$, Q_{GD} and R_G represent the Miller plateau voltage, the total gate-drain charge of the HEMT and the internal resistor of the gate driver, respectively.

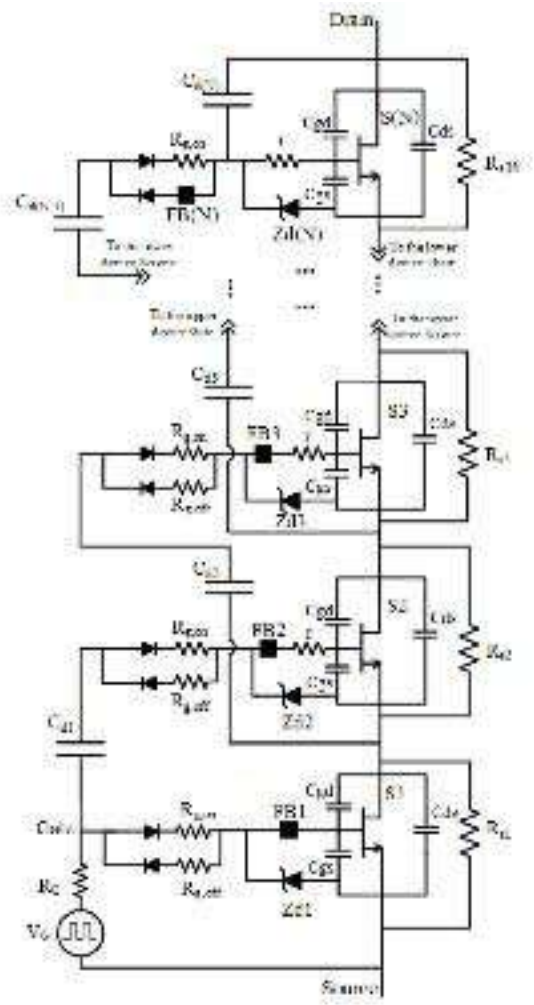


Figure 12.8: A GaN module of more than two HEMTs and the SSD.

Based on (5) and (6), one can conclude that the higher values of the resistors R_G, and $R_{g,on1}$ result in lower $\frac{dv_{ds}}{dt}$. Moreover, bigger C_{d1}, and C_{d2} also cause lower $\frac{dv_{ds1}}{dt}$ and $\frac{dv_{ds2}}{dt}$, respectively.

The described idea for sharing the voltage between two HEMT s can be extended for multiple HEMTs. In this procedure, the main concern is to provide enough gate charge for the upper HEMTs to reach a sufficient gate voltage so that the HEMT is fully turned on. This is required to ensure that the HEMT is operating in the resistive (linear) region with a very low R_{on} and consequently low on-state power loss. As the number of HEMTs in the stack exceeds two, this task becomes more challenging. An additional circuit can be used to provide gate charge for the upper HEMTs. In this circuit, a boost capacitor feeds additional charge to the upper HEMTs after the turn-on transition so that a sufficient gate voltage is achieved.

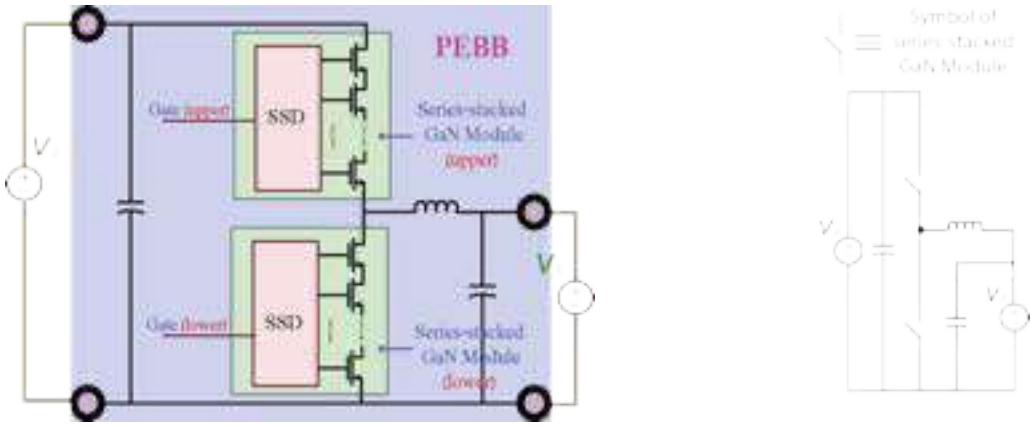
A series-stacked GaN module with more than two GaN HEMTs is presented in Figure 12.8. In this circuit, the gate charge of the third HEMT is provided through C_{d2} which is connected between the gate of the third HEMT and the source of the second HEMT. Similarly, the capacitor $C_{d(i-1)}$ is responsible for the turn-on gate charge of the i^{th} HEMT. The stored charge of the capacitor $C_{d(i-1)}$ itself is fed from the load current during the turn-off transition. On the other hand, this capacitor controls the variation rate of the drain-source voltage of the $(i-1)^{th}$ HEMT during the switching transitions.

Another challenge in the extension of the series-stacked HEMTs in the GaN module is to ensure voltage balance between the HEMTs specifically the upper HEMTs. There is a slight delay between the gate-source voltages of two adjacent HEMTs, so the delay between the first and the last HEMT would be the summation of all of the adjacent HEMT delays. This delay between the gate voltages of the HEMTs, causes a delay between the times at which the drain-source

voltages of the HEMTs starts to increase in the turn-off period. The first HEMT waveforms lead those of the last HEMT. In order to compensate for this delay, the dV_{ds}/dt of the first HEMT should be slowed down so that the V_{ds} of the both HEMTs reaches their final values at the same time and consequently balanced voltage across the HEMTs at the end of the turn-off period and during the off state of the HEMTs will be guaranteed. To achieve this goal, higher value of C_{d1} (and similarly $C_{d(i)}$) is needed which in turn prolongs the switching transition. Thus, when using large number of HEMTs in series, to ensure balanced voltage across all of the HEMTs, longer switching transitions will be resulted. Consequently, there is a tradeoff between the number of series-stacked HEMTs and the switching loss and the switching frequency.

12.5 Possible PEBB Systems

In this section examples of possible power electronic architectures synthesized with the proposed PEBB are illustrated. For each example the connection diagram is presented along with the circuit (for better illustration).



(a) (b)

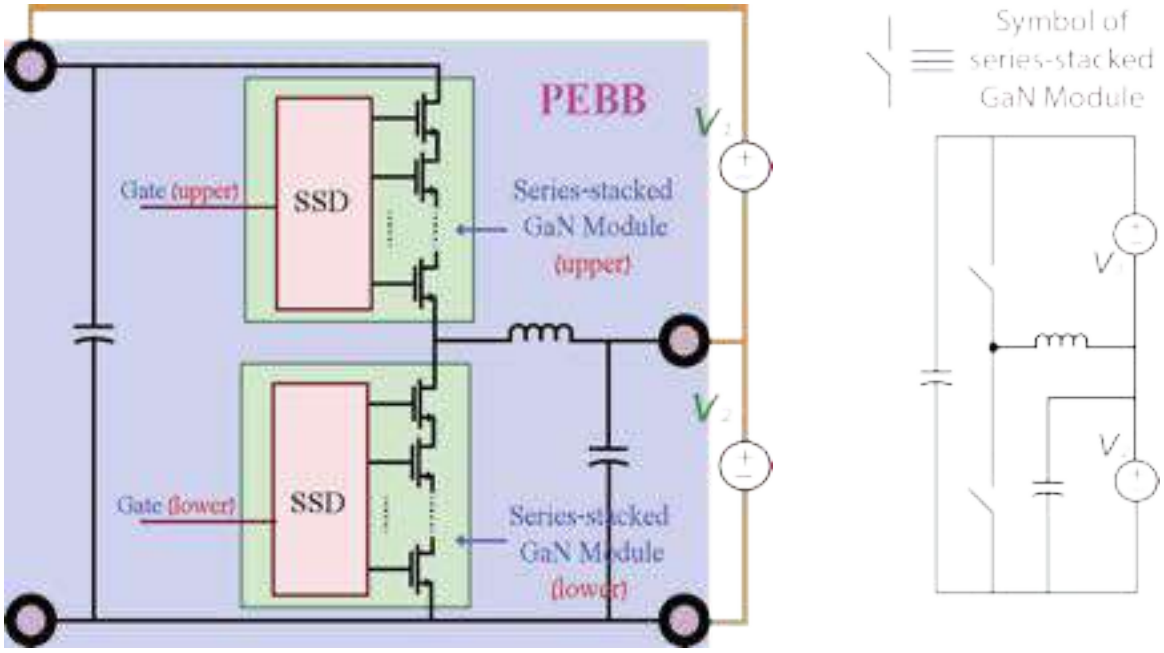
Figure 12.9: A synchronous buck DC-DC converter (a) Connection diagram. (b) Circuit.

12.5.1 Synchronous Buck DC-DC Converter

A synchronous buck converter can be synthesized with one PEBB, where a source is connected as V_2 and a load is connected as V_1 (buck mode), or a source is connected as V_1 and a load is connected as V_2 (boost mode). Figure 12.9(b) shows the circuit diagram of a synchronous buck converter, and Figure8 (a) shows the connection diagram of a synchronous buck converter.

12.5.2 Bidirectional Inverting Buck-Boost DC-DC Converter

A bidirectional inverting buck-boost converter can be synthesized with one PEBB, where a source is connected as V_2 or V_1, and the load is connected as V_1 or V_2, respectively.



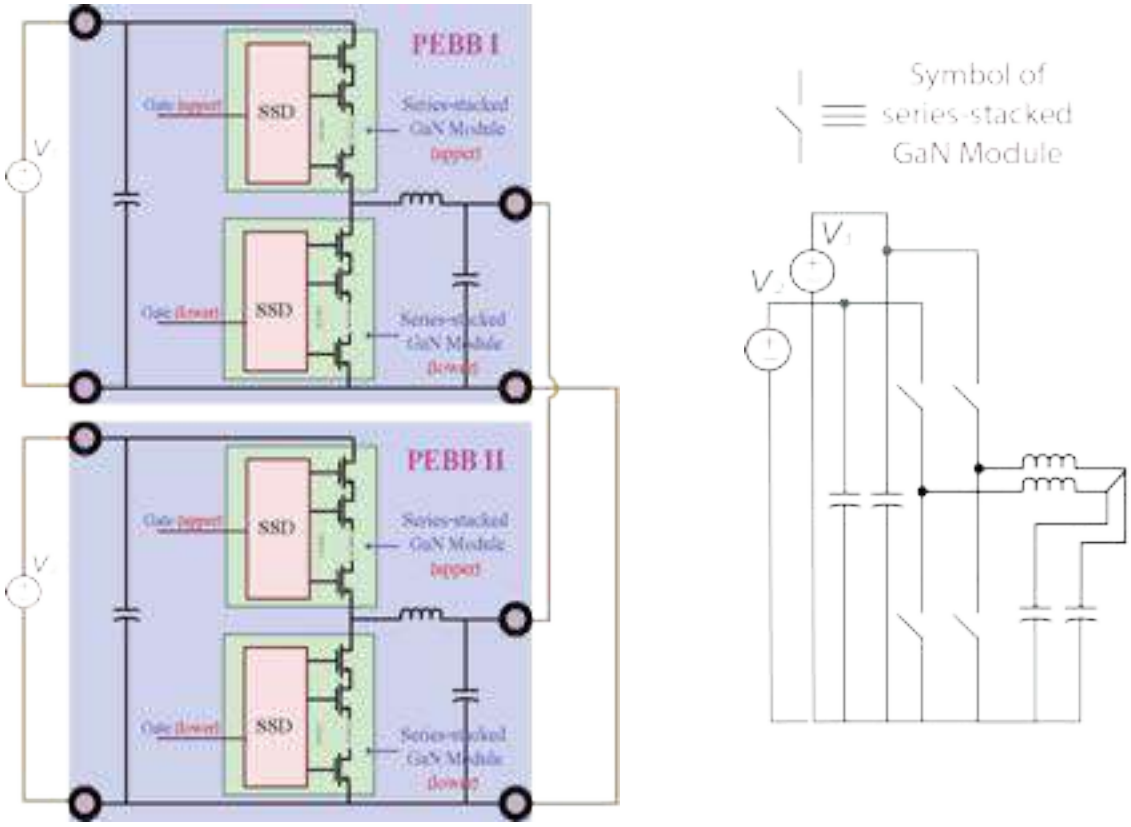
(a) (b)

Figure 12.10: A bidirectional inverting buck-boost DC-DC converter (a) Connection diagram. (b) Circuit.

12.5.3 Bidirectional Non-Inverting Buck-Boost DC-DC Converter

A bidirectional non-inverting buck-boost converter can be synthesized with two PEBBs, where a source is connected as V_2 or V_1, and the load is connected as V_1 or V_2, respectively. Figure

12.11(b) shows the circuit diagram of a bidirectional non-inverting buck-boost converter, and Figure 12.11(a) shows the connection diagram of a bidirectional non-inverting buck-boost converter.

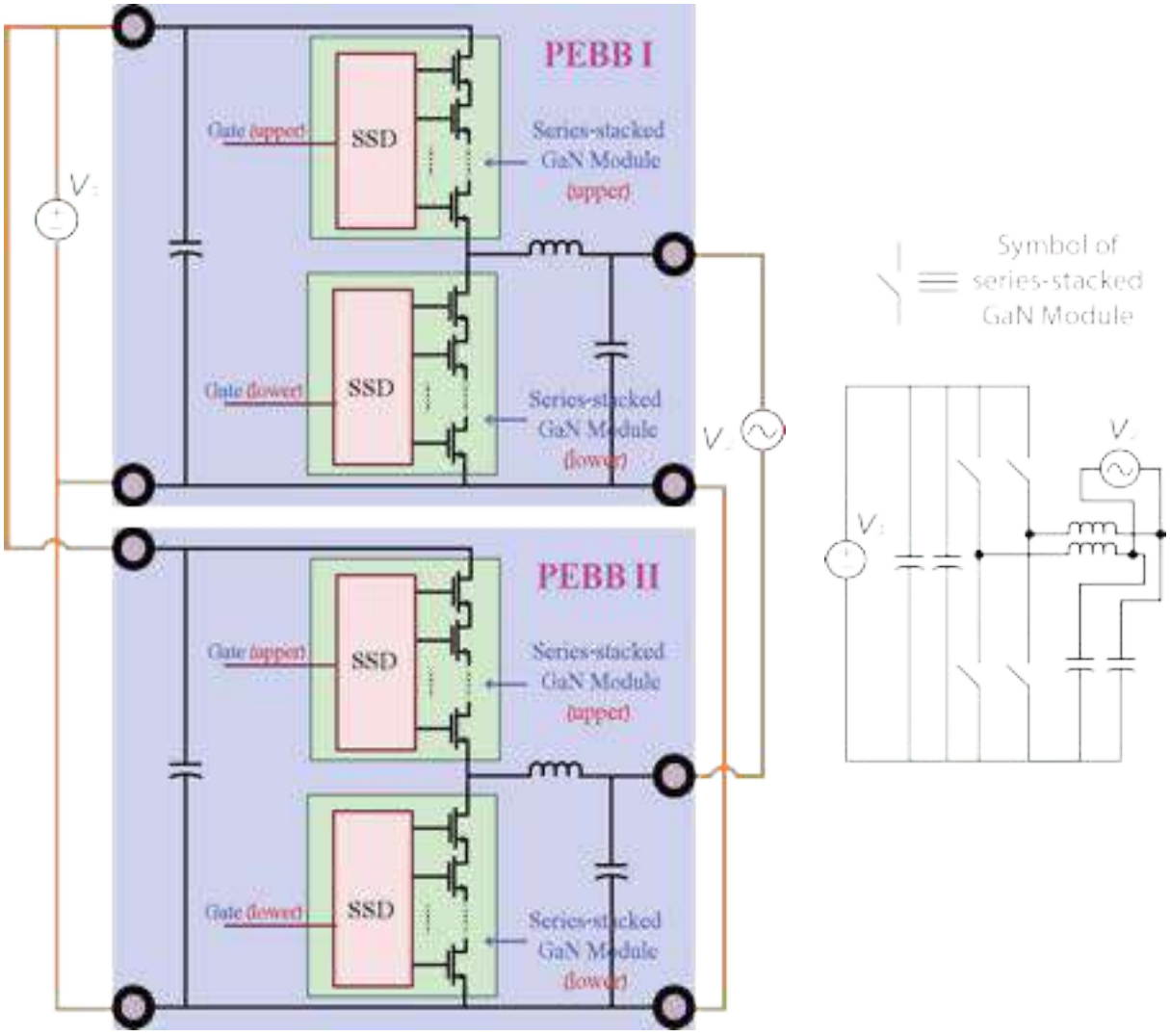


(a) (b)

Figure 12.11: A bidirectional non-inverting buck-boost DC-DC converter (a) Connection diagram. (b) Circuit.

12.5.4 Single-Phase Buck DC-AC Inverter

A single-phase buck inverter can be synthesized with two PEBBs, where a dc source is connected as V_1, and the ac load is connected as V_2. Figure 12.12(b) shows the circuit diagram of a single-phase buck inverter, and Figure 12.12(a) shows the connection diagram of a single-phase buck inverter.

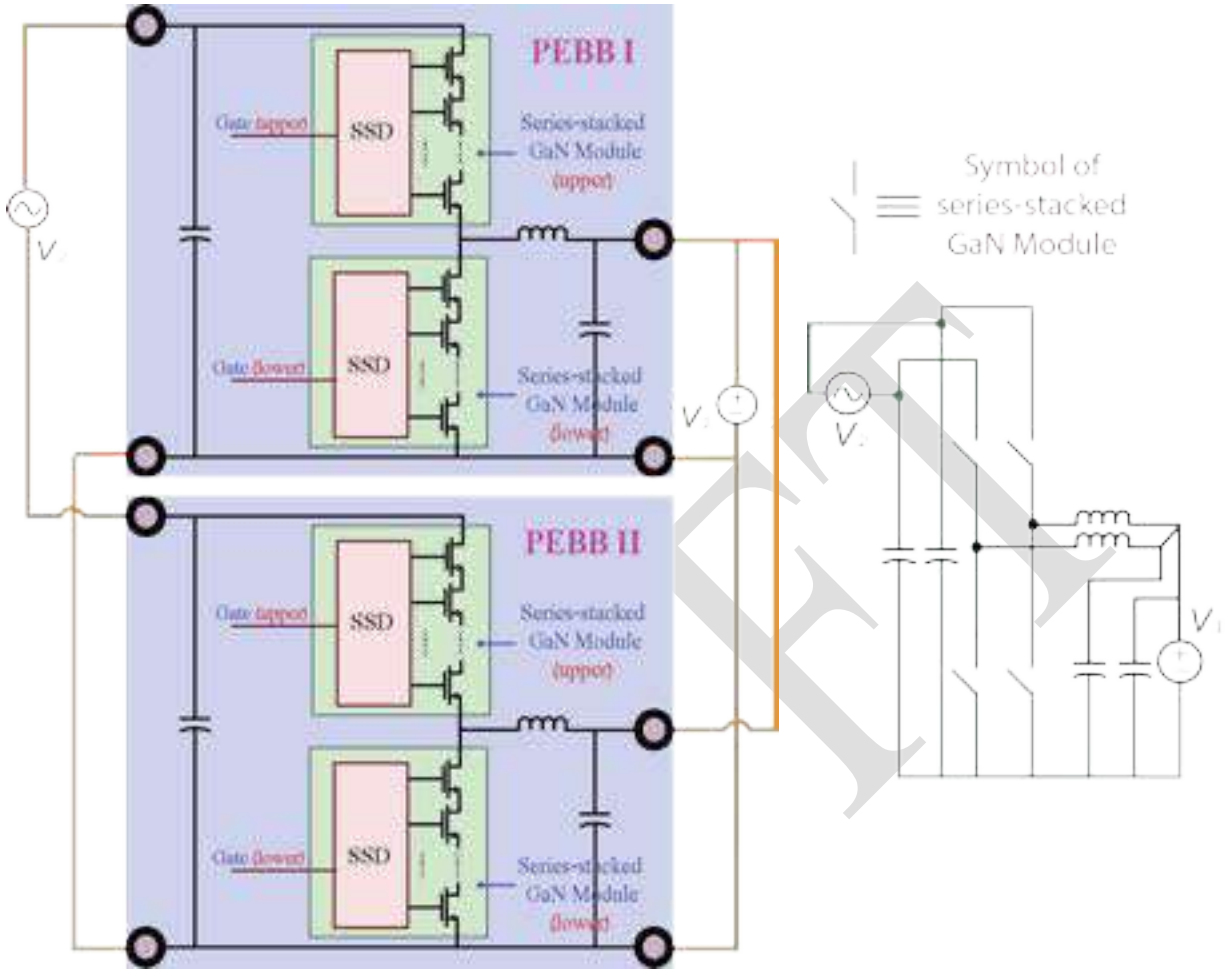


(a) (b)

Figure 12.12: A single-phase buck DC-AC inverter (a) Connection diagram. (b) Circuit.

12.5.5 Single-Phase Boost DC-AC Inverter

A single-phase boost inverter can be synthesized with two PEBBs, where a dc source is connected as V_1, and the ac load is connected as V_2. Figure 12.13(b) shows the circuit diagram of a single-phase boost inverter, and Figure 12(a) shows the connection diagram of a single-phase boost inverter.



(a) (b)

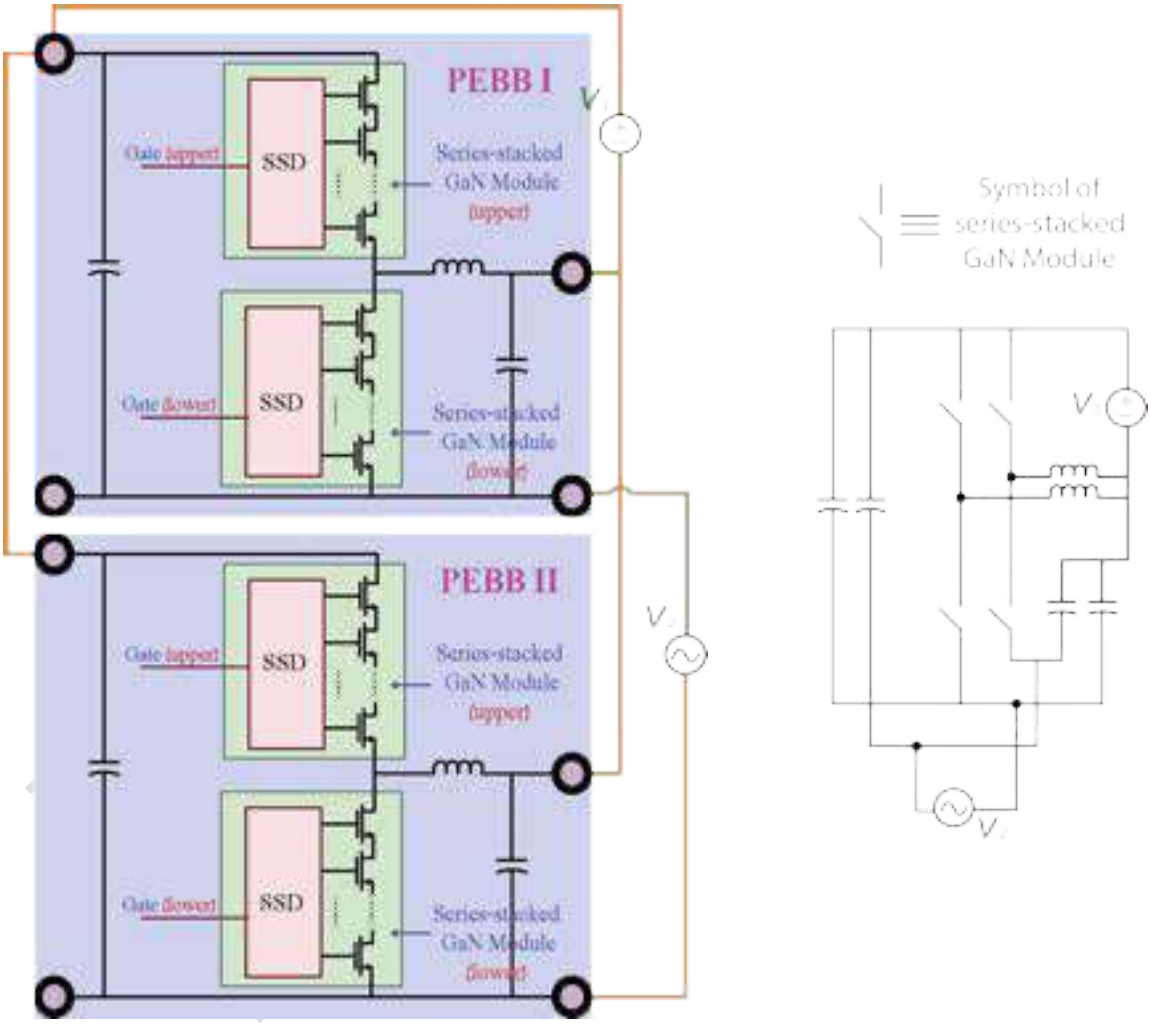
Figure 12.13: A single-phase boost DC-AC inverter (a) Connection diagram. (b) Circuit.

12.5.6 Single-Phase Buck-Boost DC-AC

A single-phase buck-boost inverter can be synthesized with two PEBBs, where a dc source is connected as V_1, and the ac load is connected as V_2. Figure 12.14(b) shows the circuit diagram of a single-phase buck-boost inverter, and Figure 12.14(a) shows the connection diagram of a single-phase buck-boost inverter.

12.5.7 Three-Phase Buck DC-AC Inverter

A three-phase buck inverter can be synthesized with three PEBBs, where a dc source is connected as V_1, and the three ac loads are connected as V_a, V_b, and V_c. Figure 12.15(b) shows the circuit diagram of a three-phase buck inverter, and Figure 12.15(a) shows the connection diagram of a three-phase buck inverter.

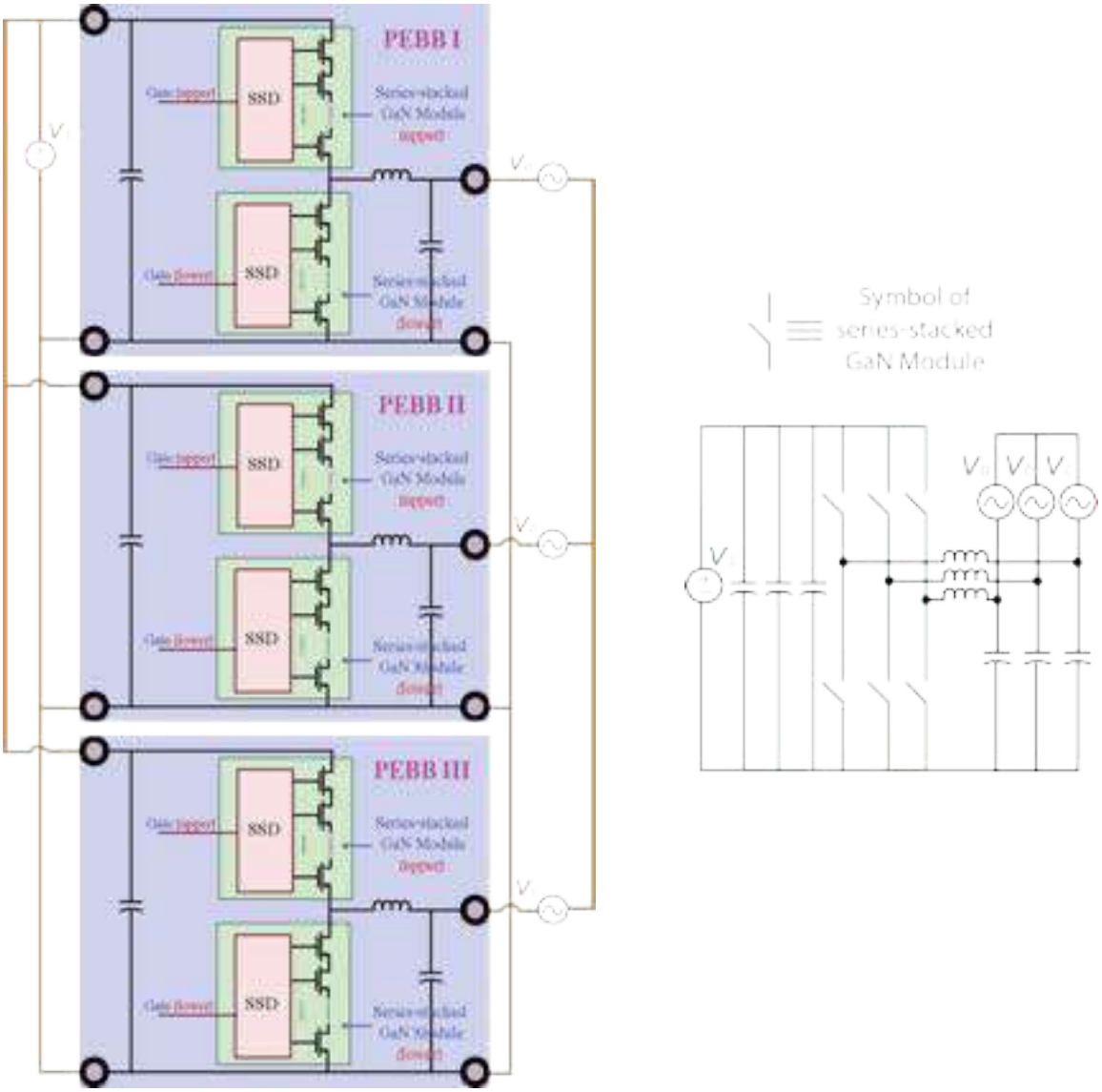


(a) (b)

Figure 12.14: A single-phase buck-boost DC-AC inverter (a) Connection diagram. (b) Circuit.

12.5.8 Three-Phase Buck-Boost DC-AC Inverter

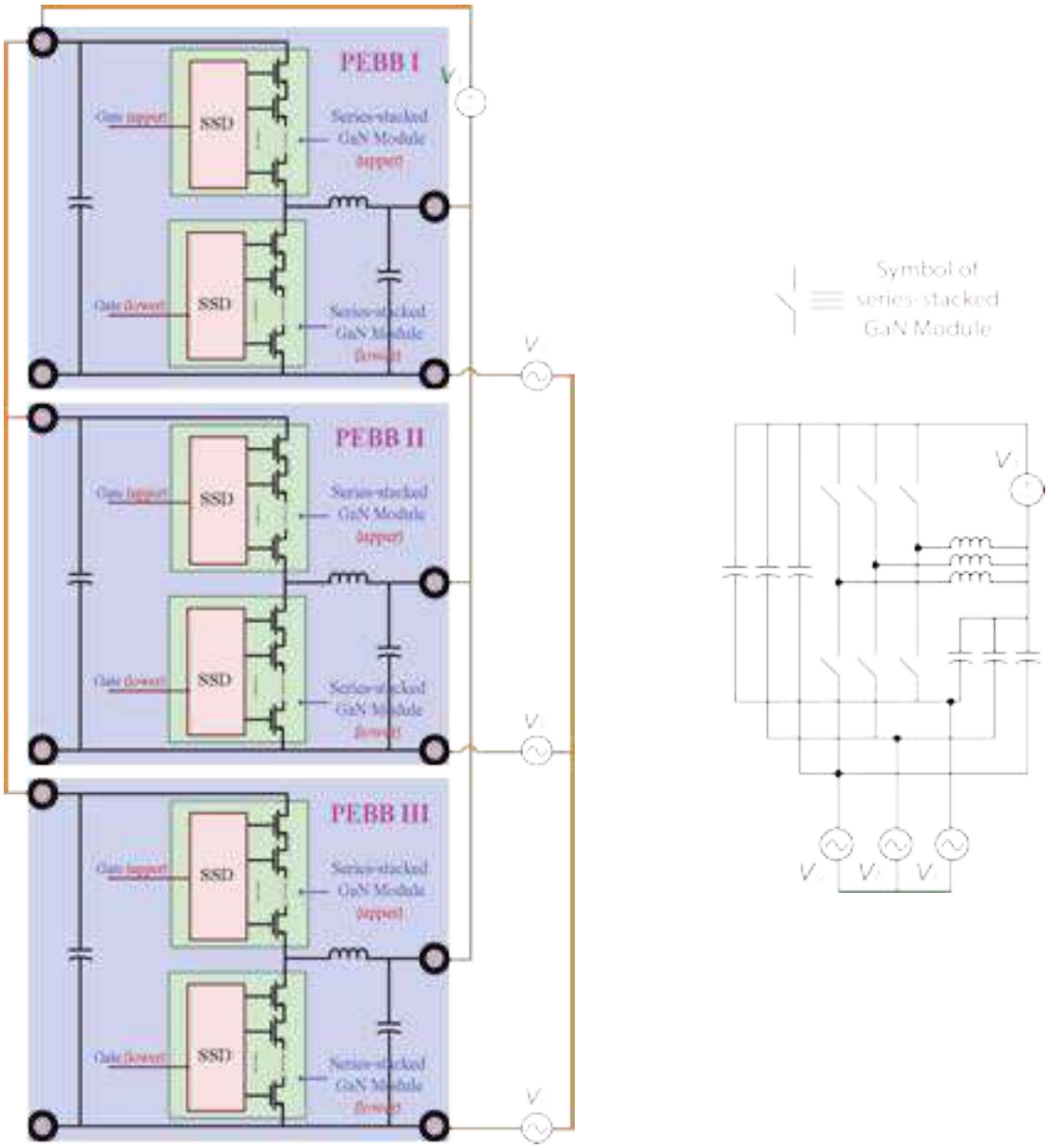
A three-phase buck-boost inverter can be synthesized with three PEBBs, where a dc source is connected as V_1, and the three ac loads are connected as V_a, V_b, and V_c.



(a) (b)

Figure 12.15: A three-phase buck DC-AC inverter (a) Connection diagram. (b) Circuit.

Figure 12.16(b) shows the circuit diagram of a three-phase buck-boost inverter, and Figure 12.16(a) shows the connection diagram of a three-phase buck-boost inverter.



(a) (b)

Figure 12.16: A three-phase buck-boost DC-AC inverter (a) Connection diagram. (b) Circuit.

12.6 Conclusion

In this chapter a new power electronic building block with series-stacked GaN modules using a series-switch driver. The developed structure has high efficiency, reduced system cooling requirement, high power density, high specific power, simple control since it is driven as a simple two-level push-pull leg, each GaN module requires only one gate driving signal, and the rated voltage of the PEBB can be extended systematically by increasing the number of series GaN HEMTs in the GaN Module.

Chapter 13 Conclusions and Future Work

13.1 Conclusions

The dissertation provided different cost-effective solutions to allow the wide-bandgap devices (i.e. Gallium Nitride and Silicon Carbide devices) to be utilized in high power applications such as microgrids, electrified means of transportation, and renewable energy systems. These solutions are based on developing new power converter topologies and high voltage series-stacked wide-bandgap switching modules.

Firstly, the technique of series stacking of the active switches extends the breakdown voltage of the power switch, thus, can be directly utilized for high voltage applications. Typically, series-stacking of the power switches is either done via an active gate driver or passive snubber circuits. The active gate driver requires an additional control circuit to control the adequate charges injected into the gate of each switch in the series array. This solution is complicated and increases the cost of the switching module. The passive snubber solution utilizes a passive branch that is composed of a capacitor and a resistor in order to balance out the voltage stress across the series-connected switches. This approach has a simple circuit structure, nevertheless, it increases the conduction losses of the switching module. In addition, it slows down the turn-on and turn-off transitions, hence, it increases the switching losses of the module. The solution discussed in this dissertation is based on a quasi-active driving circuit that is based on a number of low voltage capacitors, resistors, and diodes in order to inject adequate charges into the gate of each switch in the series array. The proposed circuit has a relatively less complex circuit structure compared to the active gate driver solution, and lower conduction and switching losses compared to the passive snubber solution. The simulation and experimental results showed that the proposed series connected

switching module has equally shared voltage stresses across the single switches in the series-connected array.

Secondly, the topology of the power converter plays a very important and critical role in enabling the utilization of wide-bandgap devices in high power applications. The topology can reduce the voltage stresses on the semiconductor devices which allows devices with low rated voltage to be used in high voltage systems. Additionally, the converter topology can reduce the common mode noise of the converter by providing either a common ground or a constant potential difference between the ports of the converter, accordingly, the converter will require a more compact EMC filter.

In this dissertation, novel power converter topologies are proposed and analyzed. These converters are categorized into isolated and non-isolated topologies. The isolated topologies utilize a high frequency power transformer to provide galvanic isolation between the power sources and the load, distribute the voltage stress on the semiconductor devices, and provide high voltage conversion ratio. In this dissertation, two new isolated high-frequency ac (HFAC) link dc-ac converters are presented and analyzed. They have reduced number of switch count compared to the state-of-the-art isolated converters in literature. Additionally, the proposed isolated converter can support the voltage and frequency of the power grid during contingences. A new hysteresis current controller is proposed for the developed HFAC link converters. This current controller is simple and enhances the dynamic performance of the system.

The non-isolated converter topologies do not require a magnetic coupling component to achieve high voltage conversion ratios, thus, they are more cost effective compared to the isolated ones. Additionally, the elimination of the magnetic coupling components allows the power converter to operate at relatively higher switching frequencies. In this dissertation, six new transformerless dc-

dc converter topologies are proposed, discusses and compared with the state-of-the-art topologies in literature. Three of these new topologies are unidirectional power converters, while the other three are bidirectional.

The unidirectional converters have universal input voltage range and can be utilized for applications like photovoltaic and fuel cell systems. In the photovoltaic system application, the wide input range of the unidirectional power converter extends the allowed range of the maximum point power tracing (MPPT) which enhances the efficiency of the system. The universal input voltage of the unidirectional dc-dc converter is an important feature for fuel cells, as they have soft output characteristics where the output voltage drops drastically as the output current increases.

In this dissertation, three new unidirectional step-up dc-dc converters are proposed and discussed. The first one is based on the SEPIC converter with an integrated switched-capacitor cell and a discontinuous current quasi-Z-source network. This converter has a wide voltage gain, reduced voltage stress on the semiconductor devices a common ground between the input and output ports, and a continuous input current. The second converter also based on the SEPIC with an integrated dual-switched capacitor multiplier network. This converter has a higher voltage gain and lower voltage stress on its switches compared to the first converter. It also has a constant potential difference between the grounds of its ports which reduces the radiated EMI noise. The third converter utilizes the two multiplier networks used in the first two converters, as it integrates a dual-switched-capacitor multiplier and a discontinuous current quasi-Z-source network, and it has a high voltage gain and lower voltage stress on its semiconductor devices compared to the first two converters. In addition it has a continuous input current which prolongs the lifetime of the fuel cell and enhances the efficiency of the photovoltaic system.

Additionally, three novel bidirectional dc-dc converters with wide voltage conversion ratios and reduced voltage stresses on the semiconductor devices are presented and discussed in this dissertation. These converters are excellent candidates for the applications that utilize energy storage systems with wide voltage swings, where the wide voltage conversion ratios of the dc-dc converter either increases the energy exchange from/to the energy storage system for the same capacitance, or reduces the required capacitance of the energy storage system to have the same energy exchange rate. The first converter is based on the bidirectional versions of the inverting buck-boost and Ćuk converters. This converter can perform buck and boost voltage conversion operations in both power flow directions. The second converter is based on the bidirectional version of the SEPIC converter with an integrated switched-capacitor network and an active discontinuous current quasi-Z-source network. It can perform buck operation in one power flow direction and boost operation in the other power flow direction. In addition, it has a common ground between the ports of the converter. This makes it an excellent candidate for microgrid and nanogrids applications. The third converter is based on a quadratic bidirectional converter structure with an integrated switched capacitor multiplier. It can achieve very high voltage conversion ratios which makes it suitable for applications like low voltage energy storage systems. In addition, it can be extended by integrating more than one switched-capacitor multiplier, in order to further extended the voltage conversion ratios of the converter and reduce the voltage stresses of the individual switches.

Finally, a high voltage series-stacked GaN switching module is proposed, thoroughly discussed, and experimentally validated in this dissertation. The switching module utilize a quasi-active gate driver in order to inject adequate charges into the gate of each GaN switch in the series-stacked array to make sure the voltage stress is equally shared among the switches. This technique has a

simple circuit structure and does not need an extra controller, on the contrary with the series-stacked module with active gate drivers. In addition, the quasi-active gate driver does not affect the efficiency of the module, on the contrary with the series-stacked modules with passive snubber circuits. The proposed technique of series-stacking extends the breakdown voltage of the commercial GaN devices which make them suitable candidates to high voltage applications such as electric vehicles and microgrid applications.

13.2 Recommendations for Future Work

This dissertation covered several aspects related to the extension of the operating voltage of the wide-bandgap devices via proposing new dc-dc converter topologies and synthesizing a high voltage series-stacked switching module using GaN transistors. Despite the proposed solutions in this dissertation and the influx of research activities on the topic of using wide-bandgap devices in high voltage dc-dc systems in recent years, a number of interesting questions are yet to be addressed properly and comprehensively.

Most of the works either ignored, or only partly addressed, the reliability of the high voltage power electronic systems built with wide-bandgap devices. The thermal performance of these systems especially in harsh working environments is a critical aspect of research and development that needs to be addressed properly.

Another pressing issue is the development of reliable high power ac-dc and dc-ac systems that can be used for traction applications. The utilization of wide-bandgap devices can have huge impact on the efficiency and performance of these systems since they have lower on resistance and lower device charges compared to their Silicon counterparts which result in lower conduction and switching losses.

The series-stacked GaN switching module proposed in this dissertation is based on the GaN enhancement high electron mobility transistor. This devices have low on resistance and low device charges, nevertheless, they have low threshold voltage which make them susceptible to false turn-on cases. The cascade GaN transistor solves this problem by integrating a low voltage Silicon MOSFET in series with a high voltage GaN depletion mode transistor as the Silicon MOSFET controls the turn-on and turn-off operations of the cascode switch, hence, the threshold voltage of the cascode GaN switch is higher compared to the enhancement GaN transistor. A high voltage series-stacked module with cascade GaN transistor should be investigated as it can be a better for high power applications in harsh environments.

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Aug 2015-present	Energy Systems Research Laboratory (ESRL), Florida International University Graduate Research Assistant • Design of new dc-dc converters with wide voltage conversion ratios using GaN and SiC devices. (Power rating > 1kW, voltage ≤ 800V, frequency ≥ 100kHz)
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Cairo, Egypt Nov 2012 – Jan 2014	National Authority for Remote Sensing & Space Science (Egyptian Space Program) Power Electronics Engineer Responsible for: • Building MATLAB/SIMULINK modes to simulate the satellite power conditioning unit and its performance. • Designing the power conditioning unit (PCU) of the satellite (based on the Maximum Power Point Tracking (MPPT) topology and the Shunt Regulator Topology). • Building check-out equipment using LabVIEW and National Instruments hardware in order to test and verify

the durability and reliability of the different items of the power subsystem (battery chargers, MPPT controllers, shunt regulators, distributed DC-DC converters, and the communication with the satellite's on-board computer using SSP and MODBUS protocols).

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A.O.I. (Electronics Research Facility)
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- Building microcontroller and FPGA based devices for industrial automation and medical applications
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Skills

- 7+ years of hands-on experience in designing, and building various power electronic stages (DC/DC, DC/AC, AC/DC).
- Hands-on experience in high frequency power electronics design using wide bandgap devices (SiC & GaN (E-Mode and Cascode)).
- Hands-on experience in custom magnetic components design (ex: coupled inductors, HF transformers).
- Hands-on experience in multilayer (6 layers), high frequency, and high density PCB design using Altium Designer.
- Hands-on experience in designer mixed signal electronic circuits (analog + digital) for sensing and gate driving applications.
- Experience with simulation programs: Matlab/Simulink, PSIM, and LTspice.
- Proficiency with lab tools (Oscilloscopes, Network analyzers, Signal Generators etc.).
- Good knowledge of control theory
- 5+ years of hands-on experience in embedded systems developments (using C2000 dsp, ARM cortex M3/4, Microchip PIC and ATMEL AVR microcontrollers) using ANSI C
- Device driver development (using C language) for LCD, SPI, I2C, DMA, PWM, .. etc.
- Experience with high-speed communication interface