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FLORIDA INTERNATIONAL UNIVERSITY

Miami, Florida

MESOSCALE CERAMIC CYLINDRICAL ION TRAP MASS ANALYZERS FOR IN SITU SAMPLE ANALYSIS

A dissertation submitted in partial fulfillment of

the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

Patrick A. Roman

To: Dean John Volakis
College of Engineering and Computing

This dissertation, written by Patrick A. Roman, and entitled Mesoscale Ceramic Cylindrical Ion Trap Mass Analyzers for In Situ Sample Analysis, having been approved in respect to style and intellectual content, is referred to you for judgment.

We have read this dissertation and recommend that it be approved.

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Florida International University, 2019

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DEDICATION

For my Smart and Beautiful Explorers, Jessica, Gioia, and Allegra.

For my family and friends.

ACKNOWLEDGMENTS

Thanks are due to every, and anyone that has made a contribution to this effort in even the smallest manner, direct or otherwise, there are too many to mention, but all have made a difference.

Sincere thanks are due to my co-major advisors and committee, for the opportunity to do this work, and their willingness to embark on this journey with me, providing guidance throughout, but especially for the funding and resources needed to complete the project. Thanks to Dr. Shekhar Bhansali for his time and funds, without these investments this work would not have been possible. Many thanks to Dr. W. Kinzy Jones for sharing his knowledge and expertise in ceramics and additive material systems, many discussions, contacts, and generous support. Thanks to Dr. Nezih Pala and Dr. Grover Larkins for their many technical discussions regarding micro and nanofabrication, devices, and electronics, there are many devils in the details. To Dr. Piero Gardinali who runs the best advanced mass spectrometry class there is, thanks very much for sharing enthusiasm for the technology and practical advice. Thanks to Dr. Eric Cardiff for his interest, understanding, and support of this work to move it forward. Much appreciation is due to Dr. Satheesh Bojja Venkatakrishnan who lent his time and expertise in pursuit of the spectrum, thank you! To all of the industry partners and others that have contributed, David J Manura, Ali Karbasi, Greg Norsworthy, Mike Newton, Xudong Chen, Evan Krumheuer, Neal Ricks, Rick Zicarelli, and others, thanks for your support. To my AMERI colleagues and the FIU College of Engineering and Computing, thanks so much for the resources, infrastructure, and support throughout this effort.

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ABSTRACT OF THE DISSERTATION

MESOSCALE CERAMIC CYLINDRICAL ION TRAP MASS ANALYZERS FOR IN SITU SAMPLE ANALYSIS

bv

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Florida International University, 2019

Miami, Florida

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As wireless network devices and IOT connectivity develop, the application and demand for small, low power, in situ sensors and instruments will expand. There are continuous efforts in the miniaturization of sensors and scientific instrument systems for conventional to field deployable and rugged hand held units for personal use to extreme harsh environment applications. This work investigates mesoscale cylindrical ion trap (CIT) mass analyzer design and the benefits of CITs realized via additive manufactured metalized ceramic material systems for improved ion signal, low power performance, and extended dynamic range. Rugged monolithic miniature mass spectrometer ceramic CIT chips have been produced that have increased signal output with reduced power consumption. We have demonstrated via simulation and experiment ~80% and greater CIT ion detection efficiency, signal improvement of the percentage of analyzed ions

detected, from 50% detection for conventional CIT designs. Utilizing a unique notched ring electrode design that increases the ion signal output to the detector, the electron ionization quantity and power required for mass spectrum generation and tuning was reduced by ~1 watt or 33%, as well as the required gain of the ion detector. Increased CIT ion detection efficiency effectively increases the total amount of the sample analyzed versus what is lost, thus increasing the instrument sensitivity and data collected, reducing duty cycle and power. Identical CITs of a ring electrode radius, ro = 1 mm, were fabricated from low temperature co-fired ceramic (LTCC) and the stainless steel (SS) for performance comparison and were tested in mass instability scanning and resonance ejection modes to produce Perfluorotribuytlamine (PFTBA) mass spectra. The ceramic material system offers design an Fd material benefits which reduce the CIT power consumption by 29x from ~10.20 mW power consumption of the stainless steel CIT design to 0.36 mW for the ceramic CIT, as well as enabling batch fabrication, reduced cost and manufacturing defects. While the stated design and material system benefits may facilitate CIT and MS system miniaturization, and the production of the ceramic CIT chip, the proof of concept of CIT ion ejection efficiency via the notched ring electrode may enhance ion trap designs at any scale.

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LIST OF SYMBOLS

SYMBOL NAME

 Ω Omega

um Micron

Da Dalton

Vrf Radio frequency voltage

KV Kilovolt

eV Electron volt

mbar Millibar

MHz MegaHertz

mW Milliwatt

 Ω/\Box Ohms per square

k Dielectric constant

ε Permittivity of free space

C Capacitance

qz Mass ejection value

ro Horizontal CIT radius

zo Vertical CIT radius

P Power

Q Quality factor

LIST OF ACRONYMS AND ABBREVIATIONS

MS Mass Spectrometry

QMS Quadrupole Mass Spectrometer

QIT Quadrupole Ion Trap

CIT Cylindrical Ion Trap

ITMS Ion Trap Mass Spectrometer

LIT Linear Ion Trap

RIT Rectilinear Ion Trap

TIT Toroidal Ion Trap

HIT Halo Ion Trap

LTCC Low Temperature Co-fired Ceramics

MEMS Micro Electro Mechanical Systems

El Electron Impact Ionization

GC Gas Chromatography

MSⁿ Tandem Mass Spectrometry

HPMS High Pressure Mass Spectrometry

SIP System in Package

ITIP Ion Trap in Package

MSIP Mass Spectrometer in Package

FWHM Full width half maximum

PFTBA Perfluorotributylamine

SOA State of the art

CHAPTER 1

1.0 INTRODUCTION

Mass spectrometry (MS) is a highly selective and sensitive method of chemical composition analysis and has a vast array of applications. These include, petroleum research, planetary science, forensics, industrial processing, military and law enforcement, first responder, drone deployment, drug testing, proteomics, shipping and marine, health care diagnostics, and environmental testing, to name a few [1-4]. Historically being limited to laboratory use given instrument size and power requirements, MS is steadily moving from the laboratory to the field for new and wide application through instrument miniaturization. Portable and probe MS instruments are enabling new discoveries through in situ application and new ground breaking methods of sampling and analysis. Recently there have been many contributions to mass spectrometer miniaturization driven by select and growing industries to enable pervasive in situ sample analysis [2-4]. For example, the Rosetta space mission, which deployed the Philae lander on comet Churyumov-Gerasimenko ('67P') was deployed with the Ptolemy ion trap mass spectrometer to analyze volatile organics, thought to be the seed molecules for the formation of the solar system in the field of Astrobiology. The Ptolemy spaceflight GC/MS ion trap mass spectrometer (ITMS) weighs 4.5 kg (9.92) lbs.), consumes 10 watts of electrical power, and has a mass range of 10 Daltons (Da) – 140 Da. Although a compact and efficient instrument, a suite of smaller individual (ITMS) instruments with reduced resource consumption, but with the same analysis performance, could provide redundancy as well as increased and varied analysis capability to maximize science data return within the same total payload size, mass, and power budget as the original singular instrument. In this vein there has been significant interest in the

development of miniaturized mass spectrometer instruments in many forms [5]. Most promising for MS miniaturization has been the ITMS for its flexible mass analysis capabilities and varied geometries, for which many designs facilitate a wide range of fabrication and material methods for realization [6-9]. Given its ability to "trap" ions or hold them in place for extended time periods, transfer, scan for mass analysis, perform ion reactions, or trap ions of interest within a group for analysis, as well as perform subsequent MS analysis of preselected ions via multiple ion traps in series, i.e. tandem MSⁿ, places the ion trap unique among mass analyzers [1, 10, 11]. Furthermore, miniaturized planar ion trap designs facilitate very short ion flight paths from the center of the trap to the detector and can operate at high frequency, enabling these ion traps to be operated at pressures in the millitorr range achieving high pressure mass spectrometry (HPMS), while maintaining a sufficient ion mean free path for feasible mass analysis [12, 13]. These features are of major importance for moving MS from the laboratory to the field, as the vacuum and ion detector requirements for traditional MS, ~1.0E-6 Torr, have been significant limiting factors for MS instrument system miniaturization.

Since the invention of the ion trap mass spectrometer by Wolfgang Paul et al in 1954, and their award of the Nobel prize in physics in 1989, there have been many advancements of its quadrupole form from the original hyperbolic geometry. These advancements focus on three main factors: first, improved ion trap performance with geometry optimization; second, increased ion trapping capacity and analysis; and third, materials and methods to enable new designs and their miniaturization [1, 9, 11]. With ITMS miniaturization comes a reduction in instrument and component scale resulting in increased difficulty of manufacturing and often performance tradeoffs [6, 14].

Miniaturizing ITMS analyzers from 1.0E-2 meters to 1.0E-3 meters, and even 1.0E-6 meters

can be prohibitive to certain analyzer geometries and manufacturing technology methods [15, 16]. ITMS performance tradeoffs can mean reduced mass range and resolution from scaling down, voltage breakdown from smaller component gaps and sharp edges, and instrument integration issues from multiple fabrication technology methods. Given the performance tradeoffs, the results of ion trap miniaturization often outweigh the tradeoffs for certain applications where size, weight, and power are limited, but a miniaturized ITMS may still perform the task. The Paul ion trap hyperbolic electrode geometries miniaturize with greater difficulty below 1.0E-2 meters while other ITMS designs have shown promise for the miniaturization of (ITMS) instruments, these include cylindrical ion traps (CIT), linear ion traps (LIT), rectilinear ion traps (RIT), and Halo ion traps (HIT) [17] [18-20] [8, 21-23]. What enables the miniaturization of the ITMS to the 1.0E-3 meter scale and below in these designs is the creation of the equipotential trapping well via quadrupole electrostatic fields by *planar electrodes* versus precision machined three dimensional curved surfaces. This provides the possibility to move to meso and microscale materials and methods for planar fabrication of highly miniaturized precision ITMS instruments. Many groups have investigated miniaturized CIT, LIT, RIT, and HIT, mass analyzers produced through miniaturized machine tool methods, 3D printing, metalized substrates, and microfabrication. CIT MS developments by Badman et al demonstrate the feasibility of the planar electrode CIT versus the hyperbolic ion trap geometry and helped to pave the way for future ion trap miniaturization efforts in this vein [21, 22, 24, 25]. While planar electrode design methods enable ion trap miniaturization, material systems can play an important role in development. The current miniature CIT standard is a mesoscale CIT assembly of metal plate planar electrodes with isolating films and is used in industrial and military applications [21, 26]. Moving down in scale, microfabricated CITs have been demonstrated with micron scale

precision, a desired feature while reducing scale, and in large arrays to regain trapping capacity [6, 14]. However, micron scale thin films and insulators constructing large area electrodes can lead to elevated power consumption and electrical breakdown, thus limiting their performance and application.

This research investigates mesoscale cylindrical ion traps with modified ring electrode geometry fabricated using microelectronic packaging materials and methods.

Novel mesoscale metallized ceramic CIT mass analyzer chips with planar electrodes were produced for improved power, electrical breakdown, and ion detection performance to further the progression of miniaturized mass spectrometer application in the field.

1.1 Motivation

The goal of this research was to investigate mesoscale cylindrical ion trap mass analyzer performance optimization through geometry and additive ceramic material systems. Achieving this goal could provide CITs with unit resolution < 1 Da and improved sensitivity, reduced power consumption, and operational durability for further integration and development toward microsystem mass spectrometer instrument systems or "instrument system in a package" (ISIP) for in situ sample analysis.

To address this goal the following were investigated:

i. CIT resolution < 1 Da: CIT geometry has a significant impact on trap performance and mass resolution. Using an optimized CIT design by Wu et al, an additive ceramic material and manufacturing system offers CIT performance benefits. A comparison of stainless steel CITs (standard) versus additive ceramic of the same design to assess ceramic material system CIT performance.

- ii. Ion detection efficient CITs: As half of all ions in a trap are lost due to oscillating ejection, improved ion detection efficiency may be enabled through notching the CIT ring electrode, providing greater ion ejection toward the ion detector.
- iii. Reduced CIT power consumption: Miniaturized device power use is a significant issue, often determining the potential for new applications. CIT power consumption may be reduced using ceramic additive manufacturing methods to design and fabricate ceramic CITs with minimal capacitance compared to conventional CITs with stacked parallel plate and insulator geometries.
- iv. Operationally stable CITs: Robust monolithic CIT device structure with stable performance through inert ceramic construction. Ceramic additive manufacturing material systems enable enhanced CIT performance stability and range as internal CIT plates have ~40 micron radii on all edges versus sharp machined or plasma etched features. This reduces the potential for internal arcing and plasma generation within the ion trap and extends the CIT high voltage mass scanning range.

1.2 Scope of Dissertation

Chapter 1 is the introduction and literature review, covering mass spectrometer miniaturization, the benefits and short comings, as well as ion trap theory, CIT background, the state of the art, and areas for advancement.

Chapter 2 presents ion trap simulation and analysis, as well as instrument design and operation simulations.

Chapter 3 outlines CIT design, fabrication, and materials used for the devices produced in this research, both conventional stainless steel and new ceramic additive manufacturing material systems.

Chapter 4 covers experimentation. The experimental setup is reviewed in detail as well as the methods used to test and asses the performance of the designed and fabricated CITs, both stainless steel and ceramic. Specific performance results of interest are mass range and resolution of generated mass spectra, as well as device ion detection efficiency, power consumption, and electrode voltage breakdown.

Chapter 5 discusses the results and discussion of the experimentation for both stainless steel and ceramic CITs. Sections 5.1 and 5.2 present CIT mass resolution performance, while section 5.3, 5.4, and 5.5 discuss CIT ion detection efficiency, power consumption, and electromechanical properties respectively.

Chapter 6 provides a summary of the research and future directions of the work.

1.3 Literature Review

1.3.1 Miniaturized Mass Spectrometers

Mass spectrometry has been a bench mark analysis method in scientific and industrial research for decades due to its highly sensitive and selective chemical analysis capability. Through instrument miniaturization mass spectrometry is moving from the laboratory to the field for wide application and discovery. Initial mass spectrometer instrument developments were made by Physicists and Chemists (J.J. Thompson, F.W. Aston, A.J. Dempster, K.T. Bainbridge) in the early twentieth century through isotope separation and the pursuit of determining atomic mass [1, 27]. These instruments were basic by today's standards and suffered numerous technological limitations of the period.

However, the significance of these early developments for instrumentation and scientific discovery cannot be overstated. Further advancements came in the 1950's as detection electronics and vacuum technology improved, and with mass spectrometer instrument commercialization, enabling broad application and new discoveries in the fields of chemistry, biology, and geology [1, 27]. As mass spectrometer instruments have developed and improved, experiencing new application, these instruments have been limited to laboratory use given their size and power requirements. In this context, sample analysis is only possible through sample acquisition in the field or laboratory, with analysis only conducted in the laboratory, creating numerous sample collection and analysis issues, as well as delays in obtaining analysis results. Similar to the pace of early instrument developments from commercialization, there has been great progress and recent improvements in mass spectrometer miniaturization driven by select industries to enable in situ sample analysis through technology development [3, 26, 28]. Miniaturized mass spectrometers are moving to smaller hand held devices, wearable networked IOT capable, and aim to provide in situ sample chemical analysis for new discoveries and applications such as, clinical diagnostics and wearable health monitoring, environmental/shipping monitoring and early warning, industrial and high-temperature process monitoring, subterranean drilling investigations, underwater research, planetary research, drug and forensics analysis, as well as first responder and battlefield applications.

Over the last twenty years great progress in mass spectrometer miniaturization has been made in conjunction with advancements in the semiconductor industry through new and improved electronic devices, increased computing power, as well as microfabrication and electronic packaging methods. Table I shows numerous miniature and micro scale MS instruments from various research groups displaying the trend in miniaturized mass

spectrometer instrumentation advancement [3, 13, 14, 26, 29-44]. The instruments listed employ a number of mass analysis methods for different applications and have varied levels of development. The instruments listed are driven by application; miniature spaceflight, portable, commercial, and micro scale devices. Descriptions of these instruments include estimated volume, the mass analyzer, and measurement performance [5]. The measurement performance listed for each was taken from the literature as reported, derived from mass spectra as m/ Δ m or Δ m (FWHM) at a given mass peak, or assumed to be unit resolution for a given mass range. The instrument size is listed in terms of an entire MS system, mass analyzer core, or chip based development to highlight the differences between the instruments and to show the trends in miniaturization. The table elucidates the technological path of mass spectrometer miniaturization over the years toward the realization of practical miniature instrument systems for in situ analysis as driven by mass analyzer physics. For example, TOF mass analyzer ion separation capability suffers greatly due to miniaturization as this method of mass separation capability improves with an increased flight tube length. Methods have been employed to regain performance, TOF drift regions have been folded to stack and increase the length for flight tubes and high speed electronics have been used for finer ion arrival time discrimination, all with great cost and diminishing return with respect to miniaturization. Later MS instrument miniaturization efforts employing the ion trap mass spectrometer have proven very successful [26, 31, 33]. This is mainly due the ion traps ability to trap and hold ions indefinitely, as well as a number of other qualities and key factors in ITMS design and operation. These include the ability to select and trap ions, scan selected masses for analysis, perform tandem MS analysis, power reduction with scale, and the simple and compact cylindrical ion trap design facilitating short ion detection path lengths and high pressure operation in the millitorr region [12, 13].

Table I. Compilation of miniature and micro scale mass spectrometers and their characteristics. 1 (LARTOF) Laser Ablation Reflectron Time of Flight, 2 (QMS) Quadrupole Mass Spectrometer, 3 (CATOF) Converging Annular Time of Flight, 4 (Wien) Wien Filter, 5 (LTOF) Linear Time of Flight, 6 (GTOF) Gated Time of Flight, 7 (CIT) Cylindrical Ion Trap

Research group	Instrument Type	Instrument size	Mass analyzer	Measurement performance
Rohner et al, 2004 [37]	Spaceflight miniature	Core ~ 339 cm ³	LARTOF ¹	$m/\Delta m = 600 \text{ (FWHM)}$
Orient et al, 2002 [36]	Spaceflight miniature	Core ~ 63cm ³	Paul Ion Trap	Range = $0 - 300$ Da m/ $\Delta m = 324$
Niemann et al, 2002 [35]	Spaceflight miniature	System ~ 11,167 cm ³	QMS ²	Range = $2 - 141$ Da $m/\Delta m = 141$
Mahaffy et al, 2008 [34]	Spaceflight miniature	Core ~ 628 cm ³	QMS	Range = $2 - 535$ Da m/ $\Delta m = 535$
Todd et al, 2004 [3]	Spaceflight miniature	System ~ 9075 cm ³	Paul Ion Trap	Range = 10 – 140Da
Brinckerhoff et al, 2001 [30]	Spaceflight miniature	Core ~ 578 cm ³	LARTOF	$m/\Delta m = 1000$
Kore Tech., 2019 [40]	Portable miniature	System ~ 24000 cm ³	CATOF ³	Range = $0 - 1000 \text{ Da}$
Bayspec, 2019 [29]	Benchtop portable	System ~ 52000 cm ³	LIT	Range = 70 – 650 Da
Microsaic Systems, 2019 [38]	Benchtop Portable	System ~ 46375 cm ³	Mems QMS	Range = 50 - 1400 Da $\Delta m = 0.7 \text{ m/z (FWHM)}$
Cooks et al, 2006- 2019 [33]	Portable miniature	System ~ 5000 cm ³	RIT	Range = 900 Th $\Delta m = 0.6$ Th (FWHM)
908 Devices, 2019 [31]	Portable miniature	System ~ 3168 cm ³	Micro CIT	Range = 55 – 400 Da
FLIR, 2019 [26]	Benchtop Portable	System ~ 129654 cm ³	CIT	Range = 35 - 425 Da
Velasquez-Garcia et al, 2007 [41]	Micro Scale device	Core ~ 9 cm ³ 30x0.56mm rods	Mems QMS	Range = 0 – 325 Da Δm = 36 at 69 Da (FWHM)
Taylor et al, 2001 [39]	Micro Scale device	25x0.5 mm rods	Mems QMS	$\Delta m = 3$ at 40 Da (FWHM)
Freidhoff et al, 1999 [32]	Micro Scale device	0.1 cm ³ chip	Wien ⁴	$\Delta m = 0.5$ at 65 Da (FWHM)
Yoon et al, 2002 [43]	Micro Scale device	0.1 cm ³ chip	LTOF ⁵	$\Delta m = 3$ at 43 Da (FWHM)
Wapelhorst et al, 2007 [42]	Micro Scale device	0.1 cm ³ chip	GTOF ⁶	$\Delta m = 3$ at 43 Da (FWHM)
Short et al, 2014 [14]	Micro Scale device	0.2 cm ³ chip	CIT ⁷	$\Delta m = 0.4$ at 42 Th (FWHM)
Ramsey et al, 2016 [13]	Micro Scale device	0.4 cm ³ assembly	CIT	$\Delta m = 1.2$ at 131 Da (FWHM)
This work, 2016	Mesoscale device	0.3 cm ³ chip	CIT	$\Delta m = 13$ at 69 (FWHM)

Initial efforts to miniaturization the Paul ion trap hyperbolic design proved difficult to manufacture with reduced scale and alternative ion trap designs were explored, with an emphasis toward simplified geometries. These include the cylindrical ion trap, first described by Langmiur in 1961, linear and rectilinear ion traps, toroidal, and halo ion traps. Each geometry offering new and unique ion analysis benefits, but with the major trend of increasing sensitivity with reduced ion trap scale. Of these designs, the cylindrical ion trap (CIT) is the most analogous to the Paul ion trap, figure 1.1, with the same general form, number of electrodes, relative trapping capacity and function. Due to its simplicity, ease of fabrication, and similarity to the Paul ion trap, the CIT has been a widely used mass analyzer in miniaturized mass spectrometer instruments to this day [26, 31].

1.3.2 Ion trap theory

The Paul ion trap or quadrupole ion trap (QIT) functions by creating an electric field equipotential well at its center for trapping ions, figure 1.1 [11]. This is accomplished through applied RF and DC voltages to central and end electrodes of the trap, respectively.

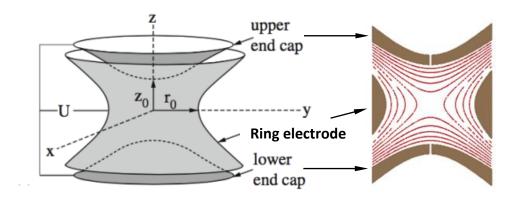


Figure 1.1. Paul ion trap geometry [45] and electrostatic field lines

As described by R.E. March et al, the general equation describing the electric field potential well of the ion trap and ion motion within is,

$$\emptyset = \frac{1}{2} (U - V \cos\Omega t) \left[\frac{x^2 + y^2 - 2z^2}{r_o^2} \right] + \left[\frac{U - V \cos\Omega t}{2} \right]$$
 (1)

with U representing the DC voltage, and V the RF voltage, applied to the end and central ring electrodes respectively [11]. The functional radius of the central ring electrode is r_o , and Ω is the frequency of the applied RF voltage. The relationship between the end electrode spacing and the central ring electrode radius is idealized when, figure 1.1,

$$r_o^2 = 2z_o^2 \tag{2}$$

Ions are trapped and oscillate along the central axis of the ion trap between the two endplate electrodes with the RF field. From the Laplace equation of electrostatics, the forces applied to ions of a given mass and charge is,

$$F = -e \cdot \nabla \emptyset = mA \tag{3}$$

This applied to equation (1) results in expressions for the ion trapping forces for each axis within the equipotential well, as shown below.

$$\left(\frac{m}{e}\right)x + \left(U - V\cos\Omega t\right)\frac{x}{r_o^2} = 0\tag{4}$$

$$\left(\frac{m}{e}\right)y + \left(U - V\cos\Omega t\right)\frac{y}{r_o^2} = 0\tag{5}$$

$$\left(\frac{m}{e}\right)z - 2(U - V\cos\Omega t)\frac{z}{r_o^2} = 0\tag{6}$$

As quadrupole ion traps are symmetric, x and y components maybe combined to form a radial component, $x^2 + y^2 = r^2$. Finally, the z component being negative as the ion motion is 180° out of phase with the r component ion motion. Each of these expressions is a form of the Mathieu equation,

$$\frac{d^2u}{dE^2} + (a_u + 2q_u \cos 2E) u = 0 \tag{7}$$

and for the ion trap,

$$u = x, y, z \tag{8}$$

$$\mathcal{E} = \frac{\Omega t}{2} \tag{9}$$

with the axial component being,

$$a_z = -2a_x = -2a_x = -\frac{16eU}{m(r_0^2 + 2z_0^2)\Omega^2}$$
 (10)

and the radial component,

$$q_z = -2q_x = -2q_y = \frac{8eV}{m(r_0^2 + 2z_0^2)\Omega^2}$$
 (11)

Equations (10) and (11) are the experimental equations of motion for trapped ions within the ion trap. Both a_z and q_z are the Mathieu parameters for the ion trap and represent ion motion stability or instability within the trap. This is depicted in the Mathieu diagram, figure 1.2, a family of curves covering the region where an ions motion is stable and remains trapped. Values for a_z and q_z must remain within this boundary region for ions to remain trapped. An ion trap operated in this mode, QIT mode, may trap ions for extended periods of time for ion separation, containment, and or reaction purposes. Finally, the QIT may be operated at a mass spectrometer (QITMS) in mass-selective ejection mode [10, 11]. In this mode, DC voltages on the trap endplates are held to zero volts, thus ion motion in a_z is minimal or nonexistent. However, the ion motion in q_z may be varied from 0 to 0.908, minimum to maximum instability, through increasing the force on the ions by ramping the RF voltage on the central ring electrode. Operating the QITMS in this mode initially traps ions of a predetermined mass range and then scans them out lowest to highest mass, orange to blue dots in figure 1.2 respectively, as their motion becomes unstable with increasing voltage, thus creating a mass spectrum.

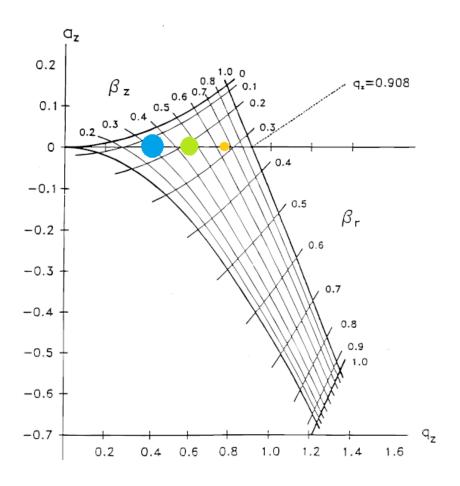


Figure 1.2. The Mathieu diagram depicting ion trap stability regions and mass instability scanning of low to high masses, yellow dot to blue [46]

1.3.3 Background and state of the art

As the cylindrical ion trap is analogous in performance to the Paul ion trap, a number of groups pursued research in its miniaturization toward the development of small portable MS instruments. The CIT was chosen for this reason as well as for its design simplicity and ease of fabrication, comparatively, and its analysis capability as an ion trap mass spectrometer. Of these research groups, Cooks et al lead the way in single millimeter scale CITs, parallel arrayed, and series MS/MS CIT research, then moving on to LIT and RIT development for MS miniaturization [18, 19, 21, 33]. Short et al focused

mainly on micro CIT arrays using MEMS and microfabrication technology [6, 7, 14]. Finally, Ramsey et al worked on meso and micro scale CITs, single and arrayed, as well as toroidal traps, all made in metal plate or silicon microfabrication technology [13, 47, 48].

The initial CIT MS work by Badman and Cooks demonstrated the comparable performance of the CIT to the standard hyperbolic ion trap design. Using a commercially available Finnigan ITMS modified to operate a CIT geometry of ro = 10mm, zo = 8.97mm, gap = 1mm, and producing mass spectra with $R = \sim 600$ Th with unit mass resolution [22]. Optimization of the CIT was also done to stretch the trap or increase the zo to reduce nonlinear field affects at the edges of the trap, improving mass resolution. Given the comparable performance of the CIT and the simplicity of the design and fabrication (stainless steel with polymer or ceramic spacers), CIT miniaturization was pursued using the same Finnigan ITMS test bed. A CIT of 1/64th the volume of the original commercial hyperbolic trap was produced, with geometry of ro = 2.5mm, zo = 2.88mm, gap = 1.25mm, and endplate hole = 1mm ϕ , with R~100da [21]. Although the CIT performance and resolution were lower than the previous CIT (ro = 10mm) investigation with scale reduction, a path for millimeter CIT miniaturization and optimization was created. With 1/64th trapping volume, the amount of analyte for analysis is greatly reduced, as well as the sensitivity of the instrument, a significant drawback of scale reduction [49]. Miniaturizing the CIT to the millimeter scale the authors found the device mean free path increases thus enabling higher pressure operation. An increase in CIT mass range and resolution was also reported, as well as a reduction in the RF voltage ramp required for ion ejection with trap miniaturization. Last, millimeter scale CITs were found to have less trapping volume relative to ion cloud size and energy spread, but with

an increase in the RF ramp voltage frequency the size of the ion cloud is reduced and centered in the trap, increasing resolution. These findings for single CITs are significant and position the ion trap as a leading candidate for mass spec on a chip microsystem devices. Follow on investigations by Cooks group included CIT arrays to overcome the obstacle of sensitivity loss with trap miniaturization and resulted in ion trap arrays producing increased ion sensitivity and comparable resolution, but having ionization difficulties given many traps over a large area [25]. First, CIT arrays of 4 and 10 traps with ro values or 2.5mm and 1.5mm respectively were fabricated in stainless steel with polymer spacers. Second, a CIT array was produced with varied ro values for mass analysis, 6mm to 2mm for mass selection, thus reducing the RF voltage ramping requirements by using the tap geometry instead, as well as increasing CIT sensitivity. The results of these works were CIT arrays with higher sensitivity than single CITs, increased resolution with increased RF frequency and decreased scanning speed, and a reduction in the mass ejection voltage required, as well as minor affects from array alignment fabrication errors [24, 25]. While this work proved the concept of arrayed CIT devices and the benefits, the Cooks group pursued other ion trap geometries and front end methods for ITMS miniaturization, such as linear ion traps (LIT) and rectilinear ion traps (RIT), where the trap geometry has an increased ionization cross section and trapping volume to aid in lost sensitivity with miniaturization [19, 33, 50].

Another effort to array ion traps utilizing microfabrication was done by Short et al for handheld devices [51]. Microfabrication technology offers a number of inherent capabilities for ion trap miniaturization given the micron scale working dimensions, materials, and processes. Their initial designs were 16x16 (256) CIT arrays in a 6mm²

and 7mm^2 chip formats. The CITs were of varied dimensions of ro = 100 um to 350 um, e.g. ro = 300um, zo = 356um (zo/ro = 1.186), and with an end plate hole diameter of 90um. The CIT arrays were fabricated from through etched silicon wafers using deep reactive ion etching (DRIE). Isolation of and between the plates was created with oxidation layers, while electrical conduction was done by selective metal deposition. Individual plates were wafer diced and selected for gold compression bonding to form the CIT chip arrays. The initial arrays had device capacitance values of 140pf to 350pf and was reduced by increasing the oxide isolation layer thickness. A follow on investigation integrated an ion source gas inlet method in silicon to increase internal trap ionization as well as a reduction in array capacitance through reduced area electrodes [52]. While these efforts showed promise in high pressure ionization and the reduction of the device capacitance, test results indicated charging of exposed area insulators, trap internal arcing, and plasma generation at an operating voltage RF = 150Vp-p. A third microfabrication run was done with 5x5 CIT arrays at ro = 360um, zo = 351um, and the end plate hole = 162um. Working off the last runs, these arrays utilized DRIE through wafer etching, silicon oxide and nitride insulating layers, and had capacitance levels ~ 200pf through additional oxide thickness. Device testing was done at RF = 100Vp-p at 5.5-6.5 Mhz over a mass range of 50-75 Da with R = 4-5 Da. Results showed limited operational mass range with lower voltage operation due device arcing and voltage breakdown [6]. A fourth run of silicon microfabrication was done using silicon on insulator (SOI) wafers as half stack CIT arrays for gold compression bonding [14]. This set was a more systematic approach to determine the optimal ro to zo ratio for CITs of ro = 350um. Utilizing SOI wafers with a buried oxide layer (box) of 10um to decrease device capacitance and voltage breakdown, ro diameter was varied with zo constant to obtain the optimal CIT resolution. Results show voltage breakdown to still be an issue and the device capacitance to be ~ 540pf, device performance was up to a mass range of 50 amu with R = 0.4 amu. Ramsey et al produced an open end ion trap array chip in polysilicon and silicon dioxide with 20um diameter individual traps, resulting in the detection of Xenon ion peaks with limited sensitivity due to the small trap diameter and device charging [48]. However, this work also discussed the relationships between trap operating pressure and voltage frequency with reduction in scale, eluding to the feasibility of high pressure mass spectrometry with ion traps. In theory silicon microfabrication technology has great promise as a method for producing micro ion trap array chips and potential toward micro mass spectrometer systems on a chip given the working scale and maturity of the technology. Unfortunately, there appear to be many material and design challenges with scale that have yet to be overcome to produce robust ion trap devices. Building off of their CIT miniaturization work and the work of Goeringer et al, the Ramsey group pursued ion trap operation at high pressures, above 100 mTorr, in an effort to reduce the pumping requirements of the instrument moving toward a hand held MS unit. While normal operating pressures for ion traps are detector limited to 1E-4 Torr, the Ramsey group was able to demonstrate unit mass resolution spectra at pressure levels of 1.2 Torr in the mass analyzer and 10 mTorr in the detection region, by increasing the RF voltage frequency and isolating the pressure regions of the analyzer and detector [12, 13]. This approach has drastically reduced the vacuum pumping requirements for the instrument enabling the production of the state of the art (SOA) hand portable units from 908 Devices, Inc. [31]. While the SOA technology has made significant advances in CIT MS instrument miniaturization, the CIT material

system may still be improved. The initial CIT work of Bhansali et al developed a miniature metalized ceramic CIT ring electrode using a low temperature co-fired ceramic (LTCC) material system, with the accompanying end plates made of stainless steel plates and fit into recessed areas of the ring electrode assembly to set the gap [7]. The LTCC CIT trap dimensions: ro = 1.375 mm, zo = 1.580 mm, Ep holes = 0.4125 mm, gap = 0.475 mm. This effort was the first ion trap with an LTCC ceramic component resulting in ion trap performance of 50 to 300 Da with R = 1.8 m/z (FWHM) showing the benefits of ceramics over silicon technology. Additional design and fabrication methods inherent in the LTCC additive manufacturing material system may be employed for improved CIT performance.

This study presents mesoscale cylindrical ion trap mass analyzer performance optimization through geometry and additive ceramic material systems for improved sensitivity, reduced power consumption, and operational durability for further integration and development toward microsystem mass spectrometer instrument systems or "instrument system in a package" (ISIP) for in situ sample analysis.

CHAPTER 2

2.0 CIT MASS ANALYZER SIMULATION

Ion trajectory modeling is a fundamental capability enabling mass spectrometer research and development. A number of pc based computer simulation packages have been developed for the field such as, ITSIM, SIMION, and LORENTZ, enabling instrument design and performance modeling [53]. Ion and electron optics may be designed or imported geometries with assigned or programmed variable magnetic or electrostatic voltage values. Charged particle initial conditions may be assigned as well as simulation programming and simulated data collection. While these ion trajectory simulators vary in capability and application, their ion trapping performance has been found comparable for collision free ion simulations and are useful tools in mass spectrometer and charged particle instrument research [54]. The charged particle optics simulator SIMION was used in this work to model CIT performance related to geometry, for affect and optimization, as well as CIT mass spectrometer instrument design.

2.1 Charged particle simulation – SIMION

SIMION is a symmetrical two and three dimensional ion optics charged particle simulator. Models are comprised of electrostatic and/or magnetic potential arrays defining boundary conditions from where the Laplace equation (12) is used to define the potential in space within the boundaries [53].

$$\nabla^2 V = \nabla \cdot \nabla V = 0 \tag{12}$$

Figure 2.1 is a cross section of a 3 dimensional CIT model of standard geometry produced in this work as well as a Paul ion trap. Both traps show the characteristic central equipotential "trapping" well. In the SIMION simulator, the trap structure, end plates and ring electrodes, are shown as potential arrays with defined boundary conditions or applied voltage. Using the Laplace equation SIMION calculates the electrostatic potential fields between electrodes (brown) as seen by the voltage contour lines (green or red) in the figure. At the very center of the CIT in the figure is the equipotential well where ions are trapped.

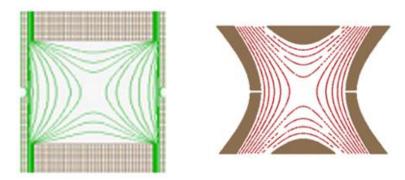


Figure 2.1. CIT and Paul ion trap SIMION simulated geometry

User defined geometry and charged particles are introduced into the model via the user interface, which enables fixed or programmable potential array simulations. Once charged particles are inserted in the model, single or in groups, the work of the simulation may begin. For this work a mass spectrometer instrument and a series of CIT simulation models were built using SIMION 8.1. The CIT models were designed to investigate and

approximate the ion trapping and ejection performance for the various material and fabrication based CIT geometries pursued. The main areas of interest of CIT performance simulation were the effects of geometry on the separation capability of the CIT, such as electrode shape, fabrication alignment, and ion detection efficiency. Finally, a mass spectrometer instrument simulation model was designed to aid in the design of the CIT instrument test bed, figure 2.2, and includes the three main sections of a mass spectrometer, (1) ionization source, (2) mass analyzer (CIT), (3) ion detector [1].

2.2 Mass Spectrometer Instrument Simulation

Project simulations were divided into two areas. Initial simulations were done to investigate the electron beam to CIT mass analyzer interaction under standard 70ev electron impact ionization conditions. The second area focused on the simulation of the CIT mass analyzer performance and various geometries of interest. The first set of simulations proved useful in guiding the electron gun and lens design for instrument operation, fabrication, and testing, and resulted in a feasible design/build as electron gun tuning and ion trapping conditions could be met at 70eV with the simulated geometry, figure 2.2.

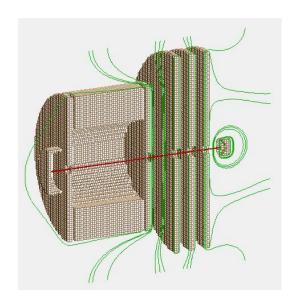


Figure 2.2. ITMS test bed instrument simulation geometry

2.3 Electron impact Ionization

The standard method of electron impact (EI) ionization was employed for neutral particle ionization for the instrument test bed. EI ionizes neutral particles through the removal of electrons in the outer electron orbits of the neutral particles [1]. Upon bombardment with electrons at 70eV to 120ev, outer shell electrons are removed and the particles have a resulting charge imbalance and become positively charged ions, which then may be manipulated in an electrostatic or magnetic field. Given the simplicity, ease of use of a thermionic source for electron generation and control, as well as the large established database of EI mass spectra for chemicals and materials, a thermionic electron ionization source was simulated for CIT internal ionization and test bed design purposes.

2.3.1 Varibeam thermionic electron gun

For simplicity and to facilitate CIT internal ionization an electron gun was designed and simulated which could meet a number of key elements in the MS test bed and CIT operation. First a focused electron beam of 70eV was desired for ionization that could have variable electron output and beam energy. This requires beam focusing electrodes; a special repeller, lenses, and a thermionic source, figure 2.3.

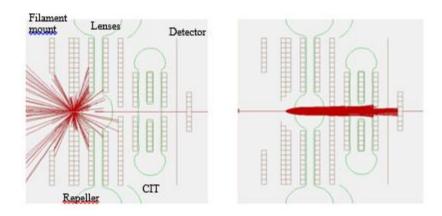


Figure 2.3. Simulated thermionic electron gun and CIT geometry at 70eV

In standard operation, the simulated gun in figure 2.3 has the electron filament boiling off electrons, left image, without focused trajectories (red). This case would provide minimal electrons for ionization and may be considered as having the electron gun (egun) off = no ions produced. The image to the right in figure 2.3 has focusing energy given to the electrons by applying 70eV to the filament, filament mount, repeller, and first lens to produce a well focused electron beam (red) at the desired 70eV energy level. While a slim well focused electron beam facilitates the testing of a single CIT, the second performance criteria of arrayed CIT testing was also desired. Through efficient design of the repeller

electrode and lenses, a slim or broad beam may be created by slightly varying the electrode voltages, figure 2.4. Based on these simulations this design was selected for fabrication.

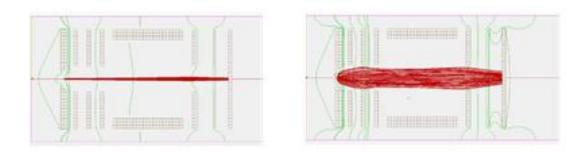


Figure 2.4. Varibeam electron gun electron beam simulations – slim and broad e beams

2.4 Ion trapping and ejection simulation

A model driven process was used to guide the design and testing of the ceramic CITs for this work. SIMION 8.1 provides and environment for geometry design, electrostatic field application, ion birthing, and ion path termination or "ion splat", as well as data collection. Models were designed to trap and eject ions in the standard mass instability scanning mode, where the ions of the smallest mass are ejected first and so on, figure 2.5. All simulations employed a viscoelastic dampening model with Helium (He) ions to approximate test bed conditions. Perfluorotribuytlamine N(C₄F₉)₃ (PFTBA), was the material of choice for simulation and testing. PFTBA is used as a calibration material in the mass spectrometer industry as it has characteristic peaks over a large mass range (0-600 Da). For the stated models ion trapping and ejection occurred as follows. First He ions and PFTBA ions we birthed in the center of the ion trap geometry while the model

applied the initial trapping RF voltage of 42 V 0-p at 2.0 MHz or 65 Da for the low mass cut off. As the first peak in PFTBA is at 69 Da, the full spectrum would be produced from this initial trapping and mass scanning voltage. The He ions give some initial collision to aid in PFTBA grouping. An RF frequency of 2.0 MHz was selected based on comparisons in the literature and for practicality do to each simulation run being 24 hours and increasing with frequency [21, 55].

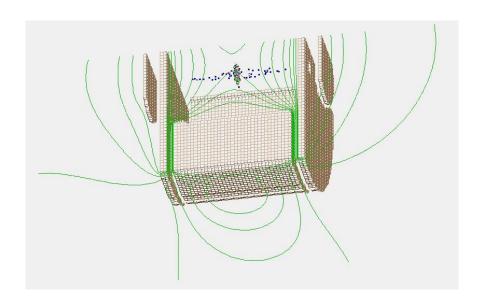


Figure 2.5. CIT trapping and mass ejection – SIMION 8.1

As the ions are birthed and trapped, the RF voltage is then ramped to eject the ions of least mass to highest mass, causing the ions to become unstable with increased energy and eject from the trap thus creating a simulated mass spectrum, figure 2.6.

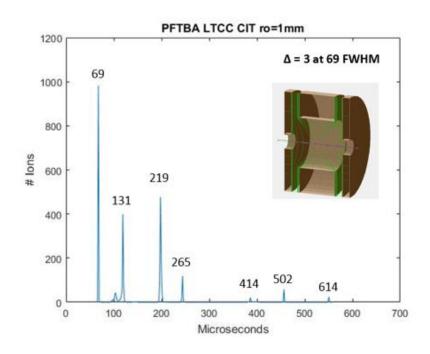
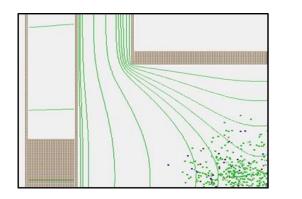


Figure 2.6. Ceramic CIT mass spectrum - PFTBA

2.5 CIT geometries

Various geometries were simulated investigating changes on the spectra performance of the mass analyzer. Sharp edge (4 um) stainless steel CITs versus rounded edge (40um) ceramic CITs displayed no difference in the spectra generated, figure 2.7. Deviating from the design geometry of Wu et al with reduced end plate gaps (-50um), had minor effect on mass range and resolution as related to trap scale and expanded trap geometry [11]. The most significant finding is the ion detection efficiency from the notched geometry and the effect on trap performance.



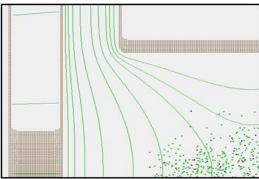


Figure 2.7. Stainless steel CIT (4um edge) and Ceramic CIT (40um edge) electrodes

2.6 Ion detection efficiency

CIT ion detection efficiency relates to the number of ions per duty cycle which are detected. In a standard ion source, mass analyzer, ion detector ITMS geometry, conventional CIT instrument designs eject only 50% of the ions separated toward the detector with the remainder ejected toward the ion source and lost. Thus, in these instruments approximately half of all ions analyzed are lost. Put another way, only half of the ion analysis data is being captured, therefore conventional CITs are 50% efficient in there analysis. Increased ion detection efficiency per cycle increases the number of analyzed ions detected, yielding more data per cycle and potential other benefits. Simulations have shown that a CIT with an increased ring electrode radius toward the detector side of the ITMS instrument allows ions to be ejected to the detector, versus the conventional constant radius CIT design, figure 2.8. Multiple simulation runs of CITs with increasing radii were done to plot this effect on ion ejection. Figure 2.9 shows the ions ejected toward the ionizing source in blue and the ions ejected toward the detector in yellow, with consistent ~80% and above ion ejection to the detector with a radius increase of 6% and higher. Experimental CIT designs were made with a ring electrode radius

increase of 25% to be well within the simulated ion ejection performance region and to enable practical fabrication.

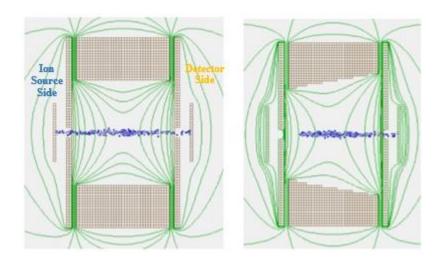


Figure 2.8. Standard and Notched CIT geometries with ion ejection depicted

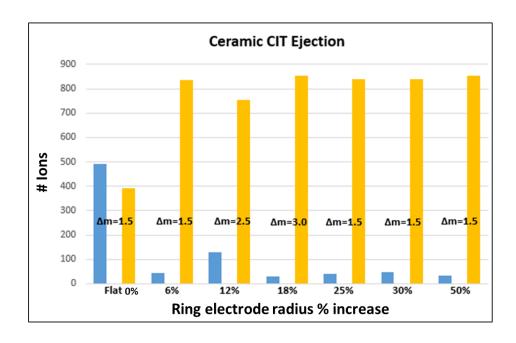


Figure 2.9. CIT ion ejection efficiency to detector with notched ring electrode

CHAPTER 3

3.0 MESOSCALE CYLINDRICAL ION TRAP DESIGN AND FABRICATION

Both conventional stainless steel and new ceramic materials and methods have been used to produce mesoscale cylindrical ion traps modeled after the Wu et al optimized CIT geometry [26, 44]. CITs on the mesoscale (100um to 5mm) offer a larger size ion trapping volume and increased sensitivity versus micro scale ion traps. A mesoscale CIT design realm was selected for this reason as well as for the compatibility with ceramic material system processing in an effort to show the benefits of this approach for CIT and miniature hand held mass spectrometer technology.

3.1 CIT design, fabrication, and materials

The efficiencies of reduced scale and new material systems are being used to investigate CITs devices for superior electrical and physical performance. A CIT has an internal volume formed by a hole in a plate with two opposing similar plates on either side. This geometry creates an equipotential region for trapping ions with an RF voltage applied to the ring electrode, figure 3.1.

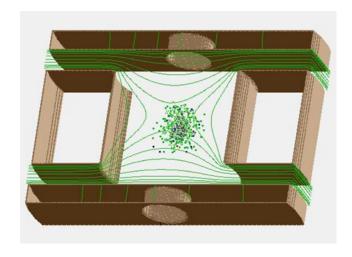
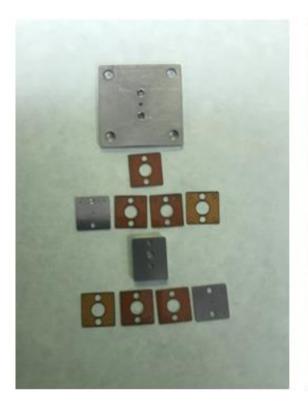


Figure 3.1. CIT simulation section – central plate ring and end plate electrodes

The conventional CIT is a parallel plate assembly of sheet insulators and stainless steel conductors, with limited downward scaling capability, higher power consumption, and cumbersome assembly alignment issues affecting performance. These items will be discussed as they relate to the instrument build and demonstrated performance.

3.2 Stainless Steel CIT

A series of stainless steel CITs were fabricated using conventional laser and CNC machining methods, figure 3.2. These traps had a ring electrode of 2 mm in diameter, (ro = 1 mm), and end plate holes of 0.6 mm, with a gap between these electrodes of 0.32 mm. This design follows the optimized CIT-2 design by Wu et al for reference. Initial material blanks were fabricated and prepared for CNC machining of the ring electrode, end plates, and their alignment holes. A fixture was designed to contain the CIT plates in an as assembled form to accept alignment hole drilling to maximize the potential for the best plate alignment in an effort to maximize CIT performance.



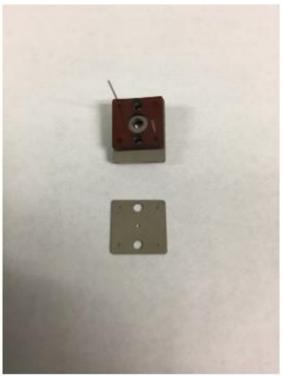


Figure 3.2. Stainless steel CIT components and assembled CIT with alignment pins

The insulating spacers that create the gap between the CIT ring electrode and end plates were laser machined from kapton sheet and stacked to form the required gap thickness. Figures 3.2 and 3.3 display the pre assembled components and the assembled stainless steel (SS) CIT that was used for reference performance measurements in this work.



Figure 3.3. SS CIT - Image of internal trapping region and components

Once the SS CIT was assembled and aligned, the CIT was fastened with two #0-80 PEEK screws which also fixed the CIT on to the test bed fixture plate, integrating the CIT with the electron gun, figures 3.4 and 2.3.



Figure 3.4. SS CIT integrated with test bed electron gun assembly

Best efforts were made at a clean and well aligned assembly process for the SS CIT, but proved difficult given the scale of the components and poor alignment markings, noted for future efforts.

3.3 Ceramic CIT publication

Patrick Roman, Xudong (Donny) Chen, W. Kinzy Jones, Ali Karbasi, C. Mike Newton, Travis Bates, Jacob Denkins, Shekhar Bhansali, "Additive Manufacturing Design and Fabrication of Ceramic Cylindrical Ion Trap Mass Analyzer Chips for Miniaturized Mass Spectrometer (IOT) Applications", JOURNAL OF MICROELECTRONICS AND ELECTRONIC PACKAGING, VOL. 13, pp. 113-120, 2016

Additive Manufacturing Design and Fabrication of Ceramic Cylindrical Ion Trap Mass Analyzer Chips for Miniaturized Mass Spectrometer Smart-Device (IOT) Applications

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3.3.1 Abstract

The current computing power and network capabilities of handheld smart-devices is helping to drive the development of new sensors; enabling the internet of things (IOT). A chip based mass spectrometer technology promises to offer a smart-device autonomous microsystem chemical analysis capability for sample determination and process monitoring for multiple applications in a small low power instrument package. This project focuses on the development of cylindrical ion trap mass analyzer chips fabricated using 3D Additive Manufacturing and planar Low Temperature Co-Fired Ceramic thick film processes toward the realization of a chip based mass spectrometer microsystem. The cylindrical ion trap (CIT) is a mass analyzer comprised of planar electrodes and operates by trapping and ejecting sample ions based on their mass in an RF field. Because of its simplicity CITs may be easily miniaturized and connected in tandem to achieve multiplexing. Additive manufacturing materials and methods enable enhanced trap miniaturization through micro machining and electrode patterning methods, fast and cost effective prototyping, batch fabrication, and material formulation flexibility. The current design incorporates three parallel ceramic plate metalized electrodes making up a singular trap geometry in a 10 mm² ceramic chip, forming a mass analyzer of reduced size, mass, and power, with enhanced material robustness for extended range use and in harsh environments. Unique processes have been developed to produce these devices which include conformal metallization layers, adhesion layers, ceramic paste formulations, sacrificial supporting materials, and co-firing methods. Additionally, 3D printing brings a unique design and fabrication capability enabling novel structures, material blending and

heterogeneous integration. With true digital control, the designs are easily scalable and shape agnostic.

3.3.2 Introduction

This article presents the application of Additive Manufacturing (AM) processes and their advantages in the development of ceramic mass analyzer chips for microsystem mass spectrometers. Miniaturized hand held and smart device based chemical analyzers can be powerful instruments for in situ sensing and remote monitoring. Mass spectrometry is a state of the art chemical analysis technique and much effort has been devoted to miniaturize these instruments given their selectivity and sensitivity [1]. Microsystem instrument applications may include, medical clinic diagnostics, normal and harsh environment monitoring, industrial and high temperature process monitoring, subterranean well investigation, underwater research, planetary research, low power wearable health monitoring, and web net based (IOT) chemical smart device node data collection, to name a few [2-4]. Cylindrical ion traps (CIT) are favorable for chip based mass analyzers as their geometry is based on planar layers that may be easily miniaturized [55]. While miniaturized CITs have been demonstrated using conventional metal plate and micro fabrication methods, these devices can be plagued by their delicate structures, high voltage breakdown, high capacitance, and power consumption issues [6, 7, 56]. These factors often limit instrument miniaturization, useable mass range, and deployable applications. Planar layer based ceramic AM techniques enable CIT miniaturization with similar scaling, but with added materials and process enhancements for improved performance CIT devices, and integration toward microsystem technology (MST) instrumentation. The advantages of AM

metalized ceramic CIT mass analyzers are low capacitance and low power RF operation, reduced arcing from internal geometries, a durable co-fired (850 C) ceramic structure, high temperature application, low cost batch fabrication, and material system compatibility for building integrated microsystem instruments.

The purpose of this work is to discuss miniaturized CITs designed and fabricated using Additive Manufacturing 3D printed Dupont 951 ceramic paste, metal inks, carbon pastes/films, as well as the Dupont 951 Low Temperature Co-fired Ceramic tape (LTCC) material system and to show the feasibility of this approach [57]. The motivation is a ceramic CIT chip based mass analyzer that could enable microsystem chemical analysis for future autonomous smart-device (IOT) applications in a small low power and low cost instrument package for more prolific chemical data acquisition.

3.3.3 Design

Cylindrical ion traps (CITs) operate by trapping ions in the center of an electrostatic potential well formed by a high frequency RF voltage in an electrode geometry Fig. 3.5 a&b [11].

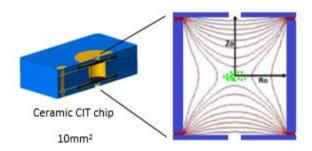


Fig. 3.5. (a) CIT section (b) Internal potential well

The CIT geometry is comprised of three parallel plate electrodes. The central ring electrode receiving the RF voltage, surrounded by two parallel end cap electrodes usually at ground potential, forming a dual capacitor as part of an oscillating LC tank circuit. Charged particles enter and exit the trap through concentric holes in these plates. Once ions are trapped they may be scanned out of the trap from low to high mass by increasing the RF voltage, thus generating a mass spectrum. The performance of CIT mass analysis using mass-selective instability scanning is determined by equation (1) [11].

$$m/z = 8V_{rf}/q_z\Omega^2(r_o^2 + 2z_o^2)$$
 (1)

Where m/z is the mass to charge ratio of the particle, V_{rf} is the trapping voltage, q_z is the mass ejection value, Ω is the V_{rf} frequency, and r_o and z_o are the horizontal and vertical radii of the CIT. Observing equation (1), m/z increases with increased scanning voltage V_{rf} . Decreasing horizontal and vertical radii of the CIT, Fig. 3.1b, reduces the V_{rf} needed for mass scanning. The highest mass analysis range of the CIT analyzer is desirable, but has miniaturization limits due to electrode arcing with increased scanning voltage. Further, from (2) we see CIT power required for mass analysis decreases by the square of the scanning voltage, a major enabling factor for smart-devices [56].

$$P = CV_{rf}^2 \Omega/Q \tag{2}$$

Where P is CIT power, C is the capacitance of the CIT, V_{rf} is the scanning voltage, Ω is the scanning voltage frequency, and Q is the quality factor of the oscillating LC tank circuit.

As a CIT is a parallel plate capacitor, more power savings may result from (3) [11].

$$C = k\varepsilon_0 A/d \tag{3}$$

By reducing the electrode area A and selecting the lowest dielectric constant k, with the permittivity of free space ε_0 and the gap d constant, CIT capacitance may be greatly reduced. Using these equations it is possible to optimize the miniaturized CIT chip design to maximize mass analysis range and reduce arcing and power consumption.

For this work we have selected a miniaturized CIT design based on CIT-2, by Wu et al, with dimensions scaled to $r_0 = 1$ mm, Table II, for AM design and fabrication development compatibility [55]. Our design approach using AM ceramic methods with cofired metalized ceramics has many advantages. First, device capacitance may be significantly reduced by minimized electrode area through 3D printing of metal inks on ceramic prints or screen printing the electrodes on LTCC tape, Fig. 3.7 a&b. Second, the design is a self-supporting structure utilizing vacuum as the dielectric between the CIT capacitor plates, thus enabling further reduction in device capacitance. *Third*, the CIT may operate in the kilovolt range as the co-firing process reduces sharp edges on the metal and ceramic layer electrodes for decreased arcing and produces a tough ceramic CIT chip, Fig. 3.8. Based on our design approach, calculated total CIT chip capacitance is 1.73pF. Finally, we see AM and material methods providing the means for improved performance CIT chip mass analyzers, miniaturized system components, and embedded circuitry for small low mass, and low power microsystems mass spectrometer instruments for smart-device (IOT) applications.

Table II – Ceramic CIT chip Dimensions

Design feature	Dimension (mm)	
End plate hole (ø)	0.60	
Ring electrode hole (ø)	2.00	
End plate thickness	0.30	
Gap thickness	0.32	
Ring electrode thickness	1.48	

3.3.4 Additive Manufacturing

A. CIT chip fabrication - LTCC Planar Tape Process

The Dupont 951 LTCC material system was selected for its miniaturized CIT fabrication compatibility, material properties, and MST capabilities. The LTCC material system enables the production of micron scale CIT devices within a 50 micron feature size, a major CIT miniaturization capability [57]. There is also the potential for the integration of additional micro mass spectrometer components on a common substrate for low power IOT MST instrument development. As the CIT chip application as an RF mass spectrometer device operating into the kilovolt range, and as a portable instrument, material properties become an important enabling factor. First, a durable and low outgassing material is desired to meet portable mass spectrometer requirements. Second, a low loss and high efficiency dielectric material is desired to reduce power losses and device voltage breakdown. Table III, lists these important and enabling LTCC material properties for the CIT application [57]. Dupont 951 was designed as a low loss RF and durable LTCC

material system yielding advantages over other potential materials for this application.

Table III – CIT enabling LTCC Material Properties

Fired Physical Properties	Dupont 951	
Shrinkage X,Y	12.7% +/- 0.3	
Shrinkage Z	15.0% +/- 0.5	
Young's Modulus	120 GPa	
Dielectric Constant	7.8 (10 GHz)	
Breakdown Voltage	>/= 1100 kV/25um	

The CIT chip is a three dimensional structure with internal voids and metalized geometries and has been designed to work with the Dupont 951 LTCC material system and a carbon sacrificial material. The LTCC tape design is made of laminated, individually drilled, and metalized component layers which are stacked and laminated to form the green CIT device, Fig. 3.6 and Fig 3.7b [57]. Finally, the stacked and laminated assembly is co-fired to produce the final chip, Fig 3.8. All green state design dimensions are oversized by ~ 14% to account for LTCC tape shrinkage in the co-firing process to yield the required dimensions for the final ceramic device.

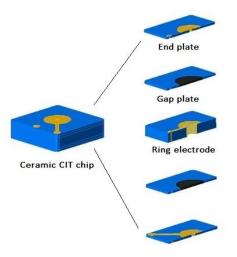


Fig. 3.6. Ceramic CIT assembly

The standard Dupont 951 LTCC fabrication processes, such as thermal compression lamination and normal metalizing methods were not readily compatible with CIT device design and were modified to fabricate the CIT chip. As the CIT chip is a 3D structure made by the addition of layers of LTCC, thermal compression lamination of the stacked device was not desired as it may cause material deformation, cracking, and movement of layers in the CIT device, thus changing the design geometry. To maintain the required CIT design dimensions, a low temperature and pressure lamination (LTPL) method was used, incorporating the organic adhesive (Honey) [58, 59]. Forming the internal parallel capacitor CIT electrodes, Fig. 3.7 a&b, a series of top and bottom metallizations connected by through hole sidewall metallization per layer are required, along with an interconnect via. To create these electrodes a unique metallization process was developed combining surface masking, vacuum assisted sidewall coating, and screen printing using Dupont 6142D silver conductor paste. First, component layer vias were masked with tape so as to expose only the via sidewalls for metallization. Second, the component layer was mounted on a vacuum chuck

and Dupont 6142D silver conductor paste, viscosity (180-270 Pa.S.), was drawn through the vias at a vacuum level of 648 Torr coating the sidewalls. The electrodes were completed using standard LTCC screen printing and baking processes.

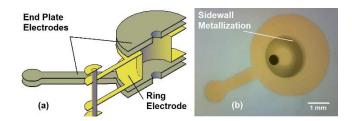


Fig. 3.7. (a) CIT electrode design, sectioned (b) Screen printed CIT ring electrode with side wall coverage

CIT chip LTCC fabrication consisted of the following processes:

Substrate layering – LTCC sheets of the needed thickness per component layer were cut to fit a 2" alignment fixture, allowing four CIT chips per substrate layer. These layers were then uniaxial laminated at 3000 psi at 75° C for 10 minutes.

Drilling – All substrate layers were drilled with a micro CNC milling machine to add alignment fixture and component layer hole and via features.

Inspection and Cleaning – Required post machining to verify and rid component layer holes of burrs.

Masking – Component layer holes masked top and bottom with office tape to facilitate metallization of sidewalls and via fills.

Via/hole metallization – Interconnect vias were filled using Hereaus TC7301 silver paste [18]. Hole sidewalls were metallized by mounting component layers on a vacuum chuck, drawing Dupont 6142D silver paste through.

Screenprinting – Electrode metallization using laser machined 230ss screens.

Baking – Metallized component layers dried in a box oven at 80° C for 20 minutes to dry electrodes pre stacking.

Stacking – Components layers coated with thin ~1mil squeegeed layer of honey and stacked in order of assembly. Laser machined carbon inserts from Thick Films

Technologies, Inc company used as sacrificial spacers in gap plates [60].

Lamination – Low temperature and pressure were used to conserve the structural dimensions of the stacked assembly. Using honey as the adhesive, a pressure of 50 psi was applied to the assembled stack in the alignment fixture to seat all component layers. A final box oven bake of 80° C for 20 minutes was done to solidify the layers and to reduce slippage.

Dicing – A micro CNC milling machine was used to dice the individual CIT chips in the green state.

Co-firing – The standard 3.5hr LTCC co-firing method with 10° C/min ramp settings were used to fire the CIT chips. Using a box furnace the organic binders were burnt out at 400° C for 1 hour. The carbon insert evaporated at 600° C, and the peak firing temperature was 850° C, held for 20 minutes, ending with a cool to room temperature producing the final devices, Fig. 3.8.

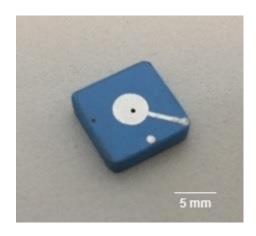
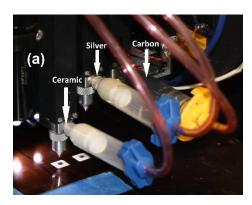


Fig. 3.8. Co-Fired LTCC CIT mass analyzer chip (10 mm²)

B. CIT chip fabrication - 3D Printing Process

The process to 3D print the ceramic CIT chip is straightforward using the nScrypt 3Dn-300 direct printing system [61]. 3D printing is a digital approach versus aligning and stacking ceramic green tape with vias and screen printed features. The device design to be printed can be generated using various CAD software packages. The output of the CAD is transferred into a script file using nScrypt software; this provides integrated, synchronous commands for the machine. There is no need for a screen, mask, or any other complicated process machinery. The nScrypt 3Dn-300 direct printing system is a digital manufacturing approach, enabling new designs, rapid prototyping, and rapid manufacturing through the integration of multi material design and material handling in a single machine. This combination facilitates complex process compatibility and can reduce material, machine, and maintenance costs. In addition, the maskless approach allows for a variety of new structures to be printed digitally. Precision XYZ motion allows for conformal printing, very high aspect ratio features, and the ability to dispense a wide range of very different materials

simultaneously. To start the process, a 3D CAD drawing of the CIT design was "sliced" into layers, with a separate drawing file for each layer. Within each layer, different materials and features are assigned to different printing heads, which are designated in the tool software. Since there are three different materials involved, a quad-head system with three SmartPumpTM100 was used, each material having a dedicated pump. Fig. 3.9 (a) shows the multi material nScrypt direct printing setup and (b) the SmartPumpTM100 schematic.



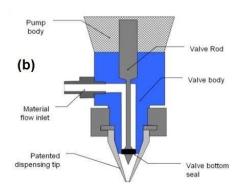


Fig. 3.9. (a) nScrypt Direct Printing Setup for CIT chip printing (b) SmartPumpTM100 schematic

When printing begins and material dispensing is initialized, the valve opens, which allows the material to flow through the pen tip onto the substrate, Fig 3.9 (b). To stop the

dispensing, the valve rod moves to a closed position that not only keeps a seal to the channel, but also maintains a negative pressure in the dispensing tip chamber to induce a reverse of the material flow. The valve opens and closes in a synchronized manner with the X and Y motion control. This allows the pattern to be printed in an X, Y plane and, if necessary, conformally in the Z plane. The linear print speed of X and Y may be as fast as 500mm/second on the nScrypt gantry system, and the resolution and repeatability of motion in all directions is within a few microns. In addition to the SmartPumpTM and the motion platform, a high resolution vision/camera system is also integrated for substrate alignment and real-time processing monitoring.

Three materials were used to print the CIT device. For the main structural component a custom ceramic paste was formulated using DuPont 951 ceramic powder and an in house sample of a proprietary noncommercial organic binder from Heraeus [62]. This allowed the paste to be formulated to meet the micron particle size and viscosity requirements of the nScrypt 3Dn-300 direct printing system to avoid nozzle clogging. The paste formulation process consisted of hand mixing the Dupont 951 powder with a solvent and the Heraeus binder. Next ball milling was done to grind the particles to a micron or less. Particle size was verified using a fineness of grind gauge. Additional mixing and viscosity adjustments were done using a Hoover Muller mixer. Commercially available carbon paste from Thick Film Technologies Inc company and silver conductive paste by Ferro company were used for the sacrificial and metallization materials [60, 63]. All materials used had a viscosity range of 60-120 Pa.S. and a solid loading of 70-80% per volume.

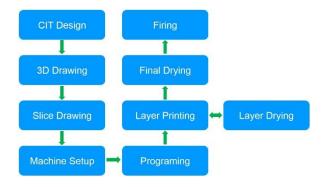


Fig. 3.10. Process Steps of 3D Direct Printing fabrication of the ceramic CIT chip

The processes of 3D printing the ceramic CIT chip are outlined in Fig. 3.10. The CIT design for the 3D printed device was set to 10 mm x 10 mm as the shrinkage behavior in the complex multi material system was unknown. A Kapton sheet was used as the base substrate for the direct print with digital camera fiducial alignment. To minimize cycle time a target thickness of 100 um per layer was selected. Each layer was comprised of at least two materials and were printed by switching the material print heads without interrupting CIT chip printing, Fig 3.11.

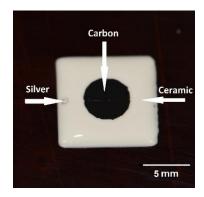


Fig. 3.11. Five initial layers of a CIT device with three materials in the printed state before drying

Drying each layer at 150°C for more than 15 minutes yields cracking throughout the print, therefore a reduced drying step of 150° C for 5 minutes was used between each printed layer

to maintain the structure and provide enough support to print subsequent layers. The final print in the green state was dried at 150° C for 60 minutes, followed by a standard LTCC co-firing process outlined previously, resulting in the device below, Fig. 3.12. The final 3D printed green state thickness was 4.1 mm and the fired thickness was 3.1 mm.

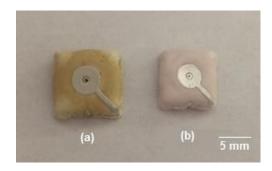


Fig. 3.12. 3D printed ceramic CIT chip (a) Green (b) Co-fired

Further development was done to prevent sidewall slumping of the ceramic paste, Fig. 3.12a, as it was not optimized in terms of rheology/viscosity and to hold the CIT device design dimensions. A fourth sacrificial material was used to build a rigid containment wall or tray around the device using white ABS nScrypt nFDTM to reduce slumping and maintain the device boundary dimensions, Fig. 3.13a. This tray was added to the ceramic device 3D print design for simultaneous printing. A 4th material pump was added and used to pattern the ABS material. Oven drying steps after each layer were not used in this case. A total of 30 material layers at 100 um thickness per layer were printed, with a 5 minute pause between layer prints to allow paste stabilization. The completed print was dried at 150° C for 60 minutes and fired at 850° C for 10 minutes driving off all binders

and burning the ABS support, resulting in the device below. The final (a) 3D printed green state thickness was 3.0 mm and the (b) fired thickness was 2.0 mm.

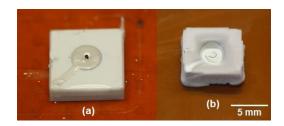


Fig. 3.13. 3D printed ceramic CIT chip with plastic wall (a) Green (b) Co-fired

3.3.5 Characterization and Testing

A CIT chip fabricated in LTCC tape was sectioned, and an optical microscope was used to determine the internal structure of the CIT, the gaps, and device layer thicknesses, Fig. 3.14. As seen below, the end plate layer (A), gap (B), and ring electrode (C), all have the correct structure, minus chipping and alignment artifacts due to the sectioning saw.

Sagging in the end plate layers is also minimal due to the use of sacrificial carbon inserts [60]. The vias and plate holes are clear and concentric, an important factor in creating a uniform potential well for trapping ions.

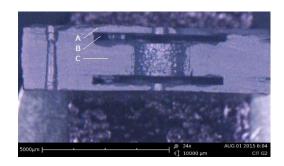


Fig. 3.14. Ceramic CIT section

Non-destructive X-ray imaging of the CIT chips was performed to verify internal device layer geometries and plate hole concentricity, a very important feature for CIT device potential well geometry. Exposed are flaws from the fabrication processes as well, such as, internal chipping, cracking, voids, material fusion, and delamination in the device, Fig. 3.15. X-ray imaging displays X and Y features of the CIT with relative intensity, where image brightness increases with material and thickness. This is a simple and very useful non-destructive technique for device characterization and prescreening of CIT chips for testing.

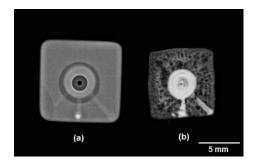


Fig. 3.15. Ceramic CIT X-ray images (a) LTCC tape CIT chip (b) 3D printed ceramic CIT chip

CIT chip design and fabrication was verified by electrode sheet resistance, continuity, and CIT capacitance measurements, as well as high vacuum (HV) testing. Sheet resistance and electrode continuity were done to verify electrode function as designed and to find any internal shorts between electrodes, resulting in device failure. Leads were added to the CIT chip to measure device capacitance. Finally, the CIT chip was integrated in a HV test setup, Fig. 3.16, to measure capacitance changes with vacuum pressure and to perform high voltage breakdown testing to determine the device maximum operating voltage at a common HV vacuum operational level for mass spectrometers.



Fig. 3.16. CIT chip mounted in HV test chamber

3.3.6 Results and Discussion

Using the Dupont LTCC tape and 3D direct ceramic print processes to fabricate the CIT chip device yield different results based on the maturity of the process technologies.

The Dupont 951 LTCC tape process yields functional CIT chip devices within 50um of designed dimensions; oversized by ~ 14% to account for co-firing shrinkage. Electrode sheet resistance was $8.5 \text{ m}\Omega/\Box$. Total CIT chip device capacitance measured in air was 2.2pF, reducing to 1.8pF in vacuum at 1.0E-6 Torr. The measured device

capacitance is 4% higher than the design value of 1.73pF and due to added lead capacitance in measuring. Electrical breakdown in vacuum at 1.0E-6 Torr occurred at 4kV, providing an extended voltage range for miniature CIT application. LTCC tape fabricated CIT chips have the desired geometric, mechanical, and electrical properties as designed for the CIT chip mass analyzer.

As a new development to 3D printing, multi-material direct prints with ceramic pastes, metal and sacrificial ink materials, have numerous challenges especially applied to the complex CIT chip design and scale. Process issues derive from multi material printing of low viscosity materials, material formulations, drying, and co-firing steps. Nozzle clogging may also be an issue, but can be resolved through additional ball milling of the ceramic powder used to make the ceramic paste. For the nScrypt 3Dn-300 direct printing system an average ceramic particle size of a micron or less is desirable. There was great difficulty in printing the ceramic CIT device due to material mixing, slumping, and dimensional changes during the drying process, Fig. 3.12a. The result was a CIT device without a well-defined boarder geometry in the green or fired states, Fig. 3.12 a & b. To remedy this issue an ABS tray was added to the CIT 3D print design to give a containment boundary to the printed layers which is burned off with co-firing, Fig. 3.13 a & b. In the green state the initial device print in Fig. 3.12 a appears to have a convex geometry from edge to edge, while the second device print in Fig. 3.12 b with the ABS boarder being flat from edge to edge. The convex versus flat CIT print results are most likely due to the binder drying process relative to exposed area for the material system. While the printed ABS boarder provides improved material control for the design geometry, the boarder may create problems in the final geometry with drying and co-firing, resulting in a

concave fired geometry, Fig. 3.13 b. CIT device thicknesses are listed in Table IV, both green state and co-fired thickness, with percent shrinkage. Varied thickness results are shown for the different material systems and 3D printing processes used to fabricate the same device design. The co-fired LTCC tape CIT device geometry was optimal of all the devices made, with thickness shrinkage results very close to the manufacturer's stated material performance of 15%.

Table IV – Ceramic CIT chip Shrinkage

CIT device	Green	Co-Fired	Chuinka aa (0/)
CIT device	Thickness (mm)	Thickness (mm)	Shrinkage (%)
LTCC Tape	2.80 mm	2.40 mm	14.3%
3D print	4.10 mm	3.10 mm	24.4%
3D print (abs)	3.00 mm	2.00 mm	33.3%

The shrinkage in the 3D printed co-fired devices appears to be dominated by the binder burnout and sintering kinetics. To facilitate 3D printing of the CIT materials high quantities of binders were used to make the material system flowable. The numerous printed materials with high quantity and differing binders for each presents printing, drying, and co-firing kinetics that may have undesirable effects on design geometry. As the materials are printed, there may be some dissolving of the previous layer and mixing of dissimilar materials. In the drying process, with different materials and varied device exposure area, layers will solidify and shrink at different rates. Finally, co-firing the

devices, the type and amount of binder is important to the sintering process [64]. As the amount of binder increases for a material, there is more binder to be removed during the binder burn out process, which may reduce particle packing and ultimately increase device shrinkage with firing. The large shrinkage results of 24.4% to 33.3% for the 3D printed devices appear to be due to the elevated levels of varied binders used. Based on this enhanced understanding the selection of a common binder for the material system is required for future 3D printed devices. X-ray imaging shows the internal and external quality of the co-fired ceramic CIT chips and fabrication processes relative to their design, Fig. 3.15a&b, as well as the effects of device shrinkage. The LTCC CIT chip displays defined internal electrodes, measurable features, concentric through holes, as well as a delamination flaw in the device lower left corner. The X-ray image of the co-fired 3D printed CIT chip shows varied material uniformity, less feature definition, distorted design geometry, and air voids within the device. The air voids, shown as black spots in the fired structure, are undesirable for this device and are a result of the large amounts of varied binders used. The difference in the co-fired size of the CIT devices in Fig. 3.15 is due to the LTCC CIT green state being oversized to 11.4 mm x 11.4 mm to account for shrinkage, while the 3D printed CIT green state size was 10 mm x 10 mm, as the shrinkage was unknown for the device material system.

3.3.7 Conclusions

The fabrication of an optimized mesoscale cylindrical ion trap mass analyzer design (CIT chip) was investigated using the Dupont 951 LTCC tape material system and 3D direct ceramic print technology to enable microsystem mass spectrometers for smart-device application. A functional CIT chip was fabricated with LTCC tape technology, while the new 3D direct ceramic printing method requires more materials development, but proves to be a fast and enabling approach. Some advantages of AM 3D printing over the LTCC tape process found in this investigation were the ability to have multiple processes and multiple materials in one machine, enabling new designs outside of planar layer processing capabilities, and material dispensing control with uniform process resolution on the micron scale. Other advantages included resource efficiencies due to reduced process machine and processing space requirements, as well as potentially higher device processing speeds and less material waste. Finally as AM technology advances complete IOT devices may be printed through component integration in a single 3D print.

Until then, the LTCC tape metalized ceramic technology enables great process development flexibility with fast and very low cost device development cycles and is the current method of choice for producing the CIT chip based on this work. New enabling process techniques developed were vacuum assisted sidewall metallization and reduced slippage organic adhesive lamination. Continued fabrication work will include the formulation of a common binder material system for 3D direct ceramic, metal, and sacrificial layer printing to address the device printing, drying, and firing shrinkage issues found in this work. The LTCC tape CIT chip process will also be developed to produce more and varied devices to test their mass analysis performance. Finally, the ceramic CIT

chip mass analyzer proved to have low capacitance (1.8pF) for application and very high voltage break down (4kV). Both lower power and higher voltage CIT chip performance in conjunction with AM material system compatibility should enable a new generation of miniaturized mass spectrometers for ground breaking (IOT) applications.

CHAPTER 4

4.0 EXPERIMENTATION

To fully test, assess, and compare the performance of the SS CIT and ceramic CIT devices a miniature mass spectrometer instrument and test bed are necessary. Mass analyzer operation and testing requires low vacuum, 1E-6 Torr to 3E-6 Torr, a method of sample analyte introduction and electrical interfacing with the instrument [7, 10, 11, 47]. Although this can be quite an undertaking, the benefits of custom system integration, testing flexibility, and control become apparent. Ion trap experiments were designed and conducted within the instrument test bed to provide clear output spectra and power consumption measurements for the instrument system and devices under test.

4.1 CIT instrument design

A miniature CIT instrument design was implemented to facilitate fabrication and testing of the CIT devices. The instrument design is comprised of three main regions, the electron ionization source, the mass analyzer, and the ion detector. A thermionic electron source enables the creation of ions internal to the CIT under test via electron impaction ionization [47]. The CIT mass analyzer traps and ejects ions based on increasing mass with increasing RF voltage. Finally, the ion detector or channel electron multiplier detects and amplifies the ion signal for the output of the instrument, creating a mass spectrum [65]. Figure 4.1 shows the designed and fabricated miniature mass spectrometer instrument with the three main regions described.

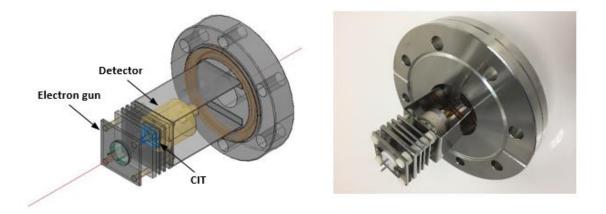


Figure 4.1. Miniature CIT instrument design and fabricated unit vacuum flange mounted

Aside from facilitating the three main components of the MS instrument, the design is also modular, where each main component is mounted on a plate for simple installation, position adjustment, and replacement. Position adjustment is important to approximate the as designed and simulated configuration. Figure 4.2 illustrates this point with ceramic CITs silver epoxied to the mounting plate.

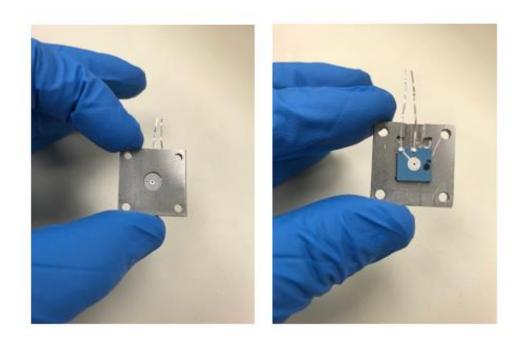


Figure 4.2. Front and back views of ceramic CIT mounting plate

Once the components were fully assembled and mounted, electrical connections were made. A series of AC and DC voltage signal connections ranging from 2Vp-p, -2 Kv, and 250 Vo-p at 2 MHz required connection. Given the variation in the signals and the very low Femtoamp output ion signal, great effort was made to extend shielding to the point of use of all signals to isolate signals and diminish noise. Figure 4.3 shows the final assembled miniature instrument ready for test with electrical connections and full shielding spot welded for termination. Materials used in the fabrication of the MS instrument were stainless steel, alumina ceramic, and PEEK; teflon coated cabling was used for all input and output signals.

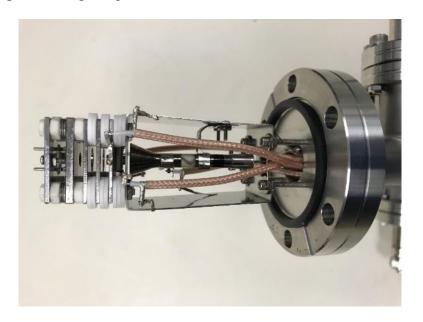


Figure 4.3. Miniature CIT mass spectrometer instrument ready for test

4.2 Experimental setup

For device testing a complete mass spectrometer test bed was constructed, figure 4.4. The goal of the test bed was to provide a relevant operational environment for CIT device operation and was comprised of a vacuum chamber with electrical feed through

flanges, pressure gauges, controlled analyte and gas leak valves, turbo molecular pump assembly, and an RGA QMS for reference mass spectrum and chamber conditioning monitoring.



Figure 4.4. CIT miniature mass spectrometer test bed – chamber & electronics

A more comprehensive understanding of the test bed system and its function may be gleaned from the block diagram in figure 4.5. Here, there are the three main elements, e gun, CIT, and detector, within the vacuum chamber at high vacuum, ~ 1.0E-7 Torr and above, with supporting vacuum pumps, pressure gauges, the sample input section and leak

valves, the system electronics, and the RGA. All required elements for CIT mass spectra generation. A typical experiment would include the following steps to produce a mass spectrum; recording of base pressure and reference RGA mass spectrum, setting the filament current for electron emission and filament bias for electron energy (70eV), and setting the pressure of the analyte leak to 1.0E-6 Torr. Once the analyte pressure is stable, the He buffer gas leak is set to a chamber pressure of 1.0E-3 Torr to stabilize. At this point a mass spectrum may be recorded. With the electronics warm and ready, the RF ramp, e gun and detector pulsing may begin, with the CEM output amplified and monitored by the pre amp and oscilloscope, generating mass spectra. Table V below is the test bed equipment list for this work.

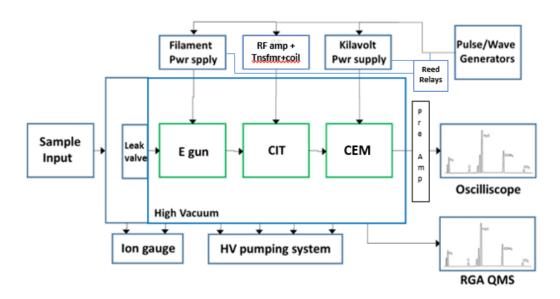


Figure 4.5. CIT miniature mass spectrometer test bed block diagram

Table V. CIT miniature mass spectrometer test bed equipment list

Component	Manufacturer	Model Number
Current Pre amp	SRS	SR570
Waveform Generator	Keysight	33600A
Waveform Generator	Keysight	33600A
DC Power Supply	Keysight	E36312A
DC Power Supply	HP	3612A
DC Power Supply	НР	E3631A
RF Amplifier	Minicircuits	LZY-22+
RGA	Extorr	XT300M

4.3 Electron gun

The CIT instrument test bed uses thermionic electron emission to create ions within the CIT under test. A focused beam of electrons is created by heating a standard tungsten SEM filament to emit electrons which are then focused at an energy of 70 eV for ionization [47]. Figure 4.6 shows the SEM filament and mounting plate as the first plate in the assembly from left to right. Next is the repeller electrode which has a counter sunk hole in which the tip of the SEM filament resides. This design feature allows for broad to narrow shaping of the electron beam. The next two electrodes are for electron focusing, with the fifth electrode being the CIT mount. Typical electrical levels for the e gun operation were a filament voltage of 1.65 vdc at 2.3A, with a filament bias of 70 eV, and a beam current of ~250 nA [47].

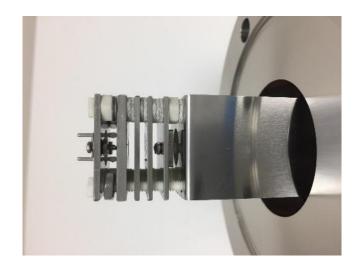


Figure 4.6. CIT instrument test bed thermionic electron gun assembly

4.4 Sample injection

Analyte injection to the test bed vacuum chamber was via a custom built heated tube inlet system, figure 4.7. Analytes were injected through a septum into a heated tube inlet, then introduced into the chamber via leak valve to the desired pressure for ionization. Helium and Nitrogen purge gases and a wet vacuum pump were used to purge and evacuate the injection inlet system with RGA validation.





Figure 4.7. CIT instrument test bed analyte injection system and septum injection port

4.5 Mass spectrum timing sequence

With the analyte and Helium buffer gas stable at the correct pressures; ionization, trapping, ejection, and detection for mass spectrum generation may be begin. To generate a mass spectrum with the CIT instrument testbed three main steps were required, figure 4.8. First, neutrals ionization at 70eV and trapping (A), second, mass ejection via RF voltage ramping (B), and third, ion detection (C). While ionization and trapping occur at the same time, so do mass ejection and detection. This a typical sequence for ion trap MS operation and the specific timing durations and duty cycles are shown in the system timing diagram, figure 4.8 below [8, 10, 11, 47]. A single duty cycle was programmed to last 100ms, figure 4.9 shows a screen shot of 5 duty cycles, the timing sequence, and spectra generated.

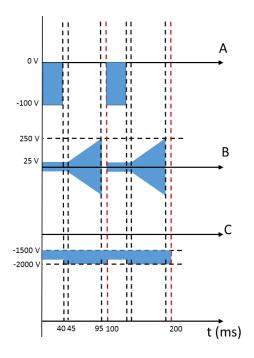


Figure 4.8. CIT instrument test bed timing diagram – 2 duty cycles



Figure 4.9. Oscilloscope image of CIT MS timing signals and mass spectrum

Key points for the timing sequence are that the detector be off while the electron beam is ionizing. Conversely, the electron beam is off when the CIT is ramping, ejecting ions, and the detector is on. This is required to achieve a good ion signal and to extend the life of the ion detector. The switching sequence was performed with two high voltage and high frequency reed relay circuits (NO/NC) that could be run via waveform generators in sync with the master ramping signal.

4.6 Ion ejection – MIS and RE

Ejection of the ions was accomplished by ramping the CIT voltage from the initial trapping voltage of 42 Vrf to 210 Vrf at 2.0 MHz. Operating the CIT in this manner is

referred to as mass instability scanning (MIS) as the ions become unstable and are ejected from the trap with increasing Vrf from low mass to high mass [11]. A voltage to mass range of 50 Da to 300 Da was selected to avoid background in the spectra, as well as to cover the range of the test bed RGA for PFTBA spectra comparison. A supplemental AC signal, 2.2 Vp-p at 1.0 MHz was applied to the end plate electrodes 180 degrees out phase to enable resonance ejection (RE), which aids in clustering the ions before ejection to improve spectrum resolution [47, 55]. All spectra were run and data collected in this operating mode.

4.7 Influence of He buffer gas

Helium was used as a buffer gas in the CIT instrument for viscoelastic dampening of the ion motion. This has the effect of grouping the ions relative to their mass and increasing the spectrum resolution [47, 53, 66]. As the atomic mass of Helium is 4 Da the buffer gas is not trapped and ejected, and does not appear in the mass spectrum.

4.8 Ion detection and spectrum generation

Ion detection was initially attempted using a faraday cup. This proved to be insufficient for generating spectra as the output ion signal is at the FemtoAmp current level, thus amplification is required. A channel electron multiplier (CEM) from DeTech was selected and installed in system for ion amplification [65]. The CEM operates by producing a cascade of secondary electrons for the initial ion impact and all subsequent electron impacts, resulting in a 10E7 gain level. The CEM has two operating modes, pulse counting and analog mode. Pulse counting mode is just that, each ion detected

results in an electron pulse at the output of the detector, but requires additional electronics to operate, e.g. a discriminator, etc. [67]. Figure 4.10 shows individual ion pulses from the CEM on an oscilloscope. The second mode is analog, where the amplified electron current from ion detection is amplified to create the mass spectrum, figure 4.11. Analog mode was used in this investigation.

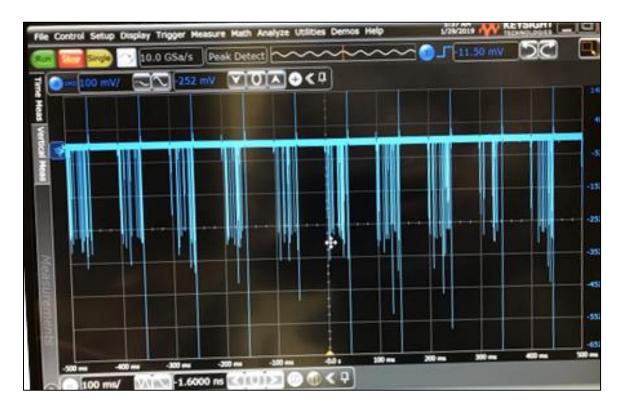


Figure 4.10. CEM ion pulses - individual ion pulse counting mode



Figure 4.11. CEM analog mode mass spectrum

4.9 Sample analyte Perfluorotributylamine (PFTBA)

The analyte of choice for testing the CIT instrument was PFTBA as this material is very stable and has characteristic peaks over a large mass range, figure 4.12 below.

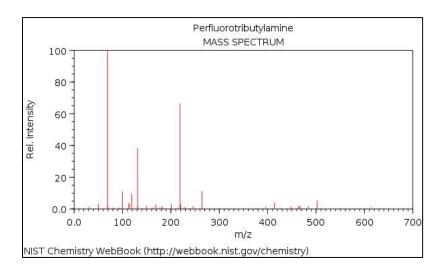


Figure 4.12. NIST EI mass spectrum of PFTBA

The mass range for CIT testing was from 50 Da to 300 Da, covering the most prominent peaks in the PFTBA spectrum for clear identification. PFTBA is color and odorless liquid for mass spectrometer calibration and was purchased from Scientific Instrument Systems (SIS) [68].

4.10 Reference mass spectra – Extorr RGA

As a reference instrument and to monitor the CIT test bed chamber conditions an Extorr residual gas analyzer (RGA) was installed in the chamber, figure 4.13 [69]. This enabled monitoring of the background gas levels and composition to determine if there was a leak in the system, residual water vapor, or malfunctions in the analyte injection system. The Extorr RGA is a small QMS which can measure 0 to 300 Da. The unit operates with a faraday cup detector at high pressures 1.0E-4 Torr and above and with an electron multiplier tube at low pressures 1.0E-6 Torr and below. The system comes with a software interface and can be setup to monitor a chamber or process automatically.

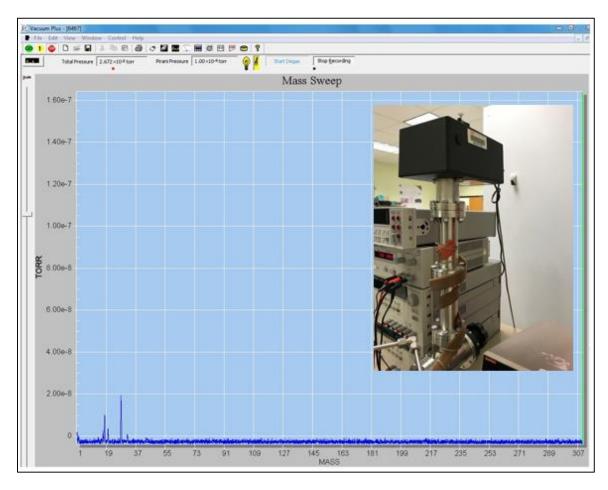


Figure 4.13. Extorr RGA (inset) and CIT test bed chamber background mass spectrum, H2O vapor and laboratory air

Before the beginning of a CIT experiment a mass spectrum of the chamber background would be taken to determine the cleanliness of the chamber. At low background levels, (water vapor, nitrogen, oxygen, argon, and CO2, the components of laboratory air), experiments could be performed.

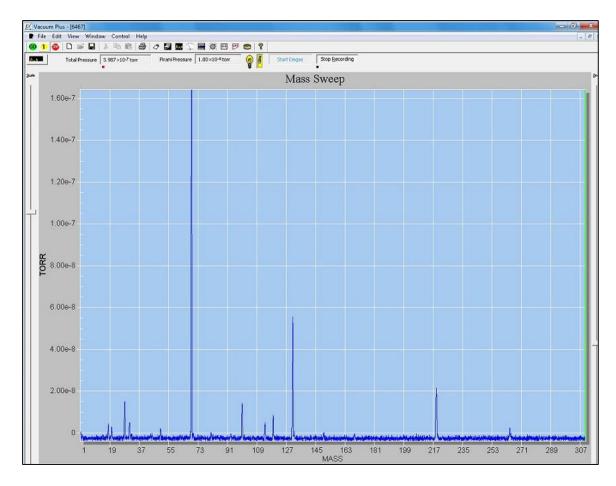


Figure 4.14. CIT test chamber RGA mass spectrum of PFTBA at 1.0E-6 Torr

To run a CIT experiment, PFTBA was leaked into the test chamber and stabilized at 1.0E-6 Torr, an RGA mass spectrum was taken before each experiment for reference, figure 4.14.

4.11 CIT power

Power consumption of the CIT devices under test is desired to compare and validate the ceramic versus stainless steel material systems for determining the most energy efficient device. Using a clamp on toroidal transformer (1:1000 P/S) on the RF

ramping voltage line of the CIT under test, device power consumption was calculated as a function the voltage drop across a 1 ohm shunt resistor, figure 4.15. This method gives a simple and robust solution for measuring the power needed to run the CIT devices.



Figure 4.15. Clamp on toroidal transformer power measurement circuit

4.12 CIT voltage breakdown

High voltage testing of the CITs was done under DC voltage conditions in a high vacuum chamber. The CITs were mounted on a vacuum flange and tested at 1.0E-6 Torr by raising the DC high voltage until failure; arcing or shorting. The higher the voltage at failure enables extended range performance or increased mass scanning for the CIT.

CHAPTER 5

5.0 RESULTS AND DISCUSSION

A multitude of experiments, device tests, and analysis were conducted to fully characterize CIT mass spectrum performance, structure, composition, and electrical performance. This was done to assess the benefits of the ceramic material system technology applied to CIT mass analyzers versus the conventional CIT and to investigate its use as a future platform for uMS instrument development. The traditional symmetric ring electrode CIT design was tested for the SS CIT and the notched ring electrode design for the ceramic CIT, as shown in figure 2.8.

5.1 Stainless steel CIT performance

The conventional CIT technology is a parallel plate assembly of insulators and stainless steel (SS) plates as shown in figure 3.2. As a reference, this device was operated at a PFTBA pressure of 1.0E-6 Torr with He at 1.0E-3 Torr as a buffer gas, and with MIS from 50 Vrf to 258 Vrf at 2.0 MHz, as well as RE at 2.2 Vp-p at 1.0 MHz. Ionization energy was 70 eV with a filament voltage of 1.65Vdc, with the CEM detector at -2 KV. The resulting mass spectrum performance was a peak width of 23 Da at 69 Da FWHM, with a mass range from 59 Da to 307 Da. Figure 5.1 is a "first device data" mass spectrum for the SS CIT and shows the basic PFTBA fragmentation pattern and relative abundance of the peaks similar to the standard in figure 4.12. Given the number of components making up the SS CIT, there is high potential for assembly alignment error which may add to peak broadening and mass shifts in the mass spectra due to ion ejection trajectory distortion from non-uniform electrostatic fields.

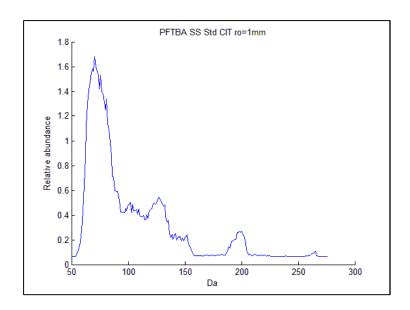


Figure 5.1. Stainless steel CIT, ro = 1mm - PFTBA mass spectrum

While the characteristic PFTBA peaks are apparent, device alignment error is estimated to be the cause of the wide peaks, see section 5.5.3, as well as the RF voltage frequency. The two most closely related works in the field by Chaudhary and Kornienko are of similar CIT size, with ro = 1.375 mm and 0.500 mm respectively, both having similar experimental designs, operation, and accepted results in the field for miniature CITs. The PFTBA spectrum results by Chaudhary and Kornienko resulted in peak widths of 1.8 Da at 69 Da FWHM [7, 47]. The main difference between the two experiments was the ramping RF voltage frequencies of 3.0 MHz by Chaudhary and 5.0 MHz of Kornienko. The increase in RF voltage frequency decreases ion orbit relative to trap size or CIT ring electrode radius, ro, within space charge limitations. This increase in ion bunching in the center of the CIT has been shown to decrease peak width or increase mass spectrum resolution, but with an increase in mass trapping and ejection voltages [11, 13, 46]. Last, the work by Patterson was a SS CIT of ro = 2.5 mm and operated at 2.0 MHz, with

PFTBA spectrum results at a peak width of 3.0 Da at 69 Da FWHM. Although the work of Patterson is very similar, the SS CIT is larger than this work and a large resonance ejection voltage (34V_{0-P}) was used to aid in mass ejection [8]. Of the works mentioned all are comparable in size, setup, and have very similar mass resolving performance at PFTBA 69 Da FWHM, but employ different techniques to achieve these results, e.g. increased Vrf frequency or resonance ejection at elevated voltage levels. Further, no mention is made of the effect of CIT alignment on mass spectrum peak width or CIT resolution. While this work is comparable to those previously mentioned, the PFTBA peak width of 23 Da at 69 Da FWHM is believed to be the result of CIT plate assembly misalignment, reduced RF voltage frequency, and or low voltage resonance ejection. All or some of the above should improve this result greatly.

5.2 Ceramic CIT performance

The first proof of concept of a full metalized ceramic material system notched CIT chip device, shown in figure 4.2, was tested to measure the device performance and generate mass spectra.

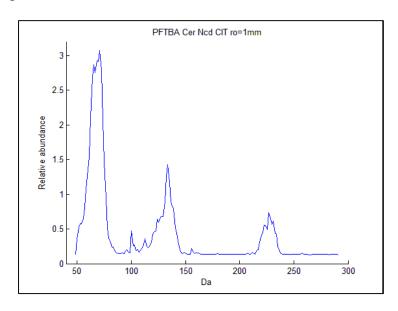


Figure 5.2. Notched Ceramic CIT, ro = 1mm - PFTBA mass spectrum

This device was operated at a PFTBA pressure of 1.0E-6 Torr with He at 1.0E-3 Torr as a buffer gas, and with MIS from 42 Vrf to 210 Vrf at 2.0 MHz, as well as RE at 2.2 Vp-p at 1.0 MHz. Ionization was at 70 eV with a <u>filament voltage of 1.20Vdc</u>, with the CEM detector at -1.88 KV. The resulting mass spectrum performance was a peak width of 13 Da at 69 Da FWHM, with a mass range from 50 Da to 250 Da, figure 5.2. Although, the peak width and mass values are improved versus the SS CIT, the peak widths are wide by mass spectrometry standards, but again are "first device data". Typical QMS and QIT instruments operate at peak width levels of 0.6 Da to 1.0 Da in the lab. The notched (Ncd) ceramic CIT being intended for a miniature portable device, peak widths of 1.0 Da to 2.0

or better are desired and may be achieved with improved CIT plate alignment and other methods previously mentioned.

The significance of this result is that it is the first mass spectrum of a complete CIT made in full co-fired metallized ceramic material system. Thus proving the concept of electronic packaging material systems for batch fabricated CIT chip device application to the field of miniature mass spectrometry [44].

5.3 Ceramic CIT ion detection efficiency

In this work, ion detection efficiency is defined as how efficient the mass analyzer is at ejecting ions toward the detector. Improved ion detection efficiency is inferred to have increased based on repeatable simulations with ~ 80% and above ion detection, figure 2.9, and reduced experimental CIT energy input and ion detector amplification results, table VI below.

Table VI. Input ionizing energy and ion amp levels for SS and Notched ceramic CITs

Device	Ionization filament Voltage (Vdc)	CEM detector Voltage (KV)	
SS CIT	1.65 V	- 2.0 KV	
Ncd Ceramic CIT	1.20 V	-1.88 KV	

For the SS CIT and the notched ceramic CIT all test conditions were identical, the only difference being the mass analyzer under test and the resulting ionizing energy and ion amplification required to produce the same mass spectrum. Each experiment was run with

the PFTBA analyte and Helium pressures being established, ion source and detector tuning, and final readout electronics tuning for best spectrum results. The notched ceramic CIT experiments, with a ring electrode larger on the detector side of the CIT, resulted in reduced ionizing energy input, nearly one watt less, as well as lower detector operating voltage or less ion amplification for the same experiment versus the SS CIT. Operating the notched ceramic CIT at the SS CIT tuned energy levels ~ 3W resulted in signal saturation, reducing the energy levels to 2.3W produced optimal operation and spectrum results for the notched ceramic CIT. It is this reduction in the required ionizing energy and ion amplification of the detector that demonstrates the increased ion detection efficiency of the notched ceramic CIT, with a power savings of nearly 1 watt for the tested instrument configuration. This is the first result demonstrating this concept, achieving ~ 80% of the analyzed ions at the detector versus only ~ 50% for conventional CIT technology [11]. It is believed this result will aid in improving the performance of miniaturized CIT instruments through increased sensitivity and reduced power consumption.

5.4 CIT power consumption

Power consumption is a performance parameter with great impact on miniaturized systems. As sensors and instruments are miniaturized their available supporting resources are also reduced, e.g. batteries and electronics. The power consumption of the SS CIT and notched ceramic CIT were measured under the same testing conditions, yielding different results, table VII, based on material selection and device design.

Table VII. CIT mass analyzer power consumption values

Device	Power consumption (mW)
SS CIT	10.20 mW
Notched Ceramic CIT	0.36 mW

The ceramic material system offers design and material benefits which reduce the CIT power consumption by a factor of 29x from ~10.20 mW power consumption of the stainless steel CIT design to 0.36 mW for the ceramic CIT. This power reduction comes from the use of the RF material system LTCC, reduced area electrodes, vacuum dielectric, and minimized capacitance design of the ceramic CIT versus the SS CIT [70]. Compared to conventional CIT previous works, design and materials, the LTCC material system offers superior design and low loss RF electronic properties enabling great power reduction for miniature CIT devices with the potential for extending field applications of these devices [8, 14, 26, 47].

5.5 CIT Electromechanical properties

5.5.1 Conducting and Insulating properties

The ceramic CIT is a radio frequency device operating in the range of 1.0 MHz to 10.0 MHz. Efficient device operation can be maximized through the selection of quality conductors and insulators designed for or compatible with operation at these frequencies. LTCC is a high Q material system; RF voltage oscillations are more efficient and less damped in LTCC [70]. This is achieved through the use of alumina/glass ceramic dielectric and silver (Ag) conductor electrodes [57]. Table VIII below lists the materials

used to construct the SS and ceramic CITs with their associated conductive and insulating properties.

Table VIII. CIT materials electrical properties

Material	Conductivity	Dielectric Const.	Bkdwn Volts	Loss tangent
Silver	6.3e7 S/m	na	na	na
Stainless steel	1.45e6 S/m	na	na	na
LTCC	Na	7.8	>44V/um	0.014
Kapton	Na	3.4	308V/um	0.007

A more conductive material system with a high quality factor such as LTCC provides a more efficient and lower power RF device. This work exploits these favorable electronic material properties for RF devices to optimize CIT performance.

5.5.2 Ceramic CIT Surface Profilometry

A contact profile scan of the ceramic CITs was performed to determine three main device characteristics; surface material roughness (Ag electrode and ceramic), electrode thickness, and sag. An Alpha-Step 200 was used to perform the scans. Surface roughness of the electrodes was a concern as it has been thought to have a negative effect on ion trap performance, mainly for traps on the micron scale [71]. Electrode thickness was measured to assess the durability of the electrodes for contact bonding. Last, a profile scan of the devices was done to determine the amount of sag of the devices due to the co-firing process. Figure 5.3 is a profile scan of the entire top surface of a ceramic CIT.

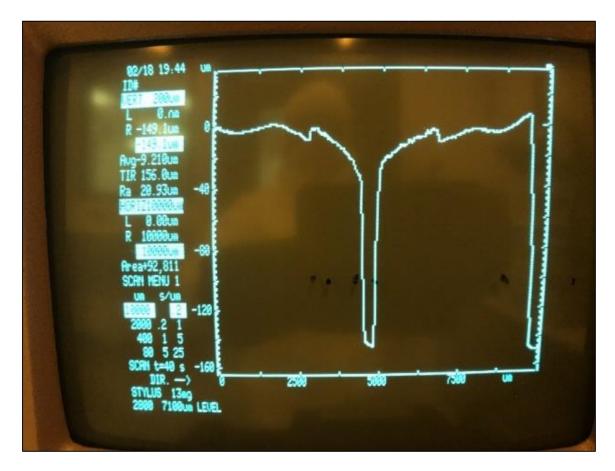


Figure 5.3. Alpha-Step 200 profile scan of the top surface of a ceramic CIT

The tested notched ceramic CIT has a measured sag of 60 um from top edge to center, which may be due to gravity during the co-firing process or buckling from the use of a Heraeus non-compatible via fill material [72]. The sag effectively reduces the internal gap between the CIT ring electrode and the end plate. The silver electrodes were measured to be 6 um thick, providing uniform coverage and a good bonding surface. Finally, the surface roughness for the electrodes and the ceramic surface measurements were Ra = 735 nm and Ra = 315 nm, respectively. While these roughness values are higher than what is achievable with silicon based CITs, they are comparable to the SS CITs and should not

adversely affect CIT performance at this scale, where as micron scale CITs may see an effect [14, 16, 48, 52].

5.5.3 Device alignment

CIT device assembly alignment was characterized to assess the effect on device performance. This was done during the assembly process of the SS CIT, as well as for the ceramic CIT post co-firing. As the plate alignment may have an adverse effect on the CIT ejection and spectrum resolution, an effort was made to benchmark the as built and tested device alignments. Figure 5.4, is the SS CIT with one end plate removed to display the internal structure of the device and to highlight the layered assembly of the plates and



Figure 5.4. SS CIT with end plate removed revealing internal structures

insulators. Alignment pins made from a D'addario 11 gauge e guitar string were used to align the CIT plates during assembly. Although the SS CIT plates were co-machined for

end plate hole concentricity and assembled with alignment pins, errors in the device alignment are apparent as shown in figure 5.5 and measured in table IX. Best efforts were made at correction, but with limited success, showing the limitations of this fabrication approach.

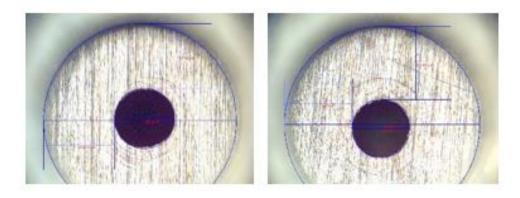


Figure 5.5. Alignment errors in SS CIT assembly – EP1, EP2 to RE

Table IX. SS CIT alignment for end plates relative to center ring electrode

SS CIT Electrode	Error in X (um)	Error in Y (um)
End plate 1	+100 um	+100 um
End plate 2	+50 um	-100 um

Accounting for the alignment errors, each error was input into a CAD model and imported to a SIMION model for simulation. Figure 5.6 shows a graphical representation of the misaligned SS CIT electrode end plate holes (left) and the distorted ion ejection pattern of the simulation (right). These distorted ion ejection trajectories result from localized assymetry in the equipotential well and trap at the end plate ejection holes. This result may contribute to peak broadening and mass shifting in mass spectra.

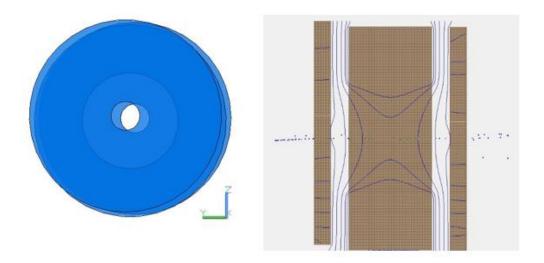
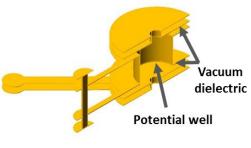


Figure 5.6. SS CIT CAD model and SIMION model of nonconcentric device

These alignment errors appear to have an adverse effect on CIT performance as shown in the SS CIT mass spectrum, figure 5.1, improved methods of assembly and alignment may potentially resolve this issue and improve CIT mass spectra. While it is assumed the CIT alignment error of previous investigations is less based on the published results, more work is needed to characterize the CIT plate misalignment effect [7, 8, 14, 47].

5.5.4 Internal electrode structures

While the SS CIT electrode structure is a rather simple parallel plate structure, the ceramic CIT device employs a more complicated design taking advantage of the LTCC material system fabrication methods to design a reduced area and capacitance electrode structure, figures 5.7 and 5.8, to minimize device power consumption.



Reduced capacitance Internal electrodes

Figure 5.7. Ceramic CIT internal electrode structure design

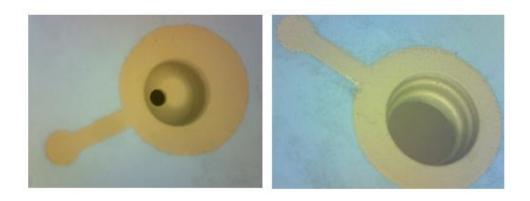


Figure 5.8. Fabricated green LTCC ceramic CIT electrode structures

While this design and fabrication method proved functional for the CIT devices, it also facilitates the batch fabrication of CIT chips for "consumable" miniature mass spectrometer applications, and is the first CIT produced using this method [44].

5.5.4.1 X-Ray imaging

As the ceramic CITs are monolithic chip ion trap devices, there is no readily available method to assess the internal geometry non-destructively other than X-Ray imaging. An X-Ray microscope was used to image, inspect, and measure the internal CIT

electrode structures to assess alignment and artifacts of the fabrication and co-firing processes.

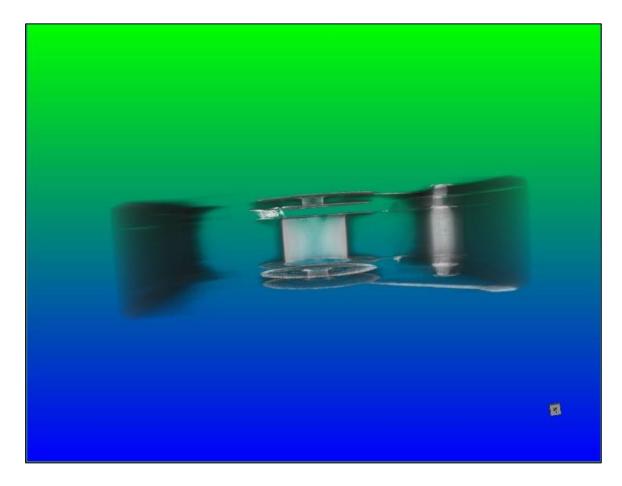


Figure 5.9. Ceramic CIT, X-Ray image of internal electrode structures

In figure 5.9, we can see the fabricated metalized ceramic LTCC, silver electrodes, and via electrode, as designed in figure 5.7. This inspection process proved invaluable for the selection of ceramic CITs for test. One can see delamination of the silver electrode in figure 5.9, this CIT was not selected for testing, but did pass an electrode continuity test. In figure 5.10 there are the apparent center offset alignment errors of the end plate

electrodes due to assembly error. All plate apertures should be concentric for best device performance. A shift in the end plates may cause mass shifts and poor spectrum resolution.

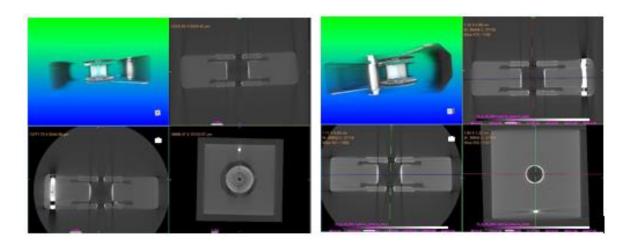


Figure 5.10. Ceramic CIT X-Ray images – Misalignment due to assembly errors

Two types of ceramic CITs were selected for testing, the standard ring design, figure 5.10, and the notched ring electrode for enhanced ion detection efficiency in figure 5.11. One can see how the LTCC material system and fabrication enables the notched ring electrode design. This CIT was selected for testing and has improved alignment and better performance compared to the standard design SS CIT tested. This proves the concept of the LTCC ceramic and notched ring electrode CIT mass separation capability.

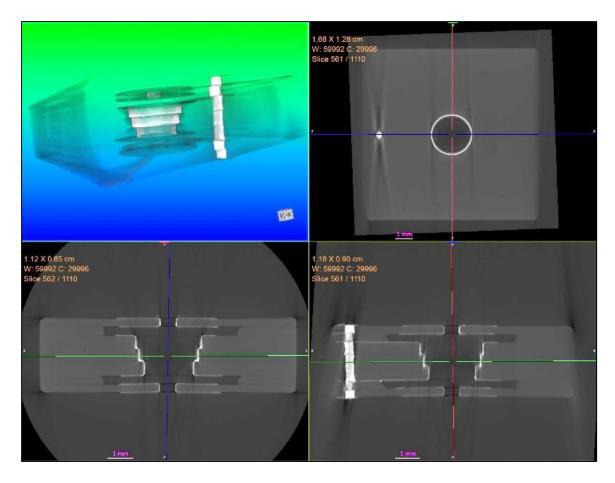


Figure 5.11. Notched ceramic CIT internal notched ring electrode structure

5.5.4.2 CIT cross sections

Destructive device inspection was also done to gain more detailed information from the internal CIT structures. The LTCC co-firing process involves the burn out of the glass ceramic binders and results in shrinkage of the overall geometry; oversized designs are made to compensate for this affect [57]. For the sections created, in figures 5.12 and 5.13, there are three main items that can be observed. First, the internal electrode structures look to be uniform with good coverage. Second, an assembly layer rotation error created the delamination and via discontinuities in both figures. Third, there is

delamination between the ring electrode and the gap and endplate electrodes. This is due to the oxidation of the device component layers before stacking, as well as the use of a non-compatible via material from Heraeus versus Dupont, causing buckling, sag, and warping of the devices. In general, these issues may be avoided by the use a single material system, non-expired, and a robust manufacturing process, which should greatly improve the quality of the resulting devices, alignment, uniformity, and their resulting performance.

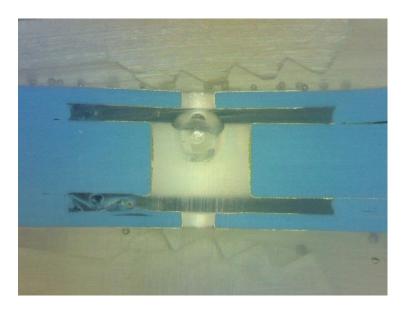


Figure 5.12. Ceramic CIT section in epoxy mount for polishing and inspection

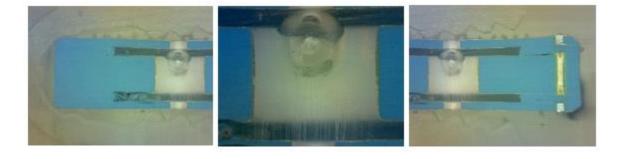


Figure 5.13. Ceramic CIT section – zoom images

5.5.4.3 SEM imaging SS and Ceramic CIT

Scanning electron microscopy (SEM) imaging of the CIT devices was done to gain more insight to the internal electrode and ceramic structure, as well as composition. Both SS and ceramic CIT devices were imaged to compare the internal structures. A fundamental difference between the two electrode structures is the co-firing of the ceramic devices. This process results in a completed device with smooth rounded edges ready for use, with no post process de burring or cleaning required, unlike SS CITs or other manufacturing methods [6, 16, 47, 48, 52]. Figure 5.14 is an SEM image of the entire SS CIT endplate and figure 5.15 shows the post machining and cleaning electrode structures up close; sharp edges and potential field emitting points remain.

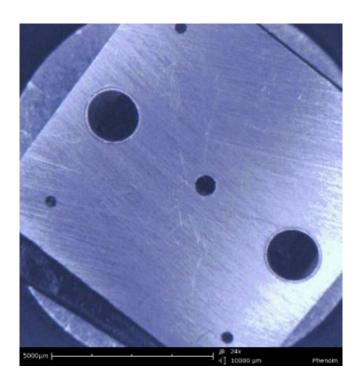


Figure 5.14. SS CIT end plate electrode

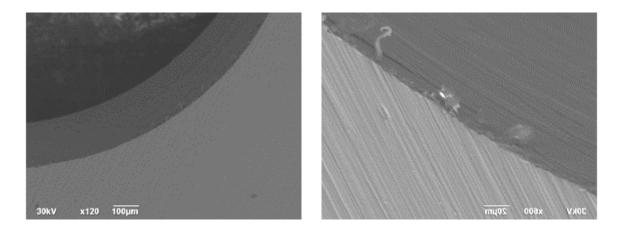


Figure 5.15. SS CIT internal electrode structure SEM images and field emitting sources

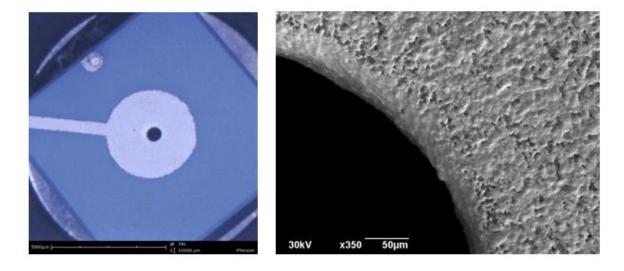


Figure 5.16a&b. SEM image of Ceramic CIT and endplate electrode surface

The ceramic CITs are completed in a final co-firing process at 850 C, resulting in a monolithic ceramic structure. The Dupont LTCC material system is formulated for co-firing compatibility to yield highly conductive electrodes and high quality insulators from the same process [57]. Figure 5.16 a&b are images of a co-fired ceramic CIT device and an SEM image of the silver electrode structure. There appears to some surface roughness

as well as discontinuity of the electrode on the surface. A closer look in figure 5.17, shows sintered silver particles as well as darker areas of glass in the surface of the electrode.

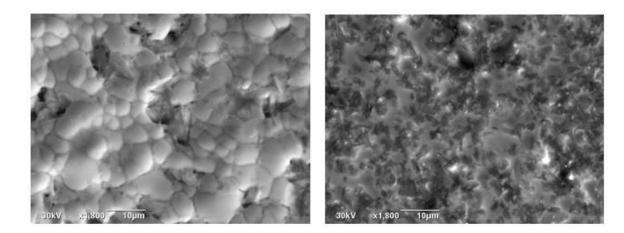


Figure 5.17. Ceramic CIT silver electrode (left) and ceramic surface (right) SEM images

The right image in figure 5.17 is of the ceramic substrate and reveals a mixed material matrix as well. The common material between the electrode and ceramic materials is assumed to be glass to promote adhesion between the two structures. The surface roughness of the electrode and ceramic were measured at Ra = 735 nm and Ra = 315 nm respectively, with closer inspection via SEM the profiler tip resolution may have been a limitation for the measurement as the roughness appears to be larger from the images. However, it is assumed the surface roughness will have a minimal effect on the performance of the ceramic CIT electrostatic field generation. As the CIT is formed in the co-firing process at 850 C it has superior electrode adhesion, device durability, elevated temperature and voltage operation capabilities compared to SS CITs.

5.5.4.4 EDS analysis of Ceramic CIT substrate and electrode material

EDS analysis were done to determine the composition of the ceramic CIT electrodes and ceramic substrate to confirm the addition of glass to both structures. Two spot locations, figure 5.18, were analyzed in the SEM EDS system producing an X-Ray spectrum for each spot, figures 5.19 and 5.20. The first electrode spot analyzed produced dominant silicon and silver peaks with an oxygen peak present as well. This result points toward the composition of spot one to be SiO₂ or glass, while the second spot has a dominant silver peak only, confirming the addition of glass to the electrode material.

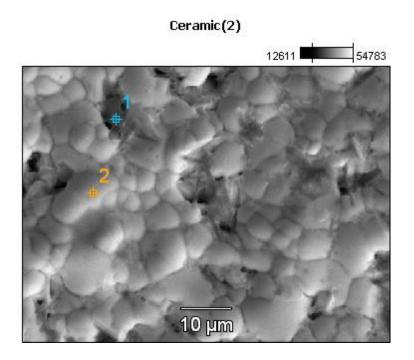


Figure 5.18. Ceramic CIT SEM/EDS analysis locations – Silver (2) and glass (1)

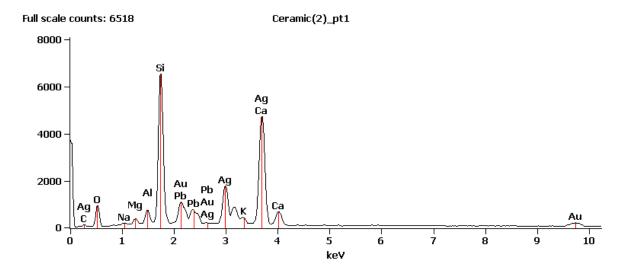


Figure 5.19. EDS spectrum of ceramic CIT electrode – Main Silicon and Oxygen peak present

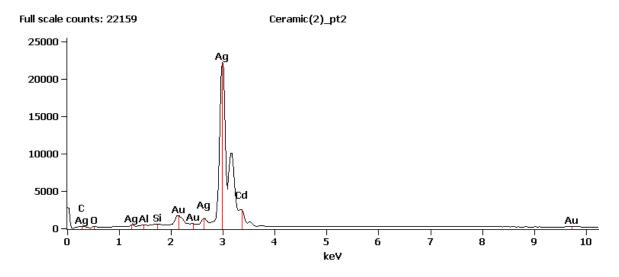


Figure 5.20. EDS spectrum of ceramic CIT electrode – Main Silver peak present

EDS analysis of the ceramic material was performed in the same manner as the electrode, figure 5.21. Figures 5.22 and 5.23 show dominant peaks for Silicon and Aluminum, as well as Oxygen. LTCC is a glass (SiO₂) and Alumina (Al₂O₃) ceramic material, the EDS results serve as a confirmation. The addition of glass to both the

electrode and substrate material aid in adhesion and stability of the material system and do not appear to effect the electrostatic performance of the CIT electrodes.

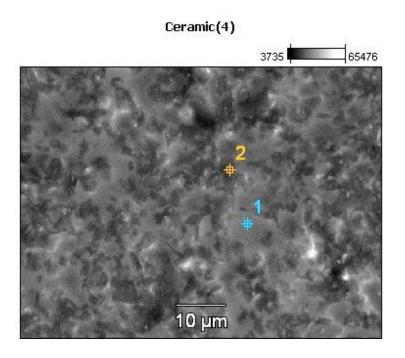


Figure 5.21. CIT ceramic substrate SEM/EDS spot analysis locations – Al_2O_3 (2) and glass (1)

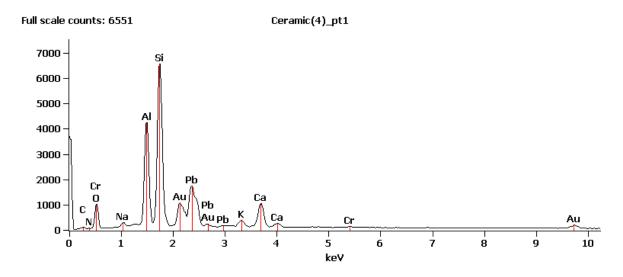


Figure 5.22. EDS spectrum of ceramic CIT substrate – Main Silicon and Oxygen peak present

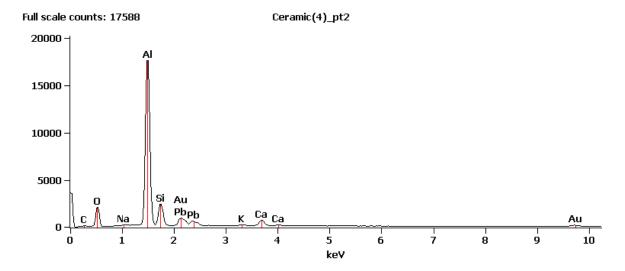


Figure 5.23. EDS spectrum of ceramic CIT substrate – Main Aluminum and Oxygen peak present

5.6 CIT Voltage Breakdown

High voltage testing of the SS CIT and ceramic CIT was done with a HV DC voltage source in the test bed high vacuum chamber. The CITs were mounted on a vacuum flange and tested at a pressure of 1.0E-6 Torr. Testing was done by raising the DC high voltage between the ring and grounded end plate electrodes, the voltage was increased until breakdown at 0.9 KVdc for the SS CIT and 4 KVdc for the ceramic CIT. The SS CIT and silicon CIT technology have 900Vdc and ~ 300Vdc operational voltage limits respectively. Device failure of the ceramic CIT at 4 KVdc enables superior extended range performance mass scanning and higher frequency operation, creating the potential for new CIT MS applications and improved resolution performance.

CHAPTER 6

6.0 CONCLUSIONS AND FUTURE WORK

This work has investigated the application of additive manufacturing and metalized ceramic material systems to mesoscale cylindrical ion trap (CIT) mass analyzer design and fabrication. A first and new class of CITs has been realized with improved ion signal output, low power performance, and extended dynamic range. High performance, miniature, rugged, monolithic mass spectrometer ceramic CIT chips have been batch fabricated and may be used as a consumable item for hand held field MS units. The new ceramic CIT technology has obvious performance, size, weight, and power (SWaP) benefits compared to conventional SS CIT assemblies in field portable MS units, figure 5.24, enabling further hand held MS development and application.



Figure 5.24. Ceramic CIT (10 mm²) and FLIR Griffin 460 SS CIT assembly [26]

Through this work, the benefits and obstacles of additive manufactured ceramic CITs have been observed and has initiated the application of co-fired metalized ceramic material systems for larger application to miniature mass spectrometer instrument systems.

Apart from the benefits of the new CIT mass spectrometer chips, the most significant finding in this work is increased CIT ion detection efficiency. It has been demonstrated via simulation and experiment ~ 80% and greater CIT ion detection efficiency, signal improvement of the percentage of analyzed ions detected, from 50% detection for conventional CIT design. Utilizing a unique notched ring electrode design that increases the ion signal output to the detector, the electron ionization quantity and power required for mass spectrum generation and tuning was reduced by ~ 1 watt or 33%, as well as the required ion amplification of the ion detector. Increased CIT ion detection efficiency effectively increases the total amount of the sample ions analyzed versus lost, thus increasing the instrument sensitivity and data collected by ~ 50%, as well as reducing duty cycle and power.

6.1 CIT mass spectrometer performance

CITs of ro = 1mm were fabricated from low temperature co-fired ceramic (LTCC), as well as in conventional stainless steel material for performance comparison, and were tested in mass instability scanning and resonance ejection modes to produce

Perfluorotribuytlamine (PFTBA) mass spectra. Two miniature cylindrical ion trap mass spectrometers were tested, SS CIT and notched Ceramic CIT, the mass spectrum range was 50 Da to 300 Da as expected given the setup and input signals, but their mass resolution varied. Due to misaligned electrodes in the CITs, the SS CIT had a peak width

of 23 Da at 69 Da FWHM, while the notched ceramic CIT had a peak width of 13 Da at 69 Da FWHM. The assembly alignment errors added to peak broadening and mass shifts in the mass spectra due to ion ejection trajectory distortion in the non-uniform electrostatic fields within the traps. Both performance results are not desirable from an analytical instrument, but the performance of the SS CIT technology and the alignment errors point to reasonable solutions for correction; better alignment and higher RF frequency. It should also be noted that the mass separation performance of the Notched Ceramic CIT is better than the stainless steel CIT tested, this is significant as the new notched ring electrode design demonstrates comparable mass separation performance, but with the added feature of ion ejection to the detector.

6.2 CIT ion detection efficiency

Ion detection efficiency is inferred to have increased based on repeatable simulation results with ~ 80% and above ion detection and experimental CIT systems energy input results. The SS CIT and notched ceramic CIT were tested in identical experimental conditions, the only difference being the mass analyzer under test. Each experiment was run with PFTBA and Helium pressures being established, ion source and detector tuning, and final readout electronics tuned for best spectrum output. The notched ring electrode ceramic CIT experiments resulted in reduced electron energy input, by nearly 1 watt for the given setup, as well as lower detector operating voltage or less ion amplification for the same experiment versus the SS CIT. Operating the notched ceramic CIT at the SS CIT tuned energy levels ~ 3W resulted in signal saturation; reducing the energy level to 2.3W produced optimal operation and mass spectrum results for the

notched ceramic CIT. It is this reduction in the required electron ionizing energy and ion amplification of the detector that demonstrates the increased ion detection efficiency of the notched ceramic CIT. The proof of the CIT ion ejection efficiency concept via the notched ring electrode is a significant finding which may enhance CIT miniaturization application and ion trap designs at any scale.

6.3 CIT power consumption

Power budgets are of great concern for miniaturized instrumentation. With instrument scale reduction available power resources are also reduced. Moving to more energy efficient designs and materials for miniaturized devices can make the difference between technology moving to field applications or remaining in the laboratory. Two miniature cylindrical ion trap mass spectrometers were tested, conventional SS CIT and the notched Ceramic CIT under identical experimental conditions. The ceramic material system offers design and material benefits which reduce the CIT power consumption by 29x from ~10.20 mW power consumption for the stainless steel CIT design to 0.36 mW for the ceramic CIT. Application of the LTCC RF material system to ITMS technology has enabled more energy efficient miniature CIT devices.

6.4 CIT operational stability

Miniature co-fired ceramic monolithic CIT mass spectrometers on a chip have been demonstrated, having rugged, inert, highly conductive, insulating, low off gassing, and high heat (600 C) tolerance properties. Internal electrode structures are rounded with 40 um radii edges which facilitates high voltage operation, ~ 4KV, and reduced internal

arcing. The current ceramic CIT design is batch fabricated, reducing cost and manufacturing defects, while providing a simple and low cost disposable CIT chip for potentially increased reliability and operational time for hand held MS instruments in the field.

6.5 Future work

Having demonstrated the first complete LTCC material system ceramic cylindrical ion trap chip and the notched ring electrode design, there is much more work to be done to develop the technology. The most significant area of work relative to immediate application of the devices is the development of additive manufacturing processes that yield ceramic CIT chips without manufacturing errors for best mass spectrum performance. The second area of work is investigating the expansion of the ceramic CIT mass analyzer into a microsystem instrument using the LTCC material system. Ceramic material systems are an advanced platform for integrated MS instruments. High performance low power ceramic CIT mass analyzers coupled with new ceramic ionization sources and detection devices may provide miniature hand held and probe MS instruments for in situ sample analysis applications, taking mass spectrometry out of the lab and farther into the field.

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