2-3-2003

Analysis of the lateral diffuse metal-oxide semiconductor (LDMOS) power amplifier for cellular base stations

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DOI: 10.25148/etd.FI14051190

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FLORIDA INTERNATIONAL UNIVERSITY

Miami, Florida

ANALYSIS OF THE LATERAL DIFFUSE METAL-OXIDE SEMICONDUCTOR
(LDMOS) POWER AMPLIFIER FOR CELLULAR BASE STATIONS

A thesis submitted in partial fulfillment of the

requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

by

Waldack Bonhome

2003

To: Dean Vish Prasad
College of Engineering

This thesis, written by Waldack Bonhome, and entitled Analysis of the Lateral Diffuse Metal-Oxide Semiconductor (LDMOS) Power Amplifier for Cellular Base Stations, having been approved in respect to style and intellectual content, is referred to you for judgment.

We have read this thesis and recommend that it be approved.

Malcolm Heimer

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Date of Defense: February 3, 2003

The thesis of Waldack Bonhome is approved.

Dean Vish Prasad
College of Engineering

Dean Douglas Wartzok
University Graduate School

Florida International University, 2003

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DEDICATION

I dedicate this thesis to my family, colleagues, and professors. Without their patience and support I would not have been able to complete my work. I thank you with all my heart.

ACKNOWLEDGMENTS

I wish to acknowledge my committee members for their support and especially their patience and understanding. Without their support I would not have been able to complete my work. I also wish to acknowledge Dr. Wunnava; you have known me since the beginning when I first started my journey. I thank you Dr. Heimer for your availability when I took ICs with you. I acknowledge Dr. Babij for giving his time to work around my schedule. I also want to give acknowledgment to Noom (Nutrapong Futrakul) for his friendship. I appreciate the projects we've worked on and I am proud to call you my friend. I also acknowledge everyone here for your support. I thank you with all my heart.

ABSTRACT OF THE THESIS

ANALYSIS OF THE LATERAL DIFFUSE METAL-OXIDE SEMICONDUCTOR
(LDMOS) POWER AMPLIFIER FOR CELLULAR BASE STATIONS

by

Waldack Bonhome

Florida International University, 2003

Miami, Florida

Professor Tadeusz M. Babij, Major Professor

The primary purpose of this thesis was to present a theoretical large-signal analysis to study the power gain and efficiency of a microwave power amplifier for LS-band communications using software simulation. Power gain, efficiency, reliability, and stability are important characteristics in the power amplifier design process. These characteristics affect advance wireless systems, which require low-cost device amplification without sacrificing system performance.

Large-signal modeling and input and output matching components are used for this thesis. Motorola's Electro Thermal LDMOS model is a new transistor model that includes self-heating affects and is capable of small-large signal simulations. It allows for most of the design considerations to be on stability, power gain, bandwidth, and DC requirements. The matching technique allows for the gain to be maximized at a specific target frequency. Calculations and simulations for the microwave power amplifier design were performed using Matlab and Microwave Office respectively. Microwave Office is the simulation software used in this thesis.

The study demonstrated that Motorola's Electro Thermal LDMOS transistor in microwave power amplifier design process is a viable solution for common-source amplifier applications in high power base stations. The MET-LDMOS met the stability requirements for the specified frequency range without a stability-improvement model. The power gain of the amplifier circuit was improved through proper microwave matching design using input/output-matching techniques. The gain and efficiency of the amplifier improve approximately 4dB and 7.27% respectively. The gain value is roughly .89 dB higher than the maximum gain specified by the MRF21010 data sheet specifications. This work can lead to efficient modeling and development of high power LDMOS transistor implementations in commercial and industry applications.

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Chapter 1

INTRODUCTION

1.1 Introduction

Since the beginning of telecommunications mankind has been trying to seek out different ways to communicate over great distances due to the rapid fading of sound waves in air. Even at low frequencies a signal will still fade out rapidly, thus, the signal must be modulated to a higher frequency to overcome this effect. A solution to this effect is to use electronics to efficiently adjust and transport a signal through a medium established for communication. However, a wireless medium does not support digital data but instead the digital data is converted into an analogous signal that can fit into the wireless medium. With 3G systems emerging the demand for increased transistor output power has escalated the support for base station RF power amplifier design. These power amplifiers must be efficient and produce an optimal degree of power to handle the increased multi-frequency traffic. Next generation technology is an evolution, rather than a revolution, of mobile network standards that encompasses W-CDMA technology, such as IS2000, IMT-2000, and cdma2000 to name a few. Therefore, can transistors meet the high demand of linearity, efficiency, and reliability at a reasonable cost required for next generation systems?

Traditionally single channel analog systems use RF bipolar transistor technology developed in the 1960s, since then this technology has improved in terms of gain, output power, efficiency, and reliability. Linearity, however, is limited by fundamental characteristics of bipolar transistors. Bipolar transistors have two significant linearity problems, high order IMD and low level crossover distortion. MOSFETs on the other hand have lower high order IMD than bipolar transistors and do not require the ballasting that stabilizes minority carrier in bipolar transistors, since they are majority carrier devices [1]. These combined MOSFET traits produce superior IMD at reduced output power. With the introduction of lateral diffused metal-oxide semiconductors (LDMOS) the operating frequency of silicon power for FETs was increased. This makes it possible to produce RF power transistors having high gain, usable efficiency, low thermal resistance and superior IMD when applied in communication systems, such as 3G.

Acknowledging the high output levels with good linearity and simple biasing requirements that LDMOS technology offers is of great benefit to wireless communications. As an example, emerging wide-band CDMA networks will support a wider range of wireless digital services, such as Internet/intranet and other Internet provider IP-based applications, video, high-speed data communications and interactive services. The information density of these more complex signals requires higher degrees of amplifier power. In other words, W-CDMA and other “spectrally efficient” modulation systems have significantly stringent requirements for their active devices.

1.2 Purpose and Significance

Due to emerging cellular standards cost effective RF power amplifiers are required. Thus, the purpose of this thesis will use software simulation to demonstrate optimal efficiency, output power, and the fulfillment of transistor stability over a desired frequency range. The second purpose is to analyze the Motorola Electro Thermal-Lateral Diffused Metal-Oxide Semiconductor (MET-LDMOS) model and how it can be engineered to achieve better gain and output power over a dynamic frequency range. Small-large signal analysis will be applied to the microwave power amplifier design for optimal output performance. The simulation results will be compared to calculated results during the design process.

First the transistor will be checked for stability. If the transistor does not satisfy Rollet's stability condition, k , then the addition of passive elements will be used to stabilize the transistor. If the transistor is stable then microwave matching methodology will be applied to match input/output impedances for maximum power transfer. The output from the non-matched transistor and matched transistor will be compared.

Chapter 2

Power Amplifier

2.1 Power Amplifier Description and Background

There are many factors present when a system desires to communicate with another system in order to allow the communication to take place. There needs to be a medium that is reliable enough to carry a signal in such a way that the receiver can recover it.

There must also be a device that can perform the following functions...

- Receiver; picks up the information signal from the medium
- AD converter; converts the analogous signal into a digital
- DSP; processes the digital data
- DA converter; converts the digital data into an analogous signal
- Transmitter; transmit the signal into a communication medium

A device exist in between the DA and transmitter that amplifies the signal to the proper level such that the effects of the medium in which it is transmitted do not prevent the signal from being received or misunderstood. That device is a power amplifier (PA) and applying the output of the PA to a load device transmits the signal, whether it is circuit

elements or an antenna or a similar device. The power levels required to reliably transmit the signal are often high which would require the PA to consume a lot of power. However, in optimal design the power consumed by a PA should be minimal to maximize the length of time for which power is needed. Therefore, in an ideal case the PA would consume only the power needed to drive an antenna (load) with the required output power for transmitting the signal, so that the ratio for power transmitted to the power consumed in the PA is one...

$$\frac{P_{out}}{P_{total}} = 1 \quad (2.1)$$

This ratio represent the power delivered to the load, to the power consumed by the device and is called the efficiency of the PA. There are several types of efficiency that measure the power amplifier's performance, but only three will be mentioned here.

One efficiency method is the Drain efficiency and is defined as...

$$\text{Efficiency}_{\text{Drain}} = \frac{P_{\text{RFout}}}{P_{\text{DC}}} \quad (2.2)$$

This ratio represent the power delivered to the load at the desired RF frequency (P_{RFout}), and the total power taken from the dc supply (P_{DC}).

However, the drain efficiency does not account for RF power delivered to the input of the amplifier. This tends to exaggerate the actual efficiency due to the relatively low gains of power amplifiers. A better measure of the efficiency that includes the effect of the input power is the Power Added Efficiency (PAE) and it is defined as...

$$PAE = \frac{(P_{RFout} - P_{RFin})}{P_{DC}} \quad (2.3)$$

This ratio represent the power delivered minus the power needed to drive the input at the desired RF frequency of interest ($P_{RFout} - P_{RFin}$), divided by the total power from the dc supply (P_{DC}).

Now the overall efficiency is then defined as...

$$Efficiency_{overall} = \frac{P_{RFout}}{P_{DC} + P_{RFin}} \quad (2.4)$$

Thus, it can be seen that the PAE and overall efficiency represent better methods to gauge the true performance of a PA, since they include the power needed to drive the input of the PA at a desired RF frequency. The driving power is also a measure of the PA's gain; therefore, the overall efficiency can distinguish between two PA with the same Drain efficiency but with different gain.

In reality, RF circuits that perform in the high frequency spectrum will not have power amplifier efficiencies at 100%. In high frequency systems the PA must amplify the signal, as well as, supply power to the load. In the amplification process, some power must be consumed within the circuit elements of the PA, but to perform both amplification and drive the load efficiently there must be a very small to no power consumed. Therefore, there must be some middle point where both interests can co-exist.

2.2 Amplifier Classes

RF power amplifiers can be categorized as linear or non-linear amplifiers. Within these categories there exist a sub-division of classes that are distinguished by the circuit configuration, operational topology, linearity, and efficiency. Class (A), (B), and (AB) represents the linear classes while the higher letters represent non-linear classes. Power classification is based on the amount of time the output device operate during one complete cycle of signal swing or the amount of current flowing in the output device with no applied signal [2]. Thus, it is primarily the design of the output stage that defines each class.

2.2.1 Class A

For class (A) operation both devices on the output stage would conduct continuously for the entire cycle duration of a signal swing, where the conduction angle is 360° . There is

no instance or condition where one device or the other is turned off, as illustrated by the waveform in Figure 2.1.

Figure 2.1 Output waveform of a Class (A) amplifier [3]

Class (A) amplifiers in reality are single ended designs where there is only one type of polarity for the output devices. This makes the class (A) amplifier design the most inefficient power amplifier where it would draw 5-times as much power from the source than what is delivered to the load. The negative of this amplifier design is that it is large, heavy, and runs very hot. The positive of this amplifier design is that it is inherently the most linear and has the least amount of distortion.

It was previously mentioned that class (A) operation amplifiers were the most linear and inefficient power amplifiers as far as their design, as illustrated in Figure 2.2.

Figure 2.2 A basic Class (A) implementation

The output of the device maintains a constant gain in the active region where it is linear in that region. However, since the device is always on it constantly carries current and that current represents a continuous lost of power in the device over and beyond what is needed to drive the load. Thus, the efficiency of the RF class (A) power amplifier is limited to 50%. However, in FET implementations, the efficiency will not realistically reach 50% [4]. The efficiency is then represented where the output is biased at the supply voltage, V_{DD} , and the output swing has amplitude of V_{DD} as illustrated in the following...

$$\eta = \frac{\left[\left(\frac{1}{2} \right) \cdot V_{DD} \right] \cdot i_D}{V_{DD} \cdot i_D} = \frac{1}{2} \quad (2.5)$$

The output is biased at the supply voltage, as illustrated in Figure 2.2, thus the output swing has amplitude of V_{DD} . The numerator is the power delivered to the load and the denominator is the average power delivered to the circuit by the supply [4]. However, for MOSFETs the peak efficiency is significantly lower, because it is not possible to have an output swing of V_{DD} and still keep the device in saturation.

2.2.2 Class B

For class (B) operation both output devices are never allowed to conduct at the same time, where the conduction angle is 180° . In other words, the current flow in a specific device is zero when not excited by an input signal and flows for one half of cycle duration when excited by an input signal, as illustrated by the waveform in Figure 1.3.

Figure 2.3 Output waveform of a Class (B) Amplifier [3]

This operation allows the class (B) design to have high efficiency but poor linearity around the crossover region, where one device is turned off and the other is turned on.

The transitional time for one device to turn on and the other to turn off produces extreme crossover distortion, which is another, negative affect on wireless communications.

A class (B) design provides two devices, one to push current into the load and the other to pull current from the load, as illustrated in Figure 2.4...

Figure 2.4 A basic Class (B) push-pull implementation

During the positive half cycle of the signal swing one device will pull current from the load and during the negative half cycle of the signal swing the other device will push current into the load this process is called “push-pull”. The design allows conduction to occur at 180° degrees or one half the input cycle. Generally this operation can remain linear, but there will be instances when the devices are off, no current flow, and crossover distortion can be produced. In other words, the signal has to cross over from one device to the other, which can degrade the architecture’s linearity and depending on the type of devices, if different, can degrade linearity even further. However, the class (B) architecture does allow for high efficiencies, thus, is useful in systems that require high efficiency and less linearity.

2.2.3 Class AB

For class (AB) operation both output devices are barely on at the same time, where the angle of conduction is greater than 180° but much less than 360° . In other words, the current flow in a specific output device appreciably more than a half cycle but less than the entire cycle, as illustrated by the waveform in Figure 2.5.

Figure 2.5 Output Waveform of a Class AB Amplifier [3]

A small amount of current flows through both devices but only enough to keep each device operating so that the device can respond quickly to an input voltage demand. Thus, the inherent non-linearity of the class (B) design is eliminated and the inefficiencies of the class (A) design are also non-existent.

A combination of class (A) and (B) amplification design is desired for base station design. The idea is to use the push-pull structure with each device biased slightly above threshold. What would differ is the biasing circuit and output waveforms, as illustrated in Figure 2.5. When the two devices are allowed to conduct current for a short period, the waveform of the output voltage can be smooth during the crossover period and thus can reduce the distortion at the output. The benefit of the class (AB) structure would then be to provide linearity close to a class (A) structure with efficiency close to a class (B) structure.

The previously mentioned classes are examples of linear architectures common to base stations where the input/output amplitude and phase are linearly related. However, there are cases where transmitted information is contained in something else other than the amplitude of the signal output and requires the efficiency of the power amplifier to be optimized. The main non-linear amplifier classes are designated: C, D, E and F to name a few. In the current high bandwidth-demanding world of wireless communications these non-linear power amplifiers are better utilized in hand-held devices to improve their efficiency and reduce the power dissipated. The requirements for high data rates in the already crowded RF spectrum necessitate the use of shaped data pulses in modern digital signals such as, CDMA. These CDMA applications are applied in cellular base stations and require simultaneous amplification of multiple carrier signals. Thus, the linear power amplifier will be investigated further in this thesis.

2.3 Linear RF Amplifier Design Theory

An ideal amplifier has constant characteristics within the bandwidth of the applied signal. However, power amplifiers contain active components, which produce non-linearities that cause linear distortion. Thus, a perfect linear amplifier represented by...

$$V_{OUT}(t) = G V_{IN}(t) \quad (2.6)$$

is replaced by its non-linear counterpart in a practical environment [5]...

$$V_{OUT}(t) = G_1 \cdot V_{IN}(t) + G_2 \cdot V_{IN}^2(t) + G_3 \cdot V_{IN}^3(t) + \dots + G_N \cdot V_{IN}^n(t) \quad (2.7)$$

Figure 2.6 Input/Output voltage characteristic [5]

As illustrated in Figure 2.6 at high signal levels the output voltage compresses for both positive and negative values. This compression is due to the third-order term G_3 while the second-order term G_2 causes an overshoot at one end and clipping at the other [5]. A design analysis using s-parameters can be used to demonstrate some basic principles of power amplifiers.

2.4 Amplifier Design Considerations

A systematic method to design an amplifier to certain system specifications can be based on the s-parameters of the transistor. This is due to the fact that the main part of an

amplifier is its active transistor component. The transistor component can be characterized as a two-port s-parameter network.

Figure 2.7 An S-parameter based transistor amplifier [6]

Figure 2.7 is a single stage s-parameter based transistor amplifier with source and load impedance selected to meet a certain specification. The reflection coefficients, Γ_s and Γ_L , are then determined from the selected impedance. After the reflection coefficients are determined the following equations can be used for the input and output reflection for the transistor, as expressed by [7]...

$$\Gamma_{IN} = S_{11} + \frac{(S_{12} \cdot S_{21} \cdot \Gamma_L)}{1 - S_{22} \cdot \Gamma_L} \quad (2.8)$$

$$\Gamma_{OUT} = S_{22} + \frac{(S_{12} \cdot S_{21} \cdot \Gamma_S)}{1 - S_{11} \cdot \Gamma_S} \quad (2.9)$$

To better understand the design aspects of an amplifier there must be an understanding of the parameters involved. The following section will discuss power gain and the stability issues.

2.5 Power Gain

One of the most important design considerations in a microwave transistor amplifier is power gain [7]. The most commonly used power gain equations are the transducer power gain, G_T , operating power gain, G_P , and the available power gain, G_A , as follows...

$$G_T = \frac{P_L}{P_{avs}} = \frac{\text{power delivered to the load}}{\text{power available from the source}} \quad (2.10)$$

$$G_P = \frac{P_L}{P_{IN}} = \frac{\text{power delivered to the load}}{\text{power input to the network}} \quad (2.11)$$

$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{\text{power available from the network}}{\text{power available from the source}} \quad (2.12)$$

The s-parameter equivalent to the above power gain equations can be expressed in the following form using the reflection coefficients, Γ_S and Γ_L , as expressed by [7].

$$G_T = \frac{[1 - (|\Gamma_S|)^2]}{(|1 - \Gamma_{IN} \Gamma_S|)^2} \cdot (|S_{21}|)^2 \cdot \frac{[1 - (|\Gamma_L|)^2]}{(|1 - S_{22} \Gamma_L|)^2} \quad (2.13)$$

$$G_T = \frac{[1 - (|\Gamma_S|)^2]}{(|1 - S_{11} \Gamma_S|)^2} \cdot (|S_{21}|)^2 \cdot \frac{[1 - (|\Gamma_L|)^2]}{(|1 - \Gamma_{OUT} \Gamma_L|)^2} \quad (2.14)$$

$$G_P = \frac{1}{(|1 - \Gamma_{IN}|)^2} \cdot (|S_{21}|)^2 \cdot \frac{[1 - (|\Gamma_L|)^2]}{(|1 - S_{22} \Gamma_L|)^2} \quad (2.15)$$

$$G_A = \frac{1 - (|\Gamma_S|)^2}{(|1 - S_{11} \Gamma_S|)^2} \cdot (|S_{21}|)^2 \cdot \frac{1}{[1 - (|\Gamma_{OUT}|)^2]} \quad (2.16)$$

Using equation 2.8 and 2.9 it can be seen that...

$$G_T = G_T[\Gamma_S, \Gamma_L, (S)] \quad (2.17)$$

$$G_P = G_P[\Gamma_L, (S)] \quad (2.18)$$

$$G_A = G_A[\Gamma_S, (S)] \quad (2.19)$$

Based on the above equations it is clear that the load impedance can be selected first to build the matching output network by using Γ_L . It is also common to use a conjugate match, $\Gamma_{IN} = \Gamma_S^*$, at the input of the transistor to suppress reflection between the input stage and the input of the transistor. This will allow for maximum power transfer to occur, $P_{IN} = P_{AVS}$. A similar procedure can be performed by selecting the source impedance first and conjugate match the output, $\Gamma_{OUT} = \Gamma_L^*$. The reflection is suppressed between the output of the transistor and output stage. Again the maximum power transfer is allowed to occur, $P_L = P_{AVN}$.

2.6 Stability

Another important design consideration in a microwave transistor amplifier is stability. For a two-port network, oscillations will occur when negative resistance is presented at either the input or output ports. In other words, when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$. Even with $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$ an amplifier circuit could still be made stable when the total input and output loop resistance is positive, as illustrated in Figure 2.8.

Figure 2.8 Stability of a two-port network [7]

This condition can be made possible by resistively loading the transistor or by adding negative feedback. In other words...

$$\text{Re}(Z_S + Z_{IN}) > 0 \quad (2.20)$$

And

$$\text{Re}(Z_L + Z_{OUT}) > 0 \quad (2.21)$$

Unfortunately, this technique does not have the same affect on narrowband systems due to degradation in power gain and noise figure [7].

Taking into consideration a unilateral two-port device, equations 2.20 and 2.21 can be satisfied for all passive components, $|\Gamma_S| < 1$ and $|\Gamma_L| < 1$, present at either the input or the output of the transistor, if the real port of the input impedance and the output impedance are greater than zero. In other words, $\text{Re}(Z_{IN}) > 0$ and $\text{Re}(Z_{OUT}) > 0$. The transistor is

then considered unconditionally stable. A more straightforward approach that provides a sufficient condition for unconditional stability is given by [7].

Through lengthy calculations the following condition is achieved...

$$K > 1$$

$$K = \frac{[1 - (|S_{11}|)^2 - (|S_{22}|)^2 + (|\Delta|)^2]}{2 \cdot |S_{12} \cdot S_{21}|} \quad (2.22)$$

$$1 - |S_{11}|^2 > |S_{12} \cdot S_{21}| \quad (2.23)$$

$$1 - |S_{22}|^2 > |S_{12} \cdot S_{21}| \quad (2.24)$$

alternatively,

$$K > 1 \text{ and } B_1 > 0$$

where,

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (2.25)$$

or,

$$K > 1 \text{ and } |\Delta| < 1$$

where,

$$|\Delta| = |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}| \quad (2.26)$$

As mentioned before in the potentially unstable case the transistor can remain stable through the proper selection of the reflection coefficients, Γ_S and Γ_L . If the reflection coefficients are selected in a stable region then they produce a stable operation. It is also possible to take a potentially unstable transistor and make it unconditionally stable by using a combination of a series or shunt resistive topology at the input and/or output [7].

2.7 Requirements for a Power Amplifier

Gain flatness and phase flatness across a desired frequency band is extremely important in a communication system. Any deviation from either can lead to poor communication between the transmitter and receiver. There are two major design goals that ensure optimum communication between systems, as explained in [8]. Optimum communication relies on good circuit design and attention to bandwidth in a RF power amplifier bias network. The transistor used is also an important component, in which the Q of the transistor affects its linearity across a desired frequency range. In other words, the lower the Q the better the transistor operates for a specified frequency band, as explained in [8]. In [9] Ericsson tested their PTF-10004 LDMOS transistor to address linearity and IMD challenges and the results are displayed in Figures 2.9 and 2.10. In Figure 2.9 the PTF-10004 is biased for class AB and the current is maximized to achieve a flat gain response [9]. In Figure 1.10 the FET demonstrates poor IMD performance at a higher power rating but demonstrates excellent IMD, surpassing the BJT, for a power rating below 30 watts.

Figure 2.9 Gain vs. input power of the PTF-10004 [9]

Figure 2.10 Third order IMD vs. output power for the PTF-10004 LDMOS and BJT [9]

Chapter 3

Lateral Diffuse Metal-oxide Semiconductor (LDMOS)

3.1 Introduction

Wireless technology is the enabler for future communications by providing a flexible alternate medium for data and voice. Data rates have risen since the IEEE 802.11 standard adaptation in 1997. Data rates since increased from 1 to 2 Mbps to the current standard of 11 Mbps (IEEE 802.11b) up to 54 Mbps (IEEE 802.11a) [10]. The availability of high data rates open the doors of expansion for wireless applications. This upward demand for wireless applications increases pressure on manufactures to make transistors more compact, less expensive and more reliable.

Wideband Code Division Multiple Access (WCDMA) cellular systems are emerging and the demand for transistors to increase output power and efficiency. WCDMA operate at the high frequencies causing stability and thermal runaway issues with current Bipolar Junction Transistors (BJT) that are commercially available. The Lateral Field Effect Transistor (LFET) features a low feedback capacitance, which results in increased stability and higher gain at high frequencies [11]. Companies like Motorola, Ericsson, and Phillips, to name a few, have pursued research in this technology with great gains.

The lateral channel structure also is less cost effective due to the amount of die area that is consumed for a given power rating. A detailed description of transistor die technology or the physics of channel generation in transistors will not be pursued in this thesis, but these concepts must be mentioned to gain an understanding for why transistors need to be designed a certain way. The introduction of the Laterally Diffused Metal-Oxide Semiconductor (LDMOS) not only give good stability and higher gain at high frequencies, but also eliminates thermal runaway through a diffused silicon that has a slight positive temperature coefficient. Thus, the LDMOS transistor can satisfy the requirements for efficiency, high linearity, reasonably high input/output impedance at the terminals, reliability, and at low cost with the proper biasing circuitry [12].

3.2 LDMOS vs. GaAs and BJT Transistors

WCDMA networks support a wider range of wireless digital services, such as IP-based applications, Internet & Intranet, video, high-speed data communications, and interactive services. This growth to WCDMA technology has increased the demand for high performance wireless subsystems. These wireless subsystems have several components and several in development, but no component is more important than the RF power transistor. The current implementation of WCDMA would require RF power transistors to operate in the 1900 MHz to 2.2 GHz frequency band. They also must demonstrate good linearity, stability, reliability, and high power gain. There are several RF power transistors in development for current and future wireless communication needs and an analysis of them all will go beyond the scope of this thesis. However, this section will

compare three RF power transistors, LDMOS, GaAs, and BJT, which have been implemented into the emerging wireless infrastructure.

Base-stations for existing and emerging wireless standards require cost effective RF power amplifiers. Much improvement has been done to bipolar junction transistors since their RF development in 1960 in terms of gain, output power, efficiency and reliability. However, BJTs have two significant linearity problems: high-order intermodulation distortion (IMD) products and low-level crossover distortion [1]. When applied in RF amplifiers BJTs require a bias voltage at the base for linear operation. Unfortunately, BJTs with their poor linearity characteristics are unable to meet the stringent requirements of new wireless standards, such as WCDMA. Thus, the development of MOSFET, specifically LDMOS, has increased and has become a viable solution to the BJT as the RF power transistor of choice for RF power amplifiers in the emerging wireless infrastructure.

LDMOS in general increases the operating frequency of silicon power FETs due to the p⁺ sinker that connects the source terminal to the p⁺ substrate, which is grounded. LDMOS has a simpler biasing circuit, higher power gain, simple control of the output power, superior thermal stability, superior load mismatch tolerance and does not require the ballasting that stabilizes a minority carrier transistor, such as BJT [13]. These and other previously mentioned characteristics are essential to handle the information density of the complex signals incorporated in WCDMA. Makers of wireless infrastructure equipment like Ericsson Microelectronics fabricate test platforms that demonstrate the

performance of an LDMOS over a BJT for base-station applications. A gold (Au)-metallized LDMOS transistor, PTF 10134, in a WCDMA communication system operating from 2110 to 2170 MHz with 10-dB typical power gain when biased under class AB with a +28 VDC supply was compared to an NPN BJT operating under similar conditions, as illustrated in Figure 3.1 and 3.2.

Figure 3.1 3rd, 4th, and 5th IMD products versus output power for the PTF 10134 LDMOS transistor [14]

Figure 3.2 3rd, 4th, and 5th IMD products versus output power for silicon bipolar junction transistor [14]

Figure 3.1 shows that the IMD products, although not monotonic, generally decrease continuously as the output decreases. However, in Figure 3.2 the bipolar junction transistor tends to have a “sweet spot”, where the output range corresponds to minimum distortion [14]. This demonstrates that the LDMOS has the more linear transfer function when compared to the bipolar. Thus, focusing on the PTF 10134 LDMOS transistor measurements of output power versus input power were made at 2170 MHz with a quiescent drain current of 1.3 A, as illustrated in Figure 3.3.

Figure 3.3 Output power, gain, and efficiency at 1dB operating from 2110 to 2170 MHz range [14]

The PTF 10134 LDMOS shows excellent performance across the high frequency band from 2110 to 2170 MHz at 1dB compression. The results re-emphasize the superior characteristics of the PTF 10134 LDMOS transistor over its NPN BJT counterpart.

Figure 3.4 ACPR performance of PTF 10134 in a broadband circuit [14]

Figure 3.4 shows the Adjacent Channel Power Ratio (ACPR) performance for the PTF 10134 LDMOS transistor, which clearly shows that the LDMOS is suitable for complex waveforms.

LDMOS has been portrayed well as the optimal choice for high frequency applications in wireless subsystems. However, GaAs is another technology that has come along and gain acceptance for RF high power amplifiers. RF power GaAs technology has mainly been used in military, peripheral, and niche market places, but with the implementation of 3G cellular communications RF power GaAs technology is now entering the wireless communications market. The GaAs technology has been significant in the cellular and PCS market places, as illustrated in Table 3-1.

Table 3-1
GaAs power transistor by application in World
Serviceable Available Market, 1999 [15]

Application	Value (\$millions)	Share
Cellular PCS	93	38%
Broadcast/Radio	0	0%
Radar	12	5%
Military	5	2%
Avionics	7	3%
Satellite	44	18%
Point to Point (licensed)	34	14%
ISM	17	7%
LMDS	17	7%
Others	15	6%
Total	246	100%

Source: Allied Business Intelligence, Inc., 2000

However, there broad usage has been in low power (<1W) cellular handset amplifier applications. GaAs capability to operate up through the microwave frequency range has increased its potential as a viable future technology in the wireless infrastructure. This in turn gives GaAs technology manufactures the opportunity to develop a strong penetration into the upper UHF and SHF frequency ranges for new wireless infrastructure technology.

Table 3-2
New Wireless Infrastructure Market Frequency Spectrum [15]

Frequency Band	Name	Primary Use
2.11 – 2.17 GHz	3G	Voice + Data
1.710 – 1.885 GHz	3G Expansion, US only	Voice + Data
2.52 – 2.67 GHz	3G Expansion Europe and maybe US (current MMDS spectrum in US)	Voice + Data
3 – 6 GHz (tbd)	4G (still to be defined)	Data

Table 3-2 gives an indication that the future of wireless communication will be bandwidth demanding. In other words, as the market demand for bandwidth increases, operating frequencies will also have to increase [15]. Therefore, the usable bandwidth must be reliable and cost-effective. For this to be possible inefficiencies in power amplifiers must be reduced and/or eliminated. Figure 3.3 illustrates the efficiency component for a PTF 10134 LDMOS transistor suggesting its reliability. However, at frequencies above 2.2 GHz the LDMOS transistor efficiency is low and becomes a performance barrier, as demonstrated in Figure 3.5.

Figure 3.5 Comparison of 30mm LDMOS die with 15.4mm GaAs die at 2.6 GHz [15]

As can be seen, the GaAs device has better efficiency than the LDMOS device at higher frequencies and is comparable with the LDMOS at lower frequencies. However, LDMOS linearity is superior to GaAs. It is suggested that the deployment of 3G systems will push for lower cost RF power amplifiers and good tradeoffs between linearity and efficiency for overall performance. For GaAs to become a major player in 3G linear power amplifiers will depend on the differentiation of improved performance due to efficiency over LDMOS and consistent RF performance [15]. Manufacturers are making strides to increase the peak power capability and improve efficiency for future generations of LDMOS. Thus, ensuring their continued acceptance in the wireless infrastructure.

3.3 LDMOS Design

Radio Frequency Laterally Diffuse Metal-Oxide Semiconductor (RF-LDMOS), as previously mentioned, is the leading transistor technology for high power RF applications in base station power amplifiers. LDMOS operate mostly in a common source circuit configuration biased at an idle current in Class AB to achieve a balance between linearity and efficiency. The common source configuration exhibit good stability, good linearity, and high power gain into the Ultra High Frequency (UHF) spectrum, 300 MHz – 3 GHz [11]. The LDMOS transistor depends upon successive lateral diffusion profiles of impurities of opposite polarity to achieve their channel regions. At low voltage applications the LDMOS transistor gate potential can substantially reduce the resistance of the N- (LDD) region by heavily accumulating charge carriers at the surface, thus allowing the LDMOS transistor to produce more current per unit area [11]. The LDMOS topology minimizes gate and drain electrode overlapping in the transistor, which produces a minimal feedback capacitance that is necessary for RF wireless systems. The following sections describe the functional characteristics for a general LDMOS transistor.

A cross-sectional view of a three terminal LDMOS device is illustrated in Figure 3.6. A highly doped p-type sinker is laterally diffused on a cross section of the MOSFET structure to ground the source to the substrate. The laterally diffused channel, under the gate, enhances RF performance and prevents punch-through at high drain-source voltage due to the increased electric field in the channel that allow electrons to reach velocity saturation. The p⁺ sinker is then diffused to the n⁺ source connecting to the p⁺ substrate,

thus minimizing common lead inductance and maximizing common source amplifier gain, since the substrate itself is bonded to the RF ground. The Lightly Doped Drain (LDD) region, as previously mentioned, between the gate and drain allow for high breakdown voltages to be achieved. It is carefully designed to maintain a uniform electric field during voltage breakdown. Without the N- (LDD) region the applied voltage would appear across the gate and lead to breakdown in the substrate region by an impact generation process. Therefore, the LDMOS transistor would have a specific breakdown voltage based on the given oxide thickness when no N- (LDD) region exist.

Figure 3.6 Cross-section of LDMOS device [16]

The current in the LDMOS transistor flow in the lateral direction, thus no current crowding is produced, as illustrated in Figure 3.7.

Figure 3.7 Current path in an LDMOS transistor [11]

There are major advantages for using LDMOS, but there are also a few disadvantages when considering LDMOS. All MOSFETs in general are sensitive to transients due to the transistors high input resistance. Hot carrier induced degradation is another concern that affects LDMOS by causing parametric shifts over time. Current day LDMOS operate at high supply voltages that cause very high electric fields in the channel of the transistor. The drain current then ionizes electrons and holes around the drain by impact ionization, which results in hot electron and hot hole injection into the gate, as illustrated in Figure 3.8 [11].

The hot carrier injection problem worsens for wide-band linear applications like WCDMA due to the dependence on the quiescent bias operation of the technology. This phenomenon forces the transistor designers to sacrifice RF performance to achieve enhanced long-term stability. However, manufacturers have already begun applying a method that reduces the drift on the LDMOS transistor. Since gate-source drift occurs in the first few hours of a device life cycle manufacturers subject the LDMOS transistor to a burn-in mechanism for about 10 hours to minimize the effect of this phenomenon.

Figure 3.8 Hot carrier injection process [11]

The XML libraries from the simulation software provide the Motorola Electro Thermal LDMOS model transistor. It is an electro thermal model that accounts for dynamic self-heating effects and is designed for high power RF LDMOS transistors used in base

station applications. This new model can represent the current-voltage characteristic at any bias point. Thus, it will be used as the large-signal simulation representation model in this thesis.

In conclusion, LDMOSs' superior attributes, overall performance, and lower cost allow the technology to be perfectly suited for the cellular formats that are currently in place. This along with further developments in wireless infrastructure ensures LDMOS as the technology for emerging wireless networks, such as WCDMA.

Chapter 4

Microwave Office Design Simulation Software

4.1 Introduction

Power amplifier design is a combination of theoretical and practical analysis. The possible ways to accomplish amplifier design is by real world implementation or through software simulation. Currently support for the LDMOS transistors are nearly non-existent due to the fact that the transistor technology is fairly new. Also many industry leaders are very strict with releasing information concerning their LDMOS research due to industry competition. Just recently more experiments using LDMOS technology has started to surface. Thus, the most convenient avenue is to use simulation software to achieve the goals of this thesis.

There are several simulation software packages available in industry, but only a limited amount for academia. The most identified software packages are Genesys Vx and Microwave Office for industry. AppCad and PUFF are mainly used in academia. AppCad and PUFF have limited capabilities and lack necessary device files needed for the LDMOS transistor. Thus, industry standard software packages had to be pursued. Microwave Office and Genesys Vx are the industry leaders for simulation software.

However, no educational sponsorship exists for either software manufacturer. Both manufacturers provide a 30-day evaluation period to utilize and test the simulation software. Then a sales representative attempts to contact the evaluator near the end of the evaluation period. A 30-day evaluation license is not sufficient time to master either simulation tool, due to their many features. However, Genesys limits the amount of features available to the designer/user in their evaluation version. Microwave Office on the other hand does not. For the purpose of the thesis the Microwave Office simulation suite was selected.

4.2 Simulation Software Description

Applied Wave Research, Inc., (AWR) is a worldwide leader in high-frequency electronic design automation (EDA) software for wireless, high-speed wire-line, and electro-optical applications. Their revolutionary EDA solution increases engineering productivity and product development. AWR's approach results in a revolutionary hierarchical design that enables interactive tradeoffs between system requirements and circuit implementation. AWR's design solutions target implementations of electronic circuits and systems. Their solutions include a complete and integrated suite of EDA tools that streamline the design process from concept through simulation to physical implementation.

AWR's Microwave Office Design Suite combines linear and nonlinear circuit simulation with electromagnetic (EM) analysis and layout to provide the most powerful design solution available today for RF and microwave engineering. Microwave Office 2002

also includes a comprehensive “Filter Synthesis Wizard” that can incorporate measured and simulated data. Engineers can download fully functioning evaluation software at AWR’s website for a 30-day free trial period.

4.3 Microwave Office Architecture

The architecture of Microwave Office takes advantage of the advances in computer science, such as Component Object Model (COM). It provides a foundation for higher-level software integration that allows the pieces of Microwave Office 2002 to work together seamlessly. Microwave Office 2002 uses a single object oriented database that contains both electrical and physical properties that is directly connected to a variety of best-in-class simulation engines that provide "real-time tuning" and greater accuracy than conventional tools.

A “Filter Synthesis Wizard” is built into the Microwave Office design framework. It is activated from the project tree through a series of choices to generate lumped element or distributed filters including ideal transmission lines or physical structures. The wizard can synthesize Chebychev, Butterworth, Bessel, quasi-elliptic, linear phase and other filter topologies. One of the major advantages of the wizard is that the networks are created directly within the simulation environment rather than forcing users to employ a separate and often-incompatible filter-design application [19]. When the design is completed the results can be immediately tuned, optimized or combined with other designs within the same project space.

4.4 Design environment of simulation software

Figure 4.1 Microwave Office design environment

Figure 4.1 displays the AWR design environment for the Microwave Office on a Windows 2000 platform. The design environment is similar to the user's Window Explorer feature where the user folders are located on the left and files are on the right. In this case, however, the simulation designs and experimentation are performed on the right of the design environment.

We begin by observing the design environment components, as displayed in Figure 4.2.

Figure 4.2 Microwave Office design environment components

4.5 Menu

The main window contains the windows, components, menu selections and tools needed to create linear and nonlinear schematics, generate circuit layouts, create system diagrams, perform simulations, and display graphs. Many of the functions and

commands can be invoked from the menus and from the toolbar, and in some cases by right clicking on a node in the Project Browser.

4.6 Toolbar and Project Browser

The first step in building and simulating a design is to create a project. The project is used to organize and manage your designs and everything associated with them in a tree-like structure. A project can include any set of designs and linear and nonlinear schematics, EM structures or system level blocks. A project can include anything associated with the design, such as global parameter values, imported files, layout views, and output graphs. When you save a project, everything associated with it is automatically saved with an **.emp* file extension. Only one project can be active at a time. After a project has been created, the circuit designs can then be created. Layout representations of the designs can be generated and output the layout to a DXF, GDSII, or Gerber file. Simulations can be performed to analyze the designs and see the results on a variety of graphical forms that are specified. Then, the design can be tune or optimize the parameter values and variables as needed to achieve the response needed.

To create a new project choose **File > New Project**. Name the new project by choosing **File > Save Project As**. The name is reflected in the title bar.

To open an existing project, choose **File > Open Project**. To save the current project, choose **File > Save Project As**.

A Microwave Office project can include multiple linear and nonlinear schematics and netlists. After a schematic or netlist name is specified, a schematic or netlist window opens in the workspace and the Project Browser displays the new schematic or netlist as a sub-node of the folder **Circuit Schematics**. Subgroups of the new schematic or netlist contain all of the parameters and options that define and describe the schematic or netlist. In addition, the menu and toolbar display new choices particular to building and simulating schematics or netlists.

4.7 Element Browser and Work Space

The Element Browser gives access to a comprehensive database of hierarchical groups of circuit elements for schematics. The Library and Data folders in the Element Browser provide a wide range of electrical models and S-parameter files from manufacturers. Circuit elements include models, sources, ports, probes, measurement devices, data libraries, and model libraries that can be placed in a circuit schematic for linear and non-linear simulations.

- To view elements or system blocks, click the **Elem** tab in the lower left window. The Element Browser replaces the Project Browser window.

- To expand and contract the model categories, click the + and - symbols to view the desired subcategory, such as **Capacitor** or **Inductor**. The available models display in the lower windowpane.
- To place a model into a schematic or system diagram, simply click and drag it into the schematic or system diagram window, release the mouse button, right-click to rotate it if needed, position it, and click to place it.
- To edit model parameters, simply double-click on the element graphic in the schematic or system diagram window. A dialog box displays for you to specify new parameter values.

Sub-circuits allow the designer to construct hierarchical circuits by including a circuit block in a schematic. The circuit block can be a schematic, a netlist, an EM structure, or a data file.

- To add a sub-circuit to a schematic, click on **Subcircuits** in the Element Browser. The available sub-circuits display in the lower windowpane. These include all of the schematics, netlists, and EM structures associated with the project, as well as any imported data files defined for the project.

- To add a data file as a sub-circuit, it must first be imported and added to the project as an object. To do so, choose **Project > Add Data File**. Any imported data files are automatically shown in the list of available sub-circuits in the Element Browser
- To place the desired sub-circuit, simply click and drag it into the schematic window, release the mouse button, position it, and click to place it.
- To edit sub-circuit parameters, select the sub-circuit in the schematic window, right-click, and choose **Open Sub-circuit**. A schematic, netlist, EM structure, or data file opens in the workspace and can be edited in the same way that you would edit the individual circuit block types.

To add ports to a schematic expand the **Ports** category in the Element Browser. Under **Circuit Elements** click the desired Port subcategory. The available models display in the lower windowpane. Drag the port into the schematic or system diagram window, right-click to rotate it if needed, position it, and click to place it. To connect an element, position the cursor over a node. The cursor displays as a wire coil symbol. Click at this position to mark the beginning of the wire and slide the mouse to a location where a bend is needed. Click again to mark the bend point. To edit port parameters, double-click on

the port in the schematic or diagram windows to display a dialog box in which you can specify new parameter values.

4.8 Creating Graphs

Before a simulation is performed a graph needs to be created and the data specified, or measurements, that needs to be plotted. Measurements can include gain, noise or scattering coefficients. To create a graph, right-click on **Graphs** in the Project Browser, and choose **Add Graph** to display a dialog box in which to specify a graph name and type. An empty graph displays in the workspace and the graph name displays under **Graphs** in the Project Browser. The following graph types are available:

Table 4-1**Graph type available in Microwave Office**

Rectangular	Displays the measurement on an x-y axis, usually over frequency.
Constellation	Displays the in-phase (real) versus the quadrature (imaginary) component of a complex signal.
Smith Chart	Displays passive impedance or admittances in a reflection coefficient chart of unit radius.
Polar	Displays the magnitude and angle of the measurement.
Histogram	Displays the measurement as a histogram.
Antenna Plot	Displays the sweep dimension of the measurement as the angle and the data dimension of the measurement as the magnitude.
Tabular	Displays the measurement in columns of numbers, usually against frequency.

4.9 Performing Simulations

To run a simulation on the active project, choose **Simulate > Analyze**. The simulation is run automatically on the entire project, using the appropriate simulator. To set the simulation frequency, double-click the **Project Options** node in the Project Browser, or

choose **Options > Project Options** and then specify frequency values in the dialog box.

When the simulation is complete, you can view its output on the graphs and then easily tune and/or optimize as needed.

In summary, the Microwave Office simulation suite provides a wealth of features where the goals of this thesis can be met. Even though all features of the simulation software will not be used it will be a benefit for future projects.

Chapter 5

MRF21010 Transistor Validation

5.1 Introduction

The Motorola MRF21010 LDMOS transistor was selected for the power amplifier design used in this thesis. The MRF21010 incorporates the Motorola Electro Thermal model, which accounts for dynamic self-heating and was specifically tailored to model high power RF LDMOS transistors used in base station applications [17]. This MET model allows for most of the design considerations to be on stability, power gain, bandwidth, and DC requirements. Using the set of specifications associated with the MRF21010 LDMOS transistor a systematic mathematical approach will be used to determine the transistor viability for power amplifier circuit design.

5.2 MRF21010 Transistor

The MRF21010 transistor is an N-channel Enhancement Mode diffuse Lateral MOSFET designed for W-CDMA base station applications. It is suitable for FM, TDMA, CDMA and multi-carrier amplifier applications. MRF21010 is to be used in class AB. It has high gain, high efficiency, and high linearity characteristics, which is ideal for large-

signal common source amplifier applications in base stations. The MRF21010 transistor guarantees performance at 2140 MHz, 28 volts drain to source voltage and delivers an output power of 2.1 W, power gain of 12 dB, and an efficiency of 21% [18]. It is also an empirical large signal non-linear model, characterized with series equivalent large-signal impedance parameters and excellent thermal stability. Thus, the MRF21010 is capable of accurately representing the current-voltage characteristics at any bias point. More information on Motorola's Electro Thermal model can be obtained from [17].

5.3 Load and Source Impedance

The Motorola data sheet suggests an $I_{ds} = 100$ mA and $V_{ds} = 28$ V to bias the MRF21010 transistor. The values were achieved through the use of an IV-curve tracer and plotted, as shown in Figure 5.1. The method used was highly reproducible as the process was repeated several times for accuracy. Three different devices were used and each reproduced similar results. Thus, V_{gs} can be obtained from the IV-curve plot to ensure class AB operation.

Figure 5.1 I-V Characteristics of MRF21010 transistor

The source and load impedances were then selected from the Motorola data sheet in order to validate the transistor operating parameters. At 2110 MHz the conjugate source impedance is $Z_{IN} = 2.89 + j*5.04$ and a load impedance $Z_{OUT} = 2.76 + j*2.28$ as suggested by Motorola. Take note that Z_{OUT} was chosen based on tradeoffs between gain, output power, drain efficiency [18].

5.4 Simulation and measurement comparison

The operating condition for the amplifier design is $I_{ds} = 100$ mA and $V_{ds} = 28$ V as determined from the previous section. The MRF21010 transistor is then terminated with 50Ω and added as a sub-circuit to be later implemented. A harmonic balance test port is

implemented with a power signal swept from -10 dBm to 40 dBm. The harmonic balance port will also sweep across the specified frequency of 2110 MHz for the MRF21010 transistor [19]. Figure 5.2 displays the biasing circuit for simulation testing.

Figure 5.2 MRF21010 Biasing circuit for fundamental Harmonic Balance Simulation

In order to validate the MRF21010 transistor as a viable device for power amplifier design several measurement and simulation comparisons were performed. The following comparisons were...

1. Output power (dBm)
2. Power gain output (dB)
3. Power added efficiency

The output plot from each comparison was captured in the simulation software. The output power is the first comparison. First the voltage and current harmonic components for the biased MRF21010 amplifier circuit are captured and stored using equation 5.1 and 5.2.

$$\text{Voltage} = \text{MRF21010_bias:|VcompSP[PORT_2,1,1]|} \quad (5.1)$$

$$\text{Current} = \text{MRF21010_bias:|IcompSP[PORT_2,1,1]|} \quad (5.2)$$

Then the output power is calculated by multiplying the voltage components to the conjugate components of the current. Then the real components are extrapolated and multiplied by 0.5 using equation 5.3.

$$\text{Pout} = 0.5 * \text{real}(\text{Voltage} * \text{conj}(\text{Current})) \quad (5.3)$$

Finally, the log of the output power is calculated using equation 5.4 and plotted against the Non-linear harmonic power component, PcompSP, in dBm at the design frequency of 2.1 GHz. Figure 5.3 displays the output power in dBm for the first comparison.

$$P_{out_dBm} = 10 \cdot \log_{10}(P_{out} \cdot 1000) \quad (5.4)$$

Figure 5.3 Simulated and calculated output comparison

Figure 5.4 is the second measurement/simulation comparison for the power gain of the MRF21010 transistor. First the harmonic components are captured and stored using equation 5.5. The captured components represent the complex measurement of the harmonics. Thus, equation 5.6 is used to capture the real part. Finally, equation 5.7 converts the result to dB. Again there is good comparison between measurement and simulation.

$$\text{Gain_LSS} = \text{MRF21010_bias} : |\text{LSSnmSP}[\text{PORT_2}, \text{PORT_1}, 1, 1, 1]| \quad (5.5)$$

$$\text{Gain} = \text{real}(\text{Gain_LSS}) \quad (5.6)$$

$$\text{Gain2} = 20 \cdot \log_{10}(\text{Gain}) \quad (5.7)$$

Figure 5.4 Transducer gain comparison for the MRF21010 transistor

Figure 5.5 PAE comparison for the MRF21010 transistor

Figure 5.5 is the PAE comparison for the MRF21010 amplifier circuit. First the voltage and current for the gate and the drain need to be defined. Equations 5.8 – 5.11 will capture and store the voltage and current values for the drain and gate.

$$I_{gDC} = \text{MRF21010_bias:|IcompSP[I_METER.AMP2,0,1]|} \quad (5.8)$$

$$I_{dDC} = \text{MRF21010_bias:|IcompSP[I_METER.AMP1,0,1]|} \quad (5.9)$$

$$V_d = \text{MRF21010_bias:|VcompSP[V_METER.vm1,0,1]|} \quad (5.10)$$

$$V_g = \text{MRF21010_bias:|VcompSP[V_METER.VM2,0,1]|} \quad (5.11)$$

Then the real harmonic power component for the input is captured and stored for the power delivered at 2.1 GHz using equation 5.12.

$$P_{del_dBW} = \text{MRF21010_bias:Re(PcompSP[PORT_1,1,1])} \quad (5.12)$$

The input in this case is defined in dB. Thus, equation 5.13 is used to convert back to watts.

$$P_{del} = 10^{(P_{del_dBW}/10)} \quad (5.13)$$

Finally, incorporating equation 5.3 into equation 5.14 will result in the calculated PAE for the MRF21010 amplifier circuit.

$$PAE = 100 \cdot (P_{out} - P_{del}) / (V_d \cdot I_{dDC} + V_g \cdot I_{gDC}) \quad (5.14)$$

In summary, the output power and power gain compared very well between the simulated and the calculated results. However, the calculated and the simulated PAE did not. This can be attributed to the fact that the calculated PAE uses ideal values and the simulated PAE takes into account the characteristics of the component. In other words, in high frequency systems the power amplifier must amplify the signal as well as supply power to the load. In the amplification process, some power must be consumed with in the circuit elements of the power amplifier. Overall, the MRF21010 transistor can be considered a viable transistor for power amplifier circuit design for this thesis.

Chapter 6

Design Methodology

6.1 Introduction

The Motorola MRF21010 N-Channel Enhancement Mode Lateral Diffuse MOSFET (LDMOS) transistor was selected for the power amplifier design used in this thesis. The MRF21010 LDMOS transistor is designed for W-CDMA base station applications in the L-S frequency band. The operating conditions for the MRF21010 transistor is based on the specifications acquired from the data sheet [18]. The frequency range to be used in the simulation software was chosen to be from .9 to 3 GHz with a desired frequency at 2.1 GHz.

First the MRF21010 transistor is selected from the XML Libraries provided. A DC current/voltage curve tracer sweep and step outputs are connected to the drain and gate leads of the MRF21010 respectively. The voltage sweep and step range are specified according to the ON transistor characteristics data sheet specifications. Next, the circuit was simulated to acquire the IV-curve for the MRF21010 transistor, as illustrated in Figure 6.1. The step range for the IV-curve output had to be modified to locate the desired operating conditions of $V_{ds} = 28 \text{ V}$ and $I_{ds} = 100 \text{ mA}$.

Generally high power circuits have higher values for drain current and require a DC bias voltage applied to the gate and drain without disturbing the RF signal [20]. A biasing and decoupling circuit for dual supply is needed to accomplish this. Figure 6.2 displays a generic biasing decoupling circuit for FETs. It provides for low noise, high gain, high power, and high efficiency when implemented as an amplifier [7]. The inductor at the DC supply act as a RF choke by providing a very low DC resistance for biasing and a very high impedance at the RF frequencies to prevent the microwave signal from being shorted by the bias supply. The input /output decoupling capacitors allow microwave signals to pass while blocking the DC from the input/output lines [20].

Figure 6.1 MRF21010 IV-Characteristic Curve

Figure 6.2 Generic biasing and decoupling circuit for FET

S-parameters are not provided in the data sheet for the MRF21010 transistor. One possible reason is due to the fact that S-parameters do not apply to large power levels [20]. However, it is possible to extrapolate the S-parameters from the simulation software using the circuit of Figure 6.3 with 50Ω termination ports. Hence, the stability of the amplifier circuit can then be determined using the extrapolated S-parameters.

Figure 6.3 MRF21010 biased circuit

6.2 Stability Design

The ability for an amplifier not to oscillate is very important in the design process and can be determined by S-parameters, matching networks, and port terminations. In a two port network oscillations are possible when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$ and for the unilateral case when $|S_{11}| > 1$ or $|S_{22}| > 1$. However, a more straightforward, but lengthy approach, is to use Rollet's Stability factor K. A device is considered unconditionally stable if the Rollet's condition, defined as...

$$K = \frac{[1 - (|S_{11}|)^2 - (|S_{22}|)^2 + (|\Delta|)^2]}{2 \cdot |S_{12} \cdot S_{21}|} \quad (6.1)$$

with an auxiliary component...

$$|\Delta| = |S_{11} * S_{22} - S_{12} * S_{21}| \quad (6.2)$$

where the condition of...

$$K > 1 \text{ and } |\Delta| < 1$$

are satisfied. When $K < 1$, the device is considered conditionally stable or potentially stable which suggests that there are frequency points that produce oscillations due to external components. Since the simulation software has the ability to extrapolate the S-parameters it also has the ability to determine the K-factor. A Matlab script was created to validate the simulated results. First the magnitude and angle (in degrees) of the S-parameters are extrapolated and placed in tabular form. Next the Matlab script is initiated. The script begins by requesting the amount of iterations that needs to be performed, which corresponds to the amount of frequency points. Next the frequency for the first set of S-parameters is requested. Finally, the magnitude and angle (in degrees) for S_{11} , S_{21} , S_{12} , and S_{22} are inputted accordingly. This process continues for the specified iteration count. Twenty-two frequency points, from .9 to 3 GHz, were selected to calculate the K-factor. The simulated and calculated K-factor compared very well, thus, validating the accuracy of the simulation software. This comparison is illustrated in Table 6-1 and Figures 6.4 and 6.5 display the K-factor results. Figure 6.6 illustrates the small-signal S-parameters when DC bias is applied to the transistor.

Table 6-1:

Simulated S-Parameters for MRF21010 from .9 to 3 GHz at Vds = 28 V and Ids = 100 mA

(GHz)	S[1,1]	S[1,1] (Deg)	S[2,1]	S[2,1] (Deg)	S[1,2]	S[1,2] (Deg)	S[2,2]	S[2,2] (Deg)
0.9	0.98954	-170.48	0.006299	-72.405	0.006299	-72.405	0.99346	-167.6
1	0.98928	-173.1	0.003123	-67.508	0.003123	-67.508	0.99332	-170.15
1.1	0.98899	-175.45	0.000798	4.2175	0.000798	4.2175	0.99316	-172.38
1.2	0.98867	-177.59	0.002951	77.531	0.002951	77.531	0.99299	-174.38
1.3	0.98833	-179.58	0.005668	83.164	0.005668	83.164	0.99279	-176.21
1.4	0.98794	178.54	0.008383	83.948	0.008383	83.948	0.99258	-177.91
1.5	0.98752	176.73	0.011111	83.531	0.011111	83.531	0.99235	-179.51
1.6	0.98705	174.97	0.013884	82.654	0.013884	82.654	0.99209	178.97
1.7	0.98653	173.24	0.016734	81.556	0.016734	81.556	0.99181	177.5
1.8	0.98594	171.52	0.019692	80.331	0.019692	80.331	0.99149	176.07
1.9	0.9853	169.8	0.022793	79.019	0.022793	79.019	0.99114	174.67
2	0.98457	168.06	0.02607	77.639	0.02607	77.639	0.99076	173.28
2.1	0.98376	166.29	0.029561	76.196	0.029561	76.196	0.99032	171.89
2.2	0.98285	164.46	0.033308	74.69	0.033308	74.69	0.98983	170.49
2.3	0.98182	162.57	0.037356	73.117	0.037356	73.117	0.98928	169.08
2.4	0.98065	160.61	0.041759	71.469	0.041759	71.469	0.98866	167.64
2.5	0.97932	158.55	0.046577	69.738	0.046577	69.738	0.98795	166.17
2.6	0.9778	156.37	0.05188	67.912	0.05188	67.912	0.98714	164.65
2.7	0.97606	154.06	0.057751	65.977	0.057751	65.977	0.98621	163.08
2.8	0.97405	151.59	0.064287	63.916	0.064287	63.916	0.98513	161.44
2.9	0.97171	148.93	0.071602	61.712	0.071602	61.712	0.98388	159.73
3	0.96898	146.05	0.079834	59.342	0.079834	59.342	0.9824	157.92

Figure 6.4 Amplifier simulated K-factor

Figure 6.5 Amplifier calculated K-factor

Figure 6.6 S-parameter result for $K > 1$

Both Figures 6.4 and 6.5 illustrate that the K-factor is greater than one, which suggests that the transistor is unconditionally stable for the specified frequency range. Figure 6.6 displays the small-signal S-parameters where $S_{11} = -0.3631$ dB, $S_{21} = 9.261$ dB, $S_{12} = -17.42$ dB, and $S_{22} = -0.2225$. Thus, the transistor does not need to be modified to improve the stability prior to applying matching conditions. However, for large-signal analysis the amplifier circuit is not dependant on the small-signal S-parameters, but more on the external elements of the circuit. As mentioned before S-parameters do not apply for large power levels, but can be used to observe the stability characteristics of the transistor.

6.3 Matching Methodology

We will briefly review the small-signal analysis method, even though small-signal analysis S-parameters are not used for large-signal analysis other than to verify device stability. However, once the device has been established for stability then the input/output matching sections are designed to achieve a specified value of gain. The most common of the matching techniques emphasizes either maximum gain or constant gain. The proposed large-signal model in this thesis cannot use the small-signal simulation other than to verify stability. Thus, a large-signal approach for maximum gain similar to the small-signal analysis technique will be applied.

Maximum gain occurs when the impedance at the input/output sections of the transistor is conjugate matched to the impedance presented by the matching section [20]. In other words...

$$\Gamma_{IN} = \Gamma_S^* \quad (6.3a)$$

$$\Gamma_{OUT} = \Gamma_L^* \quad (6.3b)$$

Therefore, assuming lossless matching conditions the conjugate condition of equations 6.3a and 6.3b will maximize the overall transducer gain. Thus, the maximum gain can be calculated using...

$$G_{T_{\max}} = \frac{1}{[1 - (|\Gamma|^2)]} * (|S_{21}|)^2 * \frac{[1 - (|\Gamma_L|)^2]}{[1 - (S_{22} \Gamma_L)]^2} \quad (6.4)$$

However, when using a bilateral transistor, when ($S_{12} \neq 0$), the input reflection coefficient, Γ_{IN} , is affected by the output reflection coefficient, Γ_{OUT} , and vice-versa. Therefore, the input/output must be matched with the following...

$$\Gamma_{IN} = S_{11} + \frac{(S_{12} S_{21} \Gamma_L)}{1 - (S_{22} \Gamma_L)} \quad (6.5a)$$

$$\Gamma_{OUT} = S_{22} + \frac{(S_{12} S_{21} \Gamma_S)}{1 - (S_{11} \Gamma_S)} \quad (6.5b)$$

By applying the condition of equation 6.3a and 6.3b we can substitute into equations 6.5a and 6.5b to produce the following...

$$\Gamma_S^* = S_{11} + \frac{(S_{12} S_{21} \Gamma_L)}{1 - (S_{22} \Gamma_L)} \quad (6.6a)$$

$$\Gamma_L^* = S_{22} + \frac{(S_{12}^* S_{21} \Gamma_S)}{1 - (S_{11} \Gamma_S)} \quad (6.6b)$$

We then rewrite the equation for the source reflection coefficient as follows...

$$\Gamma_S = S_{11}^* + \frac{(S_{12}^* S_{21}^*)}{1 - \frac{\Gamma_L^* S_{22}^*}{1 - (S_{11} \Gamma_S)}} \quad (6.7)$$

$$\Gamma_L^* = \frac{[S_{22} - (\Delta \Gamma_S)]}{1 - (S_{11} \Gamma_S)} \quad (6.8)$$

where $\Delta = S_{11}^* S_{22} - S_{12}^* S_{21}$

The same method is then applied for the load reflection coefficients...

$$\Gamma_L = S_{22}^* + \frac{(S_{12}^* S_{21}^*)}{1 - \frac{\Gamma_S^* S_{11}^*}{1 - (S_{11} \Gamma_S)}} \quad (6.9)$$

$$\Gamma_S^* = \frac{[S_{11} - (\Delta \cdot \Gamma_L)]}{1 - (S_{22} \Gamma_L)} \quad (6.10)$$

Resolving equations 6.7 – 6.10 will yield a solution of equations 6.11 and 6.12 respectively [20] [7].

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4(|C_1|)^2}}{2 \cdot C_1} \quad (6.11)$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4(|C_2|)^2}}{2 \cdot C_2} \quad (6.12)$$

where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (6.13)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \quad (6.14)$$

$$C_1 = S_{11} - \Delta^* S_{22}^* \quad (6.15)$$

$$C_2 = S_{22} - \Delta^* S_{11}^* \quad (6.16)$$

An impedance smith chart can be used to find the matching sections for the transistor when the source and load reflection coefficients have been determined. The matching method can be accomplished in several different ways. The method of choice will depend on what application the transistor will be applied to, design frequency range, and performance requirements. The amplifier designer has full control based on what is required. The simulation approach in this thesis will use single stub and series matching as explained by [20] [7]. The circuit fabrication and simulation results will be illustrated in Chapter 7.

Chapter 7

Circuit Simulation Testing and Results

7.1 Introduction

The MRF21010 LDMOS transistor was chosen, because it is designed for W-CDMA base station applications. It is suitable for FM, TDMA, CDMA, and multicarrier amplifiers that operate in class AB for PCN-PCS/cellular radio and wireless local loop (WLL) applications [18]. The MRF21010 transistor has the following characteristics:

High gain

High efficiency

High linearity

Excellent thermal stability

which make the MRF21010 transistor a good choice from the LDMOS transistor family [5]. When the stability of the MRF21010 transistor has been determined through the simulation software it is then verified by a Matlab script code (Appendix A). The MRF21010 transistor IV-characteristic curve is generated using an IV curve tracer. Then using the ON-characteristics requirements from the data sheet allows for the proper

selection of the DC bias for the MRF21010 transistor. Large-signal analysis is then used to determine input/output microstrip lines for matching. The device will be matched similar to the maximum gain method described in the Chapter 6 of this thesis.

7.2 DC Biasing Methodology

There four recommended quiescent points for a FET to operate in. If the design requires a low noise, low-power application then a low voltage and a low current point is chosen (i.e. point A). If the design requires a low noise and a high power gain then a high current and low voltage point is chosen (i.e. point B). If the design requires that the output power be increased then a high voltage and mid-current is chosen (i.e. point C). If the design requires a class AB or B operation then a low drain-to-source current and a high voltage is chosen (i.e. point D) [7]. The selected voltage, $V_{DS} = 28 \text{ V}$, and current, $I_{DS} = 100 \text{ mA}$ correspond to the gate quiescent voltage needed to operate the MRF21010 transistor in class AB. Selecting the proper DC quiescent point is critical in the analysis due to the fact it is taken into effect by the simulation software. This and other large-signal parameters characterize the amplifier system.

7.3 Large-Signal Matching

The relationship for maximum gain of equation 6.3a and 6.3b do not satisfy the parameters for large-signal analysis. The small-signal S-parameters used to calculate the source, Γ_S , and load, Γ_L , coefficients do not apply for large power levels [20]. Therefore,

the large-signal reflection coefficients must be used and given for a specified frequency. The MRF21010 transistor data sheet provides the impedance at three frequencies in the frequency design range from .9 to 3 GHz. The intermediate frequency was selected for the purpose of this thesis, but any of the provided impedances could have been selected. The reflection coefficients were then extrapolated through the use of a Matlab script (appendix A) using the following equations...

$$\Gamma_{IN} = \frac{(Z_{IN} - Z_o)}{(Z_{IN} + Z_o)} \quad (7.1)$$

$$\Gamma_{OUT} = \frac{(Z_{OUT} - Z_o)}{(Z_{OUT} + Z_o)} \quad (7.2)$$

then apply the following condition [20]...

$$\Gamma_S = \Gamma_{IN}^* \quad (7.3a)$$

$$\Gamma_L = \Gamma_{OUT}^* \quad (7.3b)$$

Initially, the reflection coefficients were extrapolated using a characteristic impedance of 50Ω. However, the MRF21010 transistor data sheet provided a characteristic impedance of 10Ω. The reflection coefficients were extrapolated for the 10Ω impedance characteristic as well. The results for the reflection coefficients are listed in Table 7-1.

Table 7-1**Large-signal source/load reflection coefficients @ 2.1 GHz**

Z_0	Γ_S (mag)	Γ_S (deg)	Γ_L (mag)	Γ_L (deg)
10 Ω	.62969	-123.31°	.5856	-152.39°
50 Ω	.8917	-168.45°	.8956	-174.76°

Once the source and load reflection coefficients are obtained they are then plotted onto the smith chart to determine the transistor matching sections. The purpose for impedance matching is for the source and load reflection coefficients to be represented by impedance Z_S and Z_L . Then the impedance Z_S is the impedance looking into the input matching section towards source impedance Z_0 . The same action occurs with Z_L looking into the output matching section towards load impedance of Z_1 . Therefore, the input/output matching sections must transform Z_0 and Z_1 to the impedance Z_S and Z_L respectively.

To properly match amplifiers in order to deliver maximum power to a load or perform in a desired way the amplifier must be properly terminated at the input and output ports.

The L-section circuit type is chosen for this thesis, because of its simplicity and practicality. However, there are many different types of matching networks that can be designed to achieve matching [7]. A microstrip line is by definition a transmission line consisting of a strip conductor and a ground plane separated by a dielectric medium [7]. It is widely used in industry because it is easy to fabricate using a printed-circuit technique and interconnections for lumped and transistor devices are easily placed on its

metal surface. Figures 7.1 and 7.2 illustrate the source and load L-section networks respectively.

Figure 7.1 Source L-section for matching

Figure 7.2 Load L-section for matching

Figures 7.3 – 7.6 illustrate the technique used to conjugate match the MRF21010 transistor for stub and line design at 10Ω and 50Ω .

Figure 7.3 Smith chart measurement for input matching at 50Ω

Figure 7.4 Smith chart measurement for output matching at 50Ω

Figure 7.6 Smith chart measurement for output matching at 10Ω

7.4 Microstrip calculation and match network

At microwave frequencies microstrip lines are used due to its low loss and ease of implementation. To establish the dimensions of the microstrip we first need to find the width, W , as illustrated in Figure 7.7.

Figure 7.7 Microstrip for transmission line dimension [21]

Then the width of the microstrip can be determined for a known value of dielectric thickness, h , using equation 7.4 [7] [21].

$$\frac{W}{h} = \frac{8 \cdot \exp(H')}{\exp(2H') - 2} \quad (7.4)$$

The value of H' is determined when the dielectric constant, ϵ_r , of the material and the characteristic impedance, Z_0 , are known. Then equation 7.5 can be used to obtain the value of H' .

$$H' = \frac{Z_0 \sqrt{2(\epsilon_r + 1)}}{120} + \frac{1}{2} \cdot \left(\frac{\epsilon_r - 1}{\epsilon_r + 1} \right) \cdot \left(\ln\left(\frac{\pi}{2}\right) + \frac{1}{\epsilon_r} \cdot \ln\left(\frac{4}{\pi}\right) \right) \quad (7.5)$$

The microstrip lengths are determined next. The fact that the effective dielectric constant, ϵ_{reff} , is the relation of length in degrees to length in millimeters allow for various implementations for microstrip lines [7] [21]. The effective dielectric constant can be determined using equation 7.6.

$$\epsilon_{\text{reff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \left(1 + \frac{10h}{W} \right)^{-\frac{1}{2}} \quad (7.6)$$

The microstrip analysis begins by obtaining the dielectric constant from the MRF21010 data sheet, $\epsilon_r = 3.53$ [18]. A characteristic impedance of 50Ω and 10Ω are used to obtain different H' . A characteristic impedance of 50Ω produced $H' = 1.399$. A characteristic impedance of 10Ω produced $H' = 0.396$. The values were calculated using a Matlab script file. Table 7-2 displays the values for the variables from equations 7.4 – 7.6.

Table 7-2**Parameter results for Microstrip line design****with $h = .0005$ and $\epsilon_r = 3.53$**

Impedance	H'	W	ϵ_{reff}
10 Ω	0.396	.02857	3.432
50 Ω	1.399	.00112	2.807

Using the effective dielectric constant, ϵ_{reff} , the transmission line dimensions can be achieved for circuit fabrication through equation 7.7. The Λ value is then applied to the value of input and output line and stub from section 7.2. The results are then displayed in Table 7-3.

$$\Lambda = \frac{\lambda}{\sqrt{\epsilon_{\text{reff}}}} = \frac{v}{f_c \cdot \sqrt{\epsilon_{\text{reff}}}} \quad (7.7)$$

Where λ is in one lambda unit for free space and...

$v = 3 \times 10^8$ m/s (speed of light)

$f_c = 2.1$ GHz (center design frequency)

Table 7-3

Results for microstrip transmission line circuit fabrication

Impedance	Λ	Input line	Input stub	Output line	Output stub
10 Ω	.077113	.005190	.007441	.010171	.005999
50 Ω	.085227	.001057	.018674	.001791	.018657

Two final amplifier circuits are displayed for a 10 and 50 (Ω) characteristic impedance in Figures 7.8 and 7.9 respectively. The input and output parts are from the simulation software along with the DC biasing components.

Figure 7.8 Microstrip matched circuit using 10 Ω characteristic impedance

Figure 7.9 Microstrip matched circuit using 50Ω characteristic impedance

7.5 Simulation Test of Circuit Fabrication

The simulation begins by comparing the output characteristics of the matched 10 and 50 (Ω) fabricated circuits with the general class AB operated circuit before matching. The goal of matching is to maximize the input/output transfer. Thus, the matched condition that satisfies the match conjugate condition the best will be used. Figure 7.10 illustrates the class AB for the MRF21010 circuit. Only simulated results for the before and after match conjugate circuit will be compared since small-signal S-parameters do not satisfy high power levels and the MRF21010 transistor characteristics compared well with calculated values in Chapter 5.

Figure 7.10 MRF21010 Amplifier Circuit in Class (AB)

The following comparisons will be observed for non-conjugate match and conjugate match conditions...

1. Power and Efficiency
2. Power Spectrum
3. Output Power
4. Power over desired frequency range

The Motorola MRF21010 data sheet specifies an output power of 2.1 W and a power gain of 12 dB, with an efficiency of 21%. Using equation 7.8 [20] the required input power to

achieve the above data sheet characteristics will be obtained. Then the input power will be applied to the conjugate match circuit for comparison.

$$P_{in} \text{ (dBm)} = P_{out} \text{ (dBm)} - G_p \text{ (dB)} \quad (7.8)$$

where G_p is the common-source amplifier power gain. Thus, $P_{in} = 21.2$ dBm. Equation 7.9 is then used to calculate the power added efficiency, which includes the effect of the input across the specified frequency band.

$$PAE = \frac{(P_{out} - P_{in})}{P_{dc}} \quad (7.9)$$

The MRF21010 has a theoretical PAE = 70.27%, when $V_d = 28$ V and $I_d = 100$ mA.

The fabricated circuits were then compared to observe their PAE across an input power range from -10 dBm to 40 dBm. This test was essential to determine the validity of the characteristic impedance to be used. Once the impedance is identified the analysis of the circuit could then be continued. Figure 7.11 displays the result.

Figure 7.11 PAE comparison for all three fabricated circuits

It is clear that the MRF21010 transistor is not designed to operate using the assumed 50Ω characteristic impedance without additional circuit manipulation. The simulation software does not allow for the lumped element equivalent values to be manipulated, therefore, the 10Ω will be used. The 7.29% difference in PAE compared to the theoretical PAE is reasonable and suggests that the simulation takes into account loss in lumped elements.

Figure 7.12 Power and Efficiency of Amplifier w/o Matching

Figure 7.12 display the power and efficiency of the amplifier for an input power range from -10 dBm to 40 dBm. The amplifier total power, DC-to-RF and PAE are extrapolated. The result is populated in Table 7-4 at the calculated input power of 21.2 dBm.

Figure 7.13 Power and Efficiency of Amplifier with Matching

Figure 7.13 display the power and efficiency of the amplifier for an input power range from -10 dBm to 40 dBm. The amplifier total power, DC-to-RF and PAE are extrapolated. At the calculated input power of 21.2 dBm the conjugate matched amplifier display higher power and higher efficiency, as illustrated in Table 7-4.

Table 7-4

Results for Figure 7.12 and 7.13

Fabricated circuit	Total Power (dB)	DC-to-RF (%)	PAE (%)
Non-conjugate	31.61	20.17	20.01
Conjugate matched	35.61	28.22	27.28
Improvement amount	4	8.05	7.27

Figure 7.14 Power gain comparison w/o and with matching at 21.2 dBm

Figure 7.15 Delivered and Output Power for Amplifier Circuit w/o Matching

Figure 7.14 illustrates an increased in gain as expected. The 14.39 is .89 dB more than the specified gain for the MRF21010 datasheet [18]. Figure 7.15 and 7.16 display the output power for the non-matched case and the matched case. The two power outputs illustrate that both amplifier circuits perform well over the harmonics of the design frequency of 2.1 GHz. However, the amplifier output power at 2.1 GHz increased from 32.74 dBm (w/o matching) to 36.73 dBm (with matching). It is obvious that the difference in output power would be approximately 4 dB. Due to the fact that the Total Power from Table 7-4 demonstrated that there was a 4 dB improvement.

Figure 7.16 Delivered and Output Power for Amplifier Circuit with Matching

Another characteristics worth observing is the linear characteristics across the desired frequency band. 3G systems place stringent linearity requirements on power amplifiers. Figure 7.17 displays the characteristics of the fabricated amplifier with and without matching.

Figure 7.17 Output Power over specified frequency band w/o and with Matching

It is obvious from Figure 7.17 that the matched amplifier circuit has better linearity characteristics than the un-matched amplifier circuit. The matched amplifier circuit remains between 34 and 40 dB. The non-matched amplifier circuit drops from 35 dB to below 30 dB. Thus, the matched amplifier circuit is suited for applications that implement 3G systems. Overall the output characteristics for the MRF21010 transistor demonstrate an increase in output power. Thus, confirming that the matching L-section circuit works.

Chapter 8

Conclusion and Future Work

8.1 Conclusion

The microwave technique in this thesis implemented a methodological approach to match input and output transistor ports for power amplifier design. Prior to initiating the microwave technique the MRF21010 transistor had to be properly biased to operate in class AB as specified by the MRF21010 data sheet [1]. A $V_{ds} = 28$ V and $I_{ds} = 100$ mA were obtained from the transistor IV characteristic curve. The gate voltage was determined to be 3.744 V, which would ensure class AB operation for the MRF21010 transistor.

To preserve the transistor characteristics during the power amplifier design process the MRF21010 transistor ports 1 and 2 were terminated with 50Ω . Port 3 was set to ground. The MRF21010 transistor then was converted into a sub-circuit that can be implemented. Most high power transistor manufacturers do not include the small-signal S-parameters due to the fact that small-signal S-parameters do not apply to large power levels. However, the small-signal analysis of Rollet's stability factor, k , is valid when determining the stability of the transistor. The large-signal impedance was applied at the

input and output ports respectively to optimize results. The stability factor, k , was extrapolated from the simulation and verified with equations 6.1 and 6.2 using Matlab (appendix A). The results for unconditional stability were then illustrated in table 6.1 and in Figures 6.4 – 6.5. Figure 6.6 displays a positive small-signal gain due to the MRF21010 transistor characteristics.

Once the stability of the transistor has been verified the determination of the source and load reflection coefficients begins. The large-signal input and output impedance for a specific design frequency is used and usually supplied in the data sheet of the transistor. Equation 7.1 and 7.2 used large-signal input and output $Z_{IN} = 2.89 + j*5.04$ and $Z_{OL} = 2.76 + j*2.28$ for the specified frequency of 2.110 GHz. An assumed impedance of 50Ω was used to obtain the source and load reflection coefficients. However, the data sheet supplied a 10Ω characteristic impedance, which resulted in different values for the source and load reflection coefficients, as illustrated in Table 7-1. The matching analysis was performed with both conditions and the results were displayed in Figures 7.3 – 7.6 and in Table 7-2 and 7-3. A simulation test was performed to determine the correct characteristic impedance for the MRF21010 transistor by comparing the theoretical PAE value of 70.27% obtained from equation 7.9 for both conditions. The 10Ω characteristic impedance resulted in a 62.98% PAE which was closer to the theoretical value of 70.27%. The fabricated circuit from the 10Ω characteristic impedance was used to complete the simulation comparison.

The MET-LDMOS model, MRF21010, simplified the amplifier circuit fabrication process with thermal stability across the frequency range. This allowed for the design process to mainly focus on stability, power gain, DC requirements, output power, and efficiency. There was no need for additional lumped element circuits and matching conditions were applied directly when stability and DC biasing were determined. Thus, the simulation analysis was successful, because it demonstrated an improvement in amplifier output gain, efficiency, and power when microwave design techniques were applied. The improvement results for the total power, DC-to-RF efficiency, and PAE with a theoretical input power of 21.2 dBm are displayed in Table 7-4. Figures 7.14 – 7.17 demonstrate the output characteristics of the conjugate matched power amplifier circuit.

8.2 Recommendation and Future Work

The microwave technique is useful and powerful when it is combined with small and large signal simulation analysis. The methodology works with slight modifications to compensate for component characteristics. As demonstrated in this thesis assumed parameters would depend on the application requirements for the transistor. The conjugate match method is excellent when component verification is needed for specified power applications. Also it can provide a measure of the components ability. Thus, the microwave technique should be explored for hybrid communication systems in an attempt to improve the input to output characteristics of the system.

Microwave Office is an advance software tool for small-large signal analysis. It did not appear to have limitations due to its vast features. However, Microwave Office Design requires an understanding of circuit theory to properly utilize pre-configured components. For the purpose of this thesis only a basic understanding was needed to utilize the components required for simulation. Microwave Office is highly accepted by industry leaders, like Motorola, and provides XML libraries that produce real world results. The software package is updated with the newest component models and can be directly downloaded from Applied Wave Research's website with easy to follow instructions for installing. Microwave Office is highly advance compared to PUFF and competes almost equally with Genesis Vx, another industry leading simulation tool.

The advance features of Microwave Office in combination with microwave technique should be utilized for system simulation, such as feed-forward linearization, and other industry standard techniques for RF and communication development. Therefore, it is recommended that Microwave Office be considered for future implementation in RF and amplifier design courses in educational institutions to help close the widening gap between industry and academia.

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Appendix A

A.1 Script Code created in Matlab for stability calculation

This script was created to perform the tedious calculations necessary to obtain the stability factor for a power transistor. The script obtains the S-parameters from the user and performs the necessary calculations once all parameters have been entered.

```
% Filename: ktest.m
clear
n = input('How many times you want to compute ==> ');
for a = 1:n % set how many loop by user? for computation
% Calculation program to find the determinant of scattering parameter, Delta
% Created by Waldack Bonhome and assisted by Nuttrapong Futrakul (Graduate Colleague)
% prepare S11,S21,S12,S22
f(a) = input('What is frequency of this compute ==>');
M11= input('What is dB of S11 ==>> '); % put the dB of S11
R11= input('What is angle (in degree) of S11 ==>> '); % put angle of S11
% M11= 10^(M11/20)
TH11=R11*(2*pi/360); % change angle to radians by multiple 2*pi/360 for S11
[X11,Y11]=pol2cart(TH11,M11); % convert from polar form to complex form
S11= (X11 + i*Y11) % set S11 ready!
S11C=(X11 - i*Y11); % conjugate of S11
M21= input('What is dB of S21 ==>> ');
R21= input('What is angle (in degree) of S21 ==>> ');
% M21 = 10^(M21/20)
TH21=R21*(2*pi/360); % change angle to radians by multiple 2*pi/360 for S21
[X21,Y21]=pol2cart(TH21,M21); % convert from polar form to complex form
S21= (X21 + i*Y21) % set S21 ready!
M12= input('What is dB of S12 ==>> ');
R12= input('What is angle (in degree) of S12 ==>> ');
% M12= 10^(M12/20)
TH12=R12*(2*pi/360); % change angle to radians by multiple 2*pi/360 for S12
[X12,Y12]=pol2cart(TH12,M12); % convert from polar form to complex form
S12= (X12 + i*Y12) % set S12 ready!
```

```

M22= input('What is dB of S22 ==>> ');
R22= input('What is angle (in degree) of S22 ==>> ');
% M22= 10^(M22/20)
TH22=R22*(2*pi/360);      % change angle to radians by multiple 2*pi/360 for S22
[X22,Y22]=pol2cart(TH22,M22); % convert from polar form to complex form
S22= (X22 + i*Y22)        % set S22 ready!
S22C= (X22 - i*Y22);      % conjugate of S22
%=====
D=((S11*S22)-(S12*S21));    % D = delta = determinant of scattering matrix
Dx=real(D);                % get the real part of delta
Dy=imag(D);                % get the imaginary part of delta
DMag=abs(D);               % get the absolute value of delta
fprintf('\nThe absolute value of Delta = %f\n', DMag)
[DangR,DeltaM] = cart2pol(Dx,Dy);% convert complex form to polar form * DMag = DeltaM
Dang = DangR*(180/pi);      % Point that fix the degree convert
    if DangR < 0
        Dang = 360+Dang;
    else
        Dang = DangR*(180/pi);
    end
fprintf('The angle of scattering determinant (in degree) = %f\n',Dang)
% K factor to determine unconditional stability
% K > 1 , abs(D) < 1 , B1 > 0 will provide sufficient conditions for unconditional stability
K(a) = (1- (abs(S11))^2 -(abs(S22))^2 +(DMag)^2 ) / (2*(abs(S12*S21)));
fprintf('The Rollets Stability Factor, K = %f\n',K(a))
B1 = 1 + abs(S11)^2 - abs(S22)^2 - (DMag)^2
% Find i/p , o/p stability circle CS,RS,CL,RL
CpreS = (S11-(D*S22C));
CS = conj(CpreS)/(abs(S11)^2 - abs(D)^2); % find the center of i/p stability circle, CS
CSx = real(CS);
CSy = imag(CS);
[CS_angR,CS_Mag]=cart2pol(CSx,CSy); % convert complex to polar form, result in radian
CS_ang = CS_angR*(180/pi);      % convert angle in radian into degree
fprintf('The Magnitude of i/p stability circle with the center CS = %f\n', CS_Mag) %CS_Mag = Abs(CS)
fprintf('The angle of CS (in degree) = %f\n',CS_ang)
RS = abs((S12*S21)/[abs(S11)^2 - abs(D)^2]); % find the radius of o/p stability circle, RS

```



```

fprintf('The radius of i/p stability circle, RS = %f\n',RS)
CpreL = (S22-(D*S11C));
CL = conj(CpreL)/(abs(S22)^2 - abs(D)^2); % find the center of o/p stability circle, CL
CLx = real(CL); % get real part from CL
CLy = imag(CL); % get imaginary part from CL
[CL_angR,CL_Mag]=cart2pol(CLx,CLy); % convert complex to polar form, result in radian
CL_ang = CL_angR*(180/pi); % convert angle in radian into degree
fprintf('The Magnitude of o/p stability circle with the center CL = %f\n', CL_Mag) %CL_Mag =
Abs(CL)
fprintf('The angle of CL (in degree) = %f\n',CL_ang)
RL = abs((S12*S21)/[abs(S22)^2 - abs(D)^2]); % find the radius of o/p stability circle, RL
fprintf('The radius of o/p stability circle, RL = %f\n',RL)
fprintf(' ----- \n')
if K > 1 & B1 > 0 & DMag <1
    fprintf('The component has sufficient conditions for unconditional stability \n');
    fprintf('For Maximum gain design, Calculate input & output matching as below \n');
    %----Calculate source reflection coefficient,rS and load reflection coefficient,rL----
    %----|rS| = [B1 + _ sqrt( B1^2 - 4*abs(C1^2)) / 2*abs(C1)-----
    B2 = 1 + abs(S22)^2 - abs(S11)^2 - (DMag)^2 %set B2 eq., for matching calculation
    C1 = S11 - (D*S22C) %set C1 eq., for matching calculation
    C2 = S22 - (D*S11C) %set C2 eq., for matching calculation
    C1x=real(C1); % get real part from C1
    C1y=imag(C1); % get imaginary part from C1
    [C1_angR,C1_Mag]=cart2pol(C1x,C1y); % convert complex to polar form, result in radian
    C1_ang = C1_angR*(180/pi); % convert angle in radian into degree
    fprintf('The absolute value of C1 = %f\n', C1_Mag) %C1_Mag = Abs(C1)
    fprintf('The angle of C1 (in degree) = %f\n',C1_ang)
    C2x=real(C2); % get real part from C2
    C2y=imag(C2); % get imaginary part from C2
    [C2_angR,C2_Mag]=cart2pol(C2x,C2y); % convert complex to polar form, result in radian
    C2_ang = C2_angR*(180/pi); % convert angle in radian into degree
    fprintf('The absolute value of C2 = %f\n', C2_Mag) %C2_Mag = Abs(C2)
    fprintf('The angle of C2 (in degree) = %f\n',C2_ang)
    fprintf(' ----- \n')
    rSplus = (B1 + sqrt(B1^2 - 4*abs(C1)^2))/(2*C1) % calculate 1st condition, + to find the right rS
    rSpX = real(rSplus);

```

```

rSpY = imag(rSplplus);
[Ang_rSp,Mag_rSp]=cart2pol(rSpX,rSpY);
Ang_rSp_deg = Ang_rSp*(180/pi);
rSminus = (B1 - sqrt(B1^2 - 4*abs(C1)^2))/(2*C1)% calculate 2nd condition, - to find the right rS
rSmX = real(rSminus);
rSmY = imag(rSminus);
[Ang_rSm,Mag_rSm]=cart2pol(rSmX,rSmY);
Ang_rSm_deg = Ang_rSm*(180/pi);
    if Mag_rSp > Mag_rSm
        fprintf('\n The source reflection coefficient, rS = %f, Mag_rSm)
        fprintf('\n The angle of rS = %f\n',Ang_rSm_deg)
    else Mag_rSp < Mag_rSm
        fprintf('\n The source reflection coefficient, rS = %f, Mag_rSp)
        fprintf('\n The angle of rS = %f\n',Ang_rSp_deg)
    end
%----|rL| = [B2 +_ sqrt( B2^2 - 4*abs(C2)^2)] / 2*abs(C2)-----
rLplus = (B2 + sqrt(B2^2 - 4*abs(C2)^2))/(2*C2) % calculate 1st condition, + to find the right rL
rLpX = real(rLplus);
rLpY = imag(rLplus);
[Ang_rLp,Mag_rLp]=cart2pol(rLpX,rLpY);
Ang_rLp_deg = Ang_rLp*(180/pi);
rLminus = (B2 - sqrt(B2^2 - 4*abs(C2)^2))/(2*C2)% calculate 2nd condition, - to find the right rL
rLmX = real(rLminus);
rLmY = imag(rLminus);
[Ang_rLm,Mag_rLm]=cart2pol(rLmX,rLmY);
Ang_rLm_deg = Ang_rLm*(180/pi);
    if Mag_rLp > Mag_rLm
        fprintf('\n The load reflection coefficient, rL = %f, Mag_rLm)
        fprintf('\n The angle of rL = %f\n',Ang_rLm_deg)
    else Mag_rLp < Mag_rLm
        fprintf('\n The load reflection coefficient, rL = %f, Mag_rLp)
        fprintf('\n The angle of rL = %f\n',Ang_rLp_deg)
    end
elseif DMag > 1 & K > 1 & B1 > 0
    fprintf(' It is potentially unstable due to absolute delta > 1 \n');
elseif K < 1 & B1 > 0 & DMag < 1

```

```

        fprintf(' It is potentially unstable due to  $K < 1$  \n');
    elseif B1 < 0 & K > 1 & DMag < 1
        fprintf(' It is potentially unstable due to  $B1 < 0$  \n');
    else    fprintf(' It is potentially unstable cause by more than 1 factor \n');
    end
end
for a = 1:n
    fprintf(' K factor = %f,K(a))
end

%The effective gain factors for amplifier
if Mag_rSp > Mag_rSm

    Gs = 1/(1-(Mag_rSm)^2);
    fprintf('Gs = %f, Mag_rSm)

else Mag_rSp < Mag_rSm

    Gs = 1/(1-(Mag_rSp)^2);
    fprintf('Gs = %f, Mag_rSp)
end

if Mag_rLp > Mag_rLm

    GL = (1-(Mag_rLm)^2)/(1-(M22*Mag_rLm))^2;
    fprintf('GL = %f, Mag_rLm)

else Mag_rLp < Mag_rLm

    GL = (1-(Mag_rLp)^2)/(1-(M22*Mag_rLp))^2;
    fprintf('GL = %f, Mag_rLp)
end

Go = (M21)^2
fprintf (' \n----- \n')

```

A.2

Script Code created in Matlab for reflection calculation

This script was created to perform the large signal reflection calculations from the given large signal input/output impedance provided by the MRF21010 data sheet. The script obtains the necessary parameters from the user and performs the necessary calculations.

```
%Filename: reflections.m
```

```
%Created by: Waldack Bonhome
```

```
%=====
```

```
%Acquire impedance parameters for source and load reflection calculations
```

```
M21= input('What is S21 ==>> ');
```

```
R21= input('What is angle (in degree) of S21 ==>> ');
```

```
% M21 = 10^(M21/20)
```

```
TH21=R21*(2*pi/360);      % change angle to radians by multiple 2*pi/360 for S21
```

```
[X21,Y21]=pol2cart(TH21,M21); % convert from polar form to complex form
```

```
S21= (X21 + i*Y21)      % set S21 ready!
```

```
M22= input('What is S22 ==>> ');
```

```
R22= input('What is angle (in degree) of S22 ==>> ');
```

```
% M22= 10^(M22/20)
```

```
TH22=R22*(2*pi/360);      % change angle to radians by multiple 2*pi/360 for S22
```

```
[X22,Y22]=pol2cart(TH22,M22); % convert from polar form to complex form
```

```
S22= (X22 + i*Y22)      % set S22 ready!
```

```
S22C= (X22 - i*Y22);      % conjugate of S22
```

```

Z0 = input('Characteristic impedance > ');

xS = input('Real part > ');
yS = input('Imaginary part > ');
sS = (xS + i*yS)

reflec_S = (sS - Z0)/(sS + Z0);

reflecX = real(reflec_S);
reflecY = imag(reflec_S);
reflecMag = abs(reflec_S);

[reflec_angR,reflec_M] = cart2pol(reflecX,reflecY); % convert complex form to polar form * DMag =
DeltaM

Dang = reflec_angR*(360/(2*pi));           % Point that fix the degree convert

    if reflec_angR < 0

        Dang = 360+Dang;

    else

        Dang = reflec_angR*(360/(2*pi));

    end

xL = input('Real part > ');
yL = input('Imaginary part > ');
sL = (xL + i*yL)

reflec_L = (sL - Z0)/(sL + Z0);

reflecX2 = real(reflec_L);
reflecY2 = imag(reflec_L);

```

```

reflecMag2 = abs(reflec_L);

[reflec_angR2,reflec_M2] = cart2pol(reflecX2,reflecY2); % convert complex form to polar form * DMag
= DeltaM

Dang2 = reflec_angR2*(360/(2*pi));          % Point that fix the degree convert

if reflec_angR2 < 0

    Dang2 = 360+Dang2;

else

    Dang2 = reflec_angR2*(360/(2*pi));

end

fprintf('\nThe absolute value of source reflection = %f\n', reflecMag)

fprintf('The angle (in degrees) of source reflection = %f\n',Dang)

fprintf('\nThe absolute value load reflection = %f\n', reflecMag2)

fprintf('The angle (in degrees) of load reflection = %f\n',Dang2)


%The effective gain factors for amplifier


Gs = 1/(1-(reflecMag)^2)

Go = (M21)^2

G1 = (1-(reflecMag2)^2)/(1-(M22*reflecMag2))^2

```

A.3

Script Code created in Matlab for microstrip calculation

This script was created to perform the necessary calculations for microstrip matching analysis. The user enters the necessary parameters and the program performs the task and obtains the needed values.

```
%Transmission line calculations
%File name: microcalc.m
%Created by Waldack Bonhome
%=====
er = input('What is er > ');      %Collect all microstrip values for calculation
Zo = input('What is Zo > ');
h = input('What is the thickness in mm > ');
%h = h*10^-3;
fc = input('What is the center frequency in GHz > ');
fc = fc*10^9;
i_line = input('What is the source trans line > ');
i_stub = input('What is the source open stub > ');
l_line = input('What is the load trans line > ');
l_stub = input('What is the load open stub > ');

H = ((Zo*sqrt(2*(er+1)))/120)+(.5)*((er-1)/(er+1))*(log(pi/2)+(1/er)*log(4/pi));

W = h*((8*exp(H))/(exp(2*H)-2));
%W = W*1000
ereff = ((er+1)/2)+(((er-1)/2)*(1+((10*h)/W))^-0.5);

v = 3*10^8;

lamda = v/(fc*sqrt(ereff));      %perform lambda conversion

fprintf('\nH is equal to %f\n', H)
fprintf('\nW is equal to %f\n', W)
fprintf('\nereff is equal to %f\n', ereff)
fprintf('\nlamda is equal to %f\n', lamda)
```

%Transformation of line calculations

```
input_line = i_line*lamda;  
input_stub = i_stub*lamda;  
output_line = l_line*lamda;  
output_stub = l_stub*lamda;
```

```
lamda2 = 360;  
input_ldeg = i_line*lamda2;  
input_sdeg = i_stub*lamda2;  
output_ldeg = l_line*lamda2;  
output_sdeg = l_stub*lamda2;
```

```
fprintf('\nThe input line is equal to = %f --> %f (degrees)\n', input_line, input_ldeg)  
fprintf('\nThe input stub is equal to = %f --> %f (degrees)\n', input_stub, input_sdeg)  
fprintf('\nThe output line is equal to = %f --> %f (degrees)\n', output_line, output_ldeg)  
fprintf('\nThe output stub is equal to = %f --> %f (degrees)\n', output_stub, output_sdeg)
```


Appendix B

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Order this document
by MRF21010/D

The RF MOSFET Line **RF Power Field Effect Transistors** N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical W-CDMA Performance: -45 dBc ACPR, 2140 MHz, 28 Volts, 5 MHz Offset/4.096 MHz BW, 15 DTCH
Output Power — 2.1 Watts
Power Gain — 13.5 dB
Efficiency — 21%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR @ 28 Vdc, 2170 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF21010 MRF21010S

2170 MHz, 10 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs

CASE 360B-05, STYLE 1
(N-360)
(MRF21010)

CASE 360C-05, STYLE 1
(N-360S)
(MRF21010S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	43.75 0.25	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.5	$^\circ\text{C/W}$

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 3

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digital dna*

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 10\text{ }\mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 10\text{ V}$, $I_D = 50\text{ }\mu\text{A}$)	$V_{GS(th)}$	2.5	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ V}$, $I_D = 100\text{ mA}$)	$V_{GS(Q)}$	2.5	4	4.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ A}$)	$V_{DS(on)}$	—	0.4	0.5	Vdc
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 1\text{ A}$)	g_{fs}	—	0.95	—	S

DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	1	—	pF
--	-----------	---	---	---	----

FUNCTIONAL TESTS (In Motorola Test Fixture)

Two-Tone Common Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	G_{ps}	12	13.5	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	η	31	35	—	%
Third Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	IMD	—	-35	-30	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	IRL	—	-12	-10	dB
Output Power, 1 dB Compression Point, CW ($V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$)	P_{1dB}	—	11	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$)	G_{ps}	—	12	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$)	η	—	42	—	%
Output Mismatch Stress ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test

Figure 1. MRF21010 Test Circuit Schematic

Table 1. MRF21010 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1 * (eared)	2.2 pF Chip Capacitor, B Case	100B2R2BW	ATC
(earless)	1.8 pF Chip Capacitor, B Case	100B1R8BW	ATC
C2	0.5 pF Chip Capacitor, B Case	100B0R5BW	ATC
C3, C9	10 μ F, 35 V Tantalum Chip Capacitors	293D106X9035D2T	Sprague-Vishay
C4, C7	1 nF Chip Capacitors, B Case	100B102JW	ATC
C5, C6	5.6 pF Chip Capacitor, B Case	100B5R6BW	ATC
C8	470 μ F, 63 V Electrolytic Capacitor		
C10	10 pF Chip Capacitor, B Case	100B100GW	ATC
N1, N2	Type N Connector Flange Mounts	3052-1648-10	Macom
R1	1.0 k Ω Chip Resistor (0805)		
R2	12 Ω Chip Resistor (0805)		
PCB	Etched Circuit Board	C-XM-00-001-01	Cibel
Raw PCB material	0.030" Glass Teflon® ($\epsilon_r = 2.55$)	TLX8-0300	Taconic

* Piece part depending on eared / earless version of the device.

Figure 2. MRF21010 Test Circuit Component Layout

Figure 3. MRF21010 Demonstration Board Component Layout

Table 2. MRF21010 Demonstration Board Component Designations and Values

Designators	Description
C1	1 μ F Chip Capacitor (0805), AVX #08053G105ZATEA
C2, C6	10 μ F, 35 V Tantalum Capacitors, Vishay-Sprague #293D106X9035D
C3, C4	6.8 pF Chip Capacitors, ACCU-P (0805), AVX #08051J6R8CBT
C5	10 nF Chip Capacitor (0805), AVX #08055C103KATDA
C7	1.5 pF Chip Capacitor, ACCU-P (0805), AVX #08051J2R2BBT
C8, C10	0.5 pF Chip Capacitors, ACCU-P (0805), AVX #08051J0R5BBT
C9	10 pF Chip Capacitor, ACCU-P (0805), AVX #08055J100GBT
L1	19 mm $\times$ 1.07 mm
L2	7.7 mm $\times$ 13.8 mm
L3	9.3 mm $\times$ 22 mm
L4	17.7 mm $\times$ 3.5 mm
L5	3.4 mm $\times$ 1.5 mm
R1, R6	10 Ω , 1/8 W Chip Resistors (0805)
R2, R3	1 k Ω , 1/8 W Chip Resistors (0805)
R4	2.2 k Ω , 1/8 W Chip Resistor (0805)
R5	0 Ω , 1/8 W Chip Resistor (0805)
P1	5 k Ω Potentiometer CMS Cermet Multi-Turn, Bourns #3224W
T1	Voltage Regulator, Micro-8, Motorola #LP2951
T2	Bipolar NPN Transistor, SOT-23, Motorola #BC847
	RF Connectors Type SMA, Johnson #142-0701-631
	Substrate: Rogers RO4350, Thickness 0.5 mm, $\epsilon_r = 3.53$

TYPICAL CHARACTERISTICS

Figure 4. Class AB Broadband Circuit Performance

Figure 5. W-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

Figure 6. Intermodulation Distortion versus Output Power

Figure 7. Intermodulation Distortion Products versus Output Power

Figure 8. Power Gain versus Output Power

Figure 9. Intermodulation and Gain versus Supply Voltage

$V_{DD} = 28 \text{ V}$, $I_{DQ} = 100 \text{ mA}$, $P_{out} = 1 \text{ dB}$ (CW)

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1990	$2.85 + j4.38$	$2.93 + j1.71$
2110	$2.89 + j5.04$	$2.76 + j2.28$
2230	$2.73 + j6.19$	$2.83 + j2.59$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 10. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS

- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.805	20.18	20.45
B	0.225	0.235	5.72	5.87
C	0.195	0.195	3.18	4.55
D	0.210	0.220	5.33	5.58
E	0.055	0.065	1.40	1.65
F	0.094	0.096	0.10	0.15
G	0.545	BSC	14.29	BSC
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.365	9.07	9.27
Q	0.125	0.135	3.18	3.43
R	0.227	0.230	5.77	5.89
S	0.225	0.235	5.72	5.87
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
1. DRAIN
 2. GATE
 3. SOURCE

CASE 360B-05
ISSUE F
(NI-360)
(MRF21010)

- NOTES:
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 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.375	0.385	9.53	9.78
B	0.225	0.235	5.72	5.87
C	0.165	0.155	2.67	3.94
D	0.210	0.220	5.33	5.58
E	0.035	0.045	0.89	1.14
F	0.094	0.096	0.10	0.15
H	0.027	0.027	1.45	1.70
K	0.065	0.113	1.65	2.92
M	0.355	0.365	9.02	9.27
N	0.357	0.360	9.07	9.22
R	0.227	0.23	5.77	5.89
S	0.225	0.235	5.72	5.87
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

- STYLE 1:
1. DRAIN
 2. GATE
 3. SOURCE

360C-05
ISSUE D
(NI-360S)
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